## 32-Bit RISC Microcontroller

CMOS

## FR Family MB91110 Series

# MB91110/MB91V110

#### DESCRIPTION

The MB91110 series is a standard single-chip micro controller featuring various I/O resources and bus control mechanisms to incorporate the control with required for high performance high-speed CPU processes, having a 32-bit RISC CPU (FR30 series) in its core. Although external bus access is the basis for supporting a large address space accessible by a 32-bit CPU, a 1-KB instruction cache memory has been built-in to increase the instruction/ execution speed of the CPU.

This unit features the optimal specifications for incorporating applications that require high performance CPU processing power such as navigation systems, high performance facsimile systems, printer control, etc.

#### FEATURES

#### FR30CPU

- 32-bit RISC, load / store architecture, 5-level pipeline
- Operating frequency : external 25 MHz, internal 50 MHz
- Multi-purpose register : 32 bits × 16
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions for barrel shift, bit processing and inter memory transfers : Instructions suited to loading purposes



#### (Continued)

- Function entry / exit instruction, multi load / store instruction of register details : Instruction capable of handling High level language instruction.
- Register Interlock function : Simplification of assembler description
- · Branch instruction with delay slot : Reduction in overheads in case of branching
- Multiplier is built-in / Supported at instruction level Signed 32-bit multiplication : 5 cycles
   Signed 16-bit multiplication : 3 cycles
- Interruption (saving PC and PS) : 6 cycles, 16 priority levels

#### **Bus Interface**

- 24-bit address bus (16 MB space)
- Operating frequency : 25 MHz
- 16- / 8-bit data bus
- Basic external bus cycle : 2 clock cycles
- · Chip select output that can be set to a minimum 64-Kbyte units
- Interface support for various memories DRAM interface (areas 4, 5)
- Automatic waiting cycle : Can be randomly set from 0 to 7 cycles per area
- Unused data and address pins can be used as input/output ports.
- Supports "little endian" mode (One area is selected from areas 1 to 5)

#### **DRAM Interface**

- 2-bank individual control (area 4, 5)
- Normal mode / high speed page mode
- Basic bus cycles : normally 5 cycles, 1 cycle access is possible in high-speed page mode.
- Programmable waveform : 1 cycle waiting can be inserted automatically in RAS and CAS.
- DRAM refresh

CBR refresh (Interval is randomly set using the 6-bit timer.)

Self refresh mode

- Supports addresses for 8, 9, 10 and 12 columns
- 2CAS/1WE or 2WE/1CAS can be selected.

#### **Cache Memory**

- 1 KB instruction cache
- 2 way set associative
- 32 blocks / way, 4 entries (4 words) / block
- Lock function : Residing in the specified program codes at cache

#### DMA Controller (DMAC)

- 5 channels
- External  $\rightarrow$  external 2.5 access cycles / transfer (if 2 clock cycles are defined as 1 access cycle)
- Internal  $\rightarrow$  external 1.5 access cycles / transfer (if 2 clock cycles are defined as 1 access cycle)
- Address register (inc, dec, or reload are possible) : 32 bits  $\times$  5 channels
- Transfer count register (reload possible) : 16 bits × 5 channels
- Transfer factors : external pin / built-in resources interruption request / software
- Transfer sequence
  - Step transfer / block transfer
  - Burst / consecutive transfer
- Transfer data length : 8-bit, 16-bit or 32-bit can be selected
- Suspension is possible using NMI / interruption request

#### UART

- Fully duplicated double buffer
- Data length : 7 to 9 bits (without parity) , 6 to 8 bits (with parity)
- Asynchronous (start-stop synchronization) or CLK synchronized communication can be selected.
- Multiprocessor mode
- Dedicated baud rate generator is built-in.
- External clock can be used as the transfer clock
- · Baud rate clock can be output
- Error detection : parity, frame, overrun

#### **PPG Timer**

- 16 bits, 6 channels (frequency setting register / duty setting register)
- PWM function or one-shot function can be selected
- Initiation : Software or external trigger can be selected

#### A/D Converter (sequential conversion type)

- 10-bit resolution, 8 channels
- Sequential comparison conversion : 5.6  $\mu s$  in the case of 25 MHz
- Sample & hold circuit is built-in.
- Conversion mode : Single, scan or repeat conversion can be selected.
- Initiation : Software, external trigger or built-in timer can be selected.

#### **Reloading Timer**

- 16-bit timer : 2 channels
- Internal clock : 2 clock cycle resolutions, 2, 8 or 32 cycles can be selected.
- Pin input : event counter input / gate function
- · Rectangular wave output

#### **Other Interval Timer**

• Watchdog timer : 1 channel

#### **Bit Search Module**

• Searches the first "1" / "0" change bit positions within 1 cycle from MSB in 1 word.

#### Interruption Controller

- External interruption input : Mask impossible interruption ( $\overline{NMI}$ ), normal interruption × 8 (INT0 to INT7)
- Internal interruption factors : UART, DMAC, A/D, reloading timer, PPG timer, delay interruption
- Priority levels are programmable except for mask impossible interruption (16 levels)

#### **Reset Factors**

· Power-on reset / hardware standby / watchdog timer / software reset / external reset

#### Low Power Consumption Mode

Sleep / stop mode

#### **Clock Control**

• Gear functions : Operating clock frequencies peripheral to the CPU can be set randomly and independently. Gear locks can be selected from 1/1, 1/2, 1/4 or 1/8 (or 1/2, 1/4, 1/8, or 1/16).

#### Others

- Package : LQFP-144
- CMOS technology : 0.35 μm
- Power : 5.0 V  $\pm$  10%, 3.3 V  $\pm$  5%

### ■ PRODUCT LINEUP

	MB91V110 (For evaluation)	MB91110 (I-RAM mounted version)
I-RAM	16 Kbyte	16 Kbyte
RAM	5 Kbyte	5 Kbyte
ROM		
I-\$	1 Kbyte	1 Kbyte
DSU3 evaluation function	Mounted	

#### ■ PIN ASSIGNMENT



#### ■ PIN DESCRIPTIONS

Pin no.	Pin name	I/O*	Circuit type	Function
1 2 3 4 5 6 7 8	D16/P20 D17/P21 D18/P22 D19/P23 D20/P24 D21/P25 D22/P26 D23/P27	I/O	С	These pins use bits 16 to 23 of the external data bus. They can be used as a port (P20 to P27) if the external bus width is 8 bits.
10 11 12 13 14 15 16 17	D24 D25 D26 D27 D28 D29 D30 D31	I/O	С	These pins use bits 24 to 31 of the external data bus.
20 21 22 23 24 25 26 27	A00 A01 A02 A03 A04 A05 A06 A07	I/O	С	These pins use bits 00 to 07 of the external address bus.
29 30 31 32 33 34 35 36	A08 A09 A10 A11 A12 A13 A14 A15	I/O	С	These pins use bits 08 to 15 of the external address bus.
38 39 40 41 42 43 44 45	A16/P60 A17/P61 A18/P62 A19/P63 A20/P64 A21/P65 A22/P66 A23/P67	I/O	С	These pins use bits 16 to 23 of the external address bus.
48	RDY/P80	I/O	С	This is for external ready input. "0" is input if the bus cycle be- ing executed is incomplete. It can be used as a port when not otherwise used.
49	BGRNT/P81	I/O	Н	This is the external bus open reception output. "L" is output if the external bus is opened. It can be used as a port when not otherwise used.

Pin no.	Pin name	I/O*	Circuit type		Functio	n	
50	BRQ/P82	I/O	С	This is the ext external bus is not otherwise	This is the external bus open request input. "1" is input if the external bus is to be opened. It can be used as a port when not otherwise used.		
51	RD	0	G	This is the ext	ernal bus read strok	pe.	
52	WR0	0	G	This is the ext	ernal bus write strol	be.	
					16-bit bus width	8-bit bus width	
53	WR1/P85	I/O	н	D31-24	WR0	WR0	
				D23-16	WR1	(Port is possible)	
55	CS0	0	G	Chip select 0	output (Low active)		
56 57 58 59 60	CS1/PA1 CS2/PA2 CS3/PA3 CS4/PA4 CS5/PA5	I/O	н	Chip select 1 output (Low active) Chip select 2 output (Low active) Chip select 3 output (Low active) Chip select 4 output (Low active) Chip select 5 output (Low active) They can be used as ports when not otherwise used.			
61	CLK/PA6	I/O	н	This is the system clock output. The same clock as the stan- dard clock is output. This can be used as a port when not oth- erwise used.			
62 63 64 65 68 69 70 71	RAS0/PB0 CS0L/PB1 CS0H/PB2 DW0/PB3 RAS1/PB4 CS1L/PB5 CS1H/PB6 DW1/PB7	I/O	н	RAS output with DRAM bank 0. CASL output with DRAM bank 0. CASH output with DRAM bank 0. WE output with DRAM bank 0. (Low active) RAS output with DRAM bank 1. CASL output with DRAM bank 1. CASH output with DRAM bank 1. WE output with DRAM bank 1. They can be used as ports when not otherwise used			
72	NMI		E	Non Maskable	e Interrupt (NMI) inp	ut. (Low active)	
73 74 75	MD0 MD1 MD2	I	I	These are mode pins from 0 to 2. Basic MCU operation modes are set using these pins. They should be connected directly to Vcc or Vss for use.			
77 78	X0 X1	 0	A	Clock (oscillation) input. Clock (oscillation) output.			
80	RST	I	В	This is the ext	ernal reset input. (L	.ow active)	
81	HST	I	E	This is the ha	dware standby inpu	it. (Low active)	
83	(OPEN)			Set this to OP	EN.		
84 85 86	(OPEN) (OPEN) (OPEN)			Set this to OP	EN.		

Pin no.	Pin name	I/O*	Circuit type	Function	
87 88 89 90	(OPEN) (OPEN) (OPEN) (OPEN)	_		Set this to OPEN.	
91	(OPEN)	_		Set this to OPEN.	
92	AVcc	_	—	Vcc power supply for the A/D converter.	
93	AVRH			A/D converter reference voltage (high potential side). Be sure to turn on/off this pin with potential higher than AVRH applied to $V_{\rm CC}$ .	
94	AVRL		—	A/D converter reference voltage (low potential side).	
95	AVss	_	—	Vss power supply for the A/D converter.	
96 97 98 99 100 101 102 103	AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7	I	D	[AN0 to 7] A/D converter analog input.	
106	ATG/PE0	I/O	н	[ATG] This is the external trigger input for the A/D converter. This function is always used if selected as the initiation factor for A/D, so output by other functions should be stopped ex- cept when it is carried out intentionally.	
				[PE0] This is a general-purpose input/output port.	
107	TRG0, 3/PE1			[TRG0 to 5] These are external trigger input pins of the PPG.	
108 109	TRG1, 4/PE2 TRG2, 5/PE3	I/O	H	[PE1 to 3] These are general-purpose input/output ports.	
110 111 112 113 114	INT0/PF0 INT1/PF1 INT2/PF2 INT3/PF3 INT4/PF4	I/O	F	[INT0 to 7] These are external interruption request inputs. This input is always used while the corresponding external interruption is permitted, so output using other functions should be stopped except when carried out intentionally.	
115 116 117	INT5/PF5 INT6/PF6 INT7/PF7			[PF0 to 7] These are general-purpose input/output ports.	
119	DREQ0/PG0	I/O	н	[DREQ0] This is the DMA external transfer request input (ch 0) . This input is always used if selected as the transfer factor for DMAC, so outputs from other functions should be stopped except when carried out intentionally.	
				[PG0] This is a multi-purpose input/output port.	

Pin no.	Pin name	I/O*	Circuit type	Function
120			C	[DACK0] This is the DMAC external transfer request recep- tion output (ch 0) . This function is effective if the transfer re- quest reception output specification of DMAC is permitted.
120	DACK0/FG1	1/0	C	[PG1] This is a multi-purpose input/output port. This function is effective if the transfer request reception output specifica- tion of DMAC is prohibited.
101		1/0	C	[DEOP0] This is the DMA transfer end signal output (ch 0) . This function is effective if the transfer end signal output specification of DMAC is permitted.
121	DEOF0/FG2	1/0	C	[PG2] This is a multi-purpose input/output port. This function is effective if the transfer end signal output specification of DMAC is prohibited.
122	DREQ1/PG3	I/O	н	[DREQ1] This is the DMA external transfer request input (ch 1). This input is always used if selected as the transfer factor of DMAC, so output using other functions should be stopped except when carried out intentionally.
				[PG3] This is a multi-purpose input/output port.
100		1/0		[DACK1] This is the DMAC external transfer request recep- tion output (ch 1) . This function is effective if the transfer re- quest reception output specification of DMAC is permitted.
123	123 DACK1/PG4 1/0		C	[PG4] This is a multi-purpose input/output port. This function is effective if the transfer request reception output specifica- tion of DMAC is prohibited.
104			0	[DEOP1] This is the DMA transfer end signal output (ch 1) . This function is effective if the transfer end signal output specification of DMAC is permitted.
124	DEOP 1/PG5	1/0	C	[PG5] This is a multi-purpose input/output port. This function is effective if the transfer end signal output specification of DMAC is prohibited.
127	DREQ2/PH0	I/O	н	[DREQ2] This is the DMA external transfer request input (ch 2) . This input is always used if selected as the transfer factor of DMAC, so output using other functions should be stopped except when carried out intentionally.
				[PH0] This is a multi-purpose input/output port.
128	DACK2/PH1		C	[DACK2] This is the DMAC external transfer request recep- tion output (ch 2) . This function is effective if the transfer re- quest reception output specification of DMAC is permitted.
.20	5,012,1111			[PH1] This is a multi-purpose input/output port. This function is effective if the transfer request reception output specifica- tion of DMAC is prohibited.

Pin no.	Pin name	I/O*	Circuit type	Function
120		1/0	C	[DEOP2] This is the DMA transfer end signal output (ch 2) . This function is effective if the transfer end signal output specification of DMAC is permitted.
129	DEOF2/FII2	1/0	C	[PH2] This is a multi-purpose input/output port. This function is effective if the transfer end signal output specification of DMAC is prohibited.
130	SI/PH3	I/O	н	[SI] This is UART data input. This input is always used while UART inputs, so outputs from other functions should be stopped except when carried out intentionally.
				[PH3] This is a general-purpose input/output port.
				[SO] This is UART data output. This function is effective when UART data output specification is permitted.
131	SO/PH4	I/O	С	[PH4] This is a general-purpose input/output port. This func- tion is effective when UART data output specification is pro- hibited.
				[SCK] This is UART clock input/output. Clock output is effec- tive when UART clock output specification is permitted.
132	SCK/PH5	I/O	Н	[PH5] This is a general-purpose input/output port. This func- tion is effective when UART clock output specification is pro- hibited.
133	TI0/PH6	I/O	н	[TI0] This is reload timer 0 input. It is always used when re- load timer input is permitted, so outputs from other functions should be stopped except when carried out intentionally.
				[PH6] This is a general-purpose input/output port.
124		1/0	C	[TO0] This is reload timer 0 Output. This function is effective when reload timer specification is permitted.
134	100/11/	1/0		[PH7] This is a general-purpose input/output port. This func- tion is effective when reload timer specification is prohibited.
136	TI1/PI0	I/O	н	[TI1] This is reload timer 1 input. It is always used when re- load timer input is permitted, so outputs from other functions should be stopped except when carried out intentionally.
				[PI0] This is a general-purpose input/output port.
				[T01] This is the reload timer 1 output. This function is effec- tive if the output specification of the reload timer is permitted.
137	TO1/PI1	I/O	C	[PI1] This is a multi-purpose input/output port. This function is effective if the output specification of the reload timer is prohibited.

Pin no.	Pin name	I/O*	Circuit type	Function
138 139 140	PPG0/PI2 PPG1/PI3 PPG2/PI4	1/0	C	[PPG0 to 5] This is the PPG timer 1 output. This function is effective if the output specification of the PPG timer is permitted.
141 142 143	PPG3/PI5 PPG4/PI6 PPG5/PI7	1/0	C	[PI2 to 7] This is a multi-purpose input/output port. This func- tion is effective if the output specification of the PPG timer is prohibited.
18 46 66 76 104 125	Vcc5			This provides power for the 5 V digital circuit system.
47 82 126	Vcc3	_		This provides power for the 3 V digital circuit system.
9 19 28 37 54 67 79 105 118 135 144	Vss			This is the earth level for digital circuits.

\*: I/O shown above indicates input/output classification.

(Continued)

Note : The I/O port and resource input/outputs for most of the above pins are multiplexed, i.e. Pxx/xxxx. In the event of both the port and resource outputs were to use the same pins, the resource is given priority.

#### ■ I/O CIRCUIT TYPE



Туре	Circuit types	Remarks
E	Digital input	CMOS level hysteresis input Without standby control
F	Digital output	<ul> <li>CMOS level output</li> <li>CMOS level hysteresis input Without standby control</li> </ul>
G	Digital output	CMOS level output
Н	Digital output Digital output Digital output Digital input STANDBY CONTROL	<ul> <li>CMOS level output</li> <li>CMOS level hysteresis input With standby control</li> </ul>
I	Digital input	CMOS level input     Without standby control

#### ■ HANDLING DEVICES

#### • Preventing Latch-up

The "Latch-up" phenomenon may be generated if a voltage in excess of V<sub>cc</sub> or lower than V<sub>ss</sub> is applied to the input/output pins, or if the voltage exceeds the rating between V<sub>cc</sub> and V<sub>ss</sub>. If latch-up is generated, the electrical current increases significantly and may destroy certain components due to the excessive heat, so great care must be taken to ensure that the maximum rating is not exceeded during use.

#### • Handling Unused Input Pins

Input pins that are not used should be pulled up or down as they may cause erroneous operations if they are left open.

#### • External Reset Input

"L" level should be input to the  $\overline{RST}$  pin, which is required for at least five machine cycles to ensure the internal status is reset.

#### • Using External Clocks

If external clock is used, X0 pin should be provided, and X1 pin should be provided with reverse phase to X0 pin input. If the STOP mode (oscillation stop mode) is used simultaneously, the X1 pin is stopped with the "H" output. So, when STOP mode is specified, approximately 1 k $\Omega$  of resistance should be added externally. An example of the external clock usage methods is shown in the following circuit.



Note : Resistance must be added to the X1 pin if the STOP mode (oscillation stop mode) is used.

#### • Power Supply Pins

In products with multiple Vcc or Vss pins, the pins of the same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect Vcc and Vss pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 F between Vcc and Vss pins near the device.

#### • Crystal Oscillator Circuits

Noise around the X0 or X1 pins may cause erroneous operation. Make sure to provide bypass capacitors via shortest distances from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuits not cross the lines of other circuit.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended .

#### • N.C. Pins

N.C. pins must be opened for use.

#### • Mode Pins (MD0 to MD2)

Those pins must be directly connected to Vcc or Vss for use.

Pattern length between  $V_{cc}$  or  $V_{ss}$  and each mode pin on the printed-circuit board should be arranged to be as short as possible to prevent the test mode being erroneously turned on due to noise, they should also be connected with low impedance.

#### • In the Event that Power Is Turned on

The  $\overline{RST}$  pin must be started from "L" level when the power is turned on, and when the power is adjusted to the V<sub>cc</sub> level it should be changed to the "H" level after being left for at least five cycles of the internal operation clock.

#### • Original Oscillation Input in the Event that Power Is Turned on

The clock must be input until the waiting status for oscillation stability is reset in the event that power is turned on.

#### · Hardware Standby in the Event that Power Is Turned on

Standby is not set in the event that power is turned on while the HST pin is set at "L" level. The HST pin becomes effective after being reset, but it must first be returned to "H" level.

#### Power on Reset

When power is turned on, "Power on reset" must be executed. If the power voltage falls below the guaranteed operating voltage, "Power on reset" must be executed by turning on power supply again.

#### • Restrictions for Standby

Programs to be set for stop and sleep must be placed address area of the external memory. If placed in the RAM address area on the I-bus, operation can not be guaranteed after returning.

#### • Execution of Programs in I-RAM Areas

In the event that programs in the I-RAM areas are executed, enter the I-RAM areas in accordance with the JMP system instruction. Conversely, when changing from programs in the I-RAM area to those in other areas, exit in accordance with the JMP system instructions.

#### • Caution on Operation during PLL Clock Mode

If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.

#### BLOCK DIAGRAM



#### MEMORY SPACE

The FR30 series has 4 Gbytes (2<sup>32</sup> addresses) of logic address space which the CPU accesses linearly.

#### 1. Memory Map



Note : MB91110 series only supports external ROM external bus mode.

#### • Direct addressing area

The following areas of the address space are used for I/O. This area is called the "direct addressing area" and the address of the operand can be specified directly during instruction. The direct area differs depending on data size to be accessed.

- Byte data access : 0-0FFH
- Half-word data access : 0-1FFH
- Word data access : 0-3FF<sub>H</sub>

#### 2. Registers

There are two types of multi-purpose registers in the FR family. One is a dedicated purpose register that exists within the CPU and the other is a multi-purpose register that exists in the memory.

<ul> <li>Dedicated Registers</li> </ul>	
Program Counter (PC)	: 32-bit length; indicates instruction storage position.
Program Status (PS)	: 32-bit length; stores register pointers and condition codes.
Table Base Register (TBR)	: Holds the starting address of the vector table to be used for Exception, In- terruption and Trapping (EIT) .
Return Pointer (RP)	: Holds the address to which you will return to from the sub-routine.
System Stuck Pointer (SSP)	: Indicates the systems stuck position.
User Stuck Pointer (USP)	: Indicates the user's stuck position.
Multiplication and Division Results Resister (MDH/MDL)	: 32-bit length; These are the registers for multiplication and division.



#### • Program Status (PS)

PS is the register that holds the program status and is classified into three categories, namely, Condition Code Register (CCR), System Condition Code Register (SCR) and Interruption Level Master Register (ILM).



#### • Condition Code Register (CCR)

S flag : Specifies the stuck pointer to be used as R15.

- I flag : Controls permission and prohibition of user interruption requests.
- N flag : Indicates codes when the computation results are defined as integers that are expressed in complements of 2.
- Z flag : Indicates if arithmetic results were "0."
- V flag : Indicates when operands are used for computation and defined as integers expressed in complements of 2, and indicates whether or not an overflow is generated as a result of the computation.
- C flag : Indicates whether carrying or borrowing is generated from the highest bit as a result of the computation.

#### • System Condition Code Register (SCR)

T flag : Specifies whether or not the step- trace- trap will be valid.

#### • Interruption Level Mask Register (ILM)

ILM4 to ILM0 : Holds the interruption level mask values, and those values that are held by the ILM are used for the level mask. Interruption requests can only be accepted when the interruption levels handled within the interruption requests to be input into the CPU are stronger than the levels shown by the ILM.

ILM4	ILM3	ILM2	ILM1	ILM0	Interruption level	Strength
0	0	0	0	0	0	Strong
			Ť			
0	1	0	0	0	15	
			Ļ			
1	1	1	1	1	31	Weak

#### MULTI-PURPOSE REGISTERS

The multi-purpose registers are CPU registers (R0 to R15) which are used as accumulators for various computations and memory access pointers (field that indicates the address) .



Special purposes are assumed for the following three registers out of the 16 registers. Thus, some instructions are emphasized.

R13 : Virtual accumulator (AC)

R14 : Frame Pointer (FP)

R15 : Stack Pointer (SP)

Initial values for R0 to R14 on resetting are unspecified. The initial value of R15 will be 0000 0000H (SSP value).

#### ■ MODE SETTING

#### 1. Pins

Mode pins and set mode

N	lode pir	IS	Mode name	Mode name Reset vector Ex		Bus modes	
MD2	MD1	MD0	wode name	access areas	width	Bus modes	
0	0	0	External vector mode 0	External	8-bit	External ROM external	
0	0	1	External vector mode 1	External	16-bit	bus mode	
0	1	0	—			Setting is prohibited	
0	1	1	Internal vector mode	Internal	(Mode register)	Single chip mode*	
1						Usage is prohibited	

\*: MB91110 series is not supported single chip mode.

#### 2. Register

#### • Mode register (MODR) and set mode



#### • Bus mode set bit and its functions

M1	MO	Functions	Remarks
0	0	Single chip mode	Not supported
0	1	Internal ROM external bus mode	Not supported
1	0	External ROM external bus mode	
1	1		Setting is prohibited

#### ■ I/O MAP

Addross		Internal recourse				
Address	+0	+1	+2	+3	internal resource	
00000н		PDR2 (R/W)	_			
		XXXXXXXX				
000004н		PDR6 (R/W)	—	—		
	PDRB (R/W)	PDRA (R/W)		PDR8 (R/W)		
000008н	XXXXXXXX	- XXXXXX -	_	XXXX	Port data register	
00000Сн		_	_			
0000104			PDRE (R/W)	PDRF (R/W)	-	
			XXXX	XXXXXXXX		
000014 <sub>H</sub>	PDRG (R/W)	PDRH (R/W)	PDRI (R/W)			
	XXXXXX	XXXXXXXX	XXXXXXXX			
000018н		Reserved				
00001Cн		Reserved				
0000200	SSR (R/W)	SIDR/SODR (R/W)	SCR (R/W)	SMR (R/W)		
000020H	00001-00	XXXXXXXX	00000100	0000-00		
000024	CDCR (R/W)		_			
00002-11		0 1 1 1 1 1				
000028н	TMRLR	(W)	TMR	(R)		
	XXXXXXXX	XXXXXXXX	XXXXXXXX	XXXXXXXX	Reload timer 0	
00002Сн	_		TMCSR	(R/W)		
			0000	0000000		
000030н	TMRLR	(VV)	TMR	(R)		
	*****	****			Reload timer 1	
000034н	_		IMCSR	(K/W)		
		(P)		(PAM)	A/D converter	
000038н	XX	XXXXXXXX	00000000	00000000	(Sequential comparison type)	
00003Сн		_	_		Reserved	

Addroso	Register				
Address	+0 +1	+2	+3	Internal resource	
000040н				Reserved	
000044н	Access is prohibited	PCSR XXXXXXXX	(W) XXXXXXXX	DDCO	
000048н	PDUT (W) XXXXXXXX XXXXXXX	PCNH (R/W) 0000000-	PCNL (R/W) 00000000		
00004Сн	Access is prohibited	PCSR XXXXXXXX	(W) XXXXXXXX		
000050H	PDUT (W) XXXXXXXX XXXXXXX	PCNH (R/W) 0000000-	PCNL (R/W) 00000000		
000054н	Access is prohibited	PCSR XXXXXXXX	(W) XXXXXXXX	PPG2	
000058н	PDUT (W) XXXXXXXX XXXXXXX	PCNH (R/W) 0000000-	PCNL (R/W) 00000000	rr Gz	
00005Сн	Access is prohibited	PCSR XXXXXXXX	PCSR (W) XXXXXXXX XXXXXXX		
000060н	PDUT (W) XXXXXXXX XXXXXXX	PCNH (R/W) 0000000-	PCNL (R/W) 00000000		
000064н	Access is prohibited	PCSR XXXXXXXX	(W) XXXXXXXX		
000068н	PDUT (W) XXXXXXXX XXXXXXX	PCNH (R/W) 0000000-	PCNL (R/W) 00000000	- 2264	
00006Сн	Access is prohibited	PCSR XXXXXXXX	(W) XXXXXXXX	DDOG	
000070н	PDUT (W) XXXXXXXX XXXXXXX	PCNH (R/W) 0000000-	PCNL (R/W) 00000000		
000074н	-	· 			
000078н	-			Beconved	
00007Сн	-			Keserved	
000080H	-				

Addross	Register				
Address	+0	+1	+2	+3	Internal resource
000084н			_		
000088H			_		Reserved
00008Cн			_		
000090н			_		
000094 <sub>H</sub>	EIRR (R/W) 00000000	ENIR (R/W) 00000000		_	External interruption/
000098н	ELVR 00000000	(R/W) 00000000	_	_	NMI
00009Сн			_		
0000А0н	_				
0000A4н	_				
0000А8н			_		
0000ACн			_		
0000В0н			_		Reserved
0000В4н	—				
0000В8н	_				
0000BCH					
0000С0н					
0000C4н		_			

Addross		Internal resource			
Address	+0	+1	+2	+3	
0000C8H		-	_		Reserved
0000ССн		-	_		
0000D0н		_	DDRE (W) 0000	DDRF (W) 00000000	Data direction
0000D4н	DDRG (W) 000000	DDRH (W) 00000000	DDRI (W) 00000000		register
0000D8н to 0000FCн		Reserved			
000100н to 0001FCн		Reserved			
000200н	DMACS0 0-00-0				
<b>000204</b> н	DMACC0 XX	xx xxxx - xxx	xxxxxx xx	(R/W) XXXXXX	DMA controller channel 0
000208н	DMASA0 XXXXXX	xx xxxxxxxx	xxxxxx xx	(R/W) XXXXXX	
00020Cн	DMADA0 XXXXXX	xx xxxxxxxx	xxxxxx xx	(R/W) XXXXXX	
<b>000210</b> н	DMACS1 0-00-0				
<b>000214</b> н	DMACC1 XX	xx xxxx-xxx	xxxxxxx	(R/W) XXXXX	DMA controller
000218н	DMASA1 XXXXXX	xx xxxxxxx	xxxxxxx xx	(R/W) XXXXXX	channel 1
00021Cн	DMADA1 XXXXXX	xx xxxxxxx	xxxxxxx xx	(R/W) XXXXXX	

Addross		Internal resource			
Audress	+0	+1	+2	+3	internal resource
000220	DMACS2			(R/W)	
0002208	0 - 0 0 - 0	000 000000	XX-00000	- XX - X	
000224	DMACC2			(R/W)	
00022 <b>4</b> H	XX>	XXXXX-XXX	XXXXXXXX XXX	XXXXXX	DMA controller
000228	DMASA2			(R/W)	channel 2
000220H	XXXXXX	xx xxxxxxxx	XXXXXXXX XX	XXXXXX	
000220	DMADA2			(R/W)	
0002208	XXXXXX	xx xxxxxxxx	XXXXXXXX XX	XXXXXX	
0002304	DMACS3			(R/W)	
0002308	0 - 0 0 - 0	00 00 00 00	XX-00000	- XX - X	
000224	DMACC3			(R/W)	
000234H	XX>	XXXX-XXX	XXXXXXXX XXX	XXXXXX	DMA controller
000238	DMASA3			(R/W)	channel 3
000230H	XXXXXX	xx xxxxxxxx	XXXXXXXX XX	XXXXXX	
000230	DMADA3			(R/W)	
00023CH	XXXXXX	xx xxxxxxxx	XXXXXXXX XX	XXXXXX	
000240	DMACS4			(R/W)	
0002408	0-00-0	00 000000	XX-00000	XX - X	
000244	DMACC4			(R/W)	
0002448	XX>	XXXX-XXX	XXXXXXXX XXX	XXXXX	DMA controller
000248	DMASA4			(R/W)	channel 4
0002408	XXXXXX	xx xxxxxxxx	XXXXXXXX XX	XXXXXX	
00024Cu	DMADA4			(R/W)	
0002408	XXXXXX	xx xxxxxxxx	XXXXXXXX XX	XXXXXX	
0002500	DMACR			(R/W)	Overall DMA
0002308			0 0	0	controller
000254					
0002348		_	_		
000258					
000230H		_	_		Reserved
000250					
00023CH					
000260					
000200H		-			

Addross	Register				
Address	+0	+1	+2	+3	Internal resource
000264н		-	- 		
000268н		_	_		-
00026Cн		-			
000270н		_	_		Reserved
000274н		_	_		
000278н					
to 0002FCн		-	_		
000300н					-
to					
0003E0H					
0003E4н		_		000000	Instruction cache
0003E8н		-	_		Reserved
0003ECн		_		IRMC (R/W)	I-RAM control
0003F0н	BSD0 XXXXXX	xx xxxxxxxx	xxxxxxx xx	(W) XXXXXX	
000054	BSD1			(R/W)	-
0003F4H	XXXXXX	xx xxxxxxxx	xxxxxxx xx	XXXXXX	Dit aaarah madula
000259	BSDC			(W)	Bit search module
0003500	XXXXXX	XXX XXXXXXXX	XXXXXXXX XX	XXXXXX	
0003ECu	BSRR			(R)	
00001 04	XXXXXX	XX XXXXXXXX	XXXXXXXX XX	XXXXXX	
000400	ICR00 (R/W)	ICR01 (R/W)	ICR02 (R/W)	ICR03 (R/W)	
	11111	11111	11111	11111	Interruption controller
000404	ICR04 (R/W)	ICR05 (R/W)	ICR06 (R/W)	ICR07 (R/W)	
	11111	11111	11111	11111	

Addross		Internal resource			
Audress	+0	+1	+2	+3	internariesource
000408	ICR08 (R/W)	ICR09 (R/W)	ICR10 (R/W)	ICR11 (R/W)	
0004008	11111	11111	11111	11111	
000400	ICR12 (R/W)	ICR13 (R/W)	ICR14 (R/W)	ICR15 (R/W)	
0004004	11111	11111	11111	11111	
000410	ICR16 (R/W)	ICR17 (R/W)	ICR18 (R/W)	ICR19 (R/W)	
0004108	11111	11111	11111	11111	
000414	ICR20 (R/W)	ICR21 (R/W)	ICR22 (R/W)	ICR23 (R/W)	
0004148	11111	11111	11111	11111	
000/18.	ICR24 (R/W)	ICR25 (R/W)	ICR26 (R/W)	ICR27 (R/W)	
0004108	11111	11111	11111	11111	Interruption controller
000410	ICR28 (R/W)	ICR29 (R/W)	ICR30 (R/W)	ICR31 (R/W)	
0004104	11111	11111	11111	11111	
000420	ICR32 (R/W)	ICR33 (R/W)	ICR34 (R/W)	ICR35 (R/W)	
000420H	11111	11111	11111	11111	
000424	ICR36 (R/W)	ICR37 (R/W)	ICR38 (R/W)	ICR39 (R/W)	
0004248	11111	11111	11111	11111	
000428.	ICR40 (R/W)	ICR41 (R/W)	ICR42 (R/W)	ICR43 (R/W)	
0004208	11111	11111	11111	11111	
000420	ICR44 (R/W)	ICR45 (R/W)	ICR46 (R/W)	ICR47 (R/W)	
0004208	11111	11111	11111	11111	
000430	DICR (R/W)	HRCL (R/W)			Delay interruption
0004308	0	11111			Delay Interruption
000434н					
to 00047C⊦		_	_		Reserved
	RSRR/WTCR (R/W)	STCR (R/W)	PDRR (R/W)	CTBR (W)	
000480н	1 XXXX-0 0	000111	0000	xxxxxxx	
	GCR (R/W)	WPR (W)			Clock control area
<b>000484</b> н	110011-1	xxxxxxxx	_	_	
	PCTR (R/W)				
<b>000488</b> н	000				PLL control register
00048Cн		1			
to		_	_		Reserved
UUUUTUH					

(Continued)

Addroop		Internal recourse			
Address	+0	+1	+2	+3	Internal resource
000000		DDR2 (W)			
0006000		00000000			
000604		DDR6 (W)			Data direction
000004H		00000000			register
000608	DDRB (W)	DDRA (W)		DDR8 (W)	
000000	00000000	-00000-		0000	
000600	ASR1	(W)	AMR1	(W)	
00000CH	00000000	0000001	00000000	00000000	
000610	ASR2	(W)	AMR2	(W)	
000010H	00000000	0000010	00000000	00000000	
000614	ASR3	(W)	AMR3	(VV)	
0000148	00000000	0000011	00000000	00000000	
000618	ASR4	(VV)	AMR4	(VV)	
0000108	00000000	00000100	00000000	00000000	
00061Cu	ASR5	(VV)	AMR5	(VV)	External bus
0000101	00000000	00000101	00000000	00000000	interface
0006204	AMD0 (R/W)	AMD1 (R/W)	AMD32 (R/W)	AMD4 (R/W)	
00002011	00111	000000	00000000	000000	
000624	AMD5 (R/W)	DSCR (W)	RFCR	(R/W)	
00002 111	000000	00000000	XXXXXX	00000	
000628	EPCR0	(W)	EPCR1	(W)	
	1100	-1111111		11111111	
00062CH	DMCR4	(R/W)	DMCR5	(R/W)	
00002011	00000000	000000-	00000000	000000-	
000630н					Beeenved
0007F8н		_			Reserved
0007ECH			LER (W)	MODR (W)	"Little endian" register
			000	XXXXXXXX	Mode register

Note : Do not execute RMW instructions to registers with write-only bits. RMW instruction (RMW : Read / Modify / Write)

A	ND	Rj, @Ri	OR	Rj, @Ri	EOR	Rj, @Ri
A	NDH	Rj, @Ri	ORH	Rj, @Ri	EORH	Rj, @Ri
A	NDB	Rj, @Ri	ORB	Rj, @Ri	EORB	Rj, @Ri
В	BANDL	#u4, @Ri	BORL	#u4, @Ri	BEORL	#u4, @Ri
В	BANDH	#u4, @Ri	BORH	#u4, @Ri	BEORH	#u4, @Ri
Data in ar	ooo with	" " or rocort	d onoo	ia undopidad		

Data in areas with "—" or reserved ones is undecided.

### ■ INTERRUPTION VECTOR

Interruption factor and allocation of interruption vectors / interruption control registers are described in the interruption vector table.

	Interruption number		Interruption		Interruption vector
Interruption source	Decimal	Hexadeci- mal	level *1	Offset	address to TBR of default *2
Reset	0	00	—	3FCн	000FFFFCн
System reservation	1	01	—	3F8⊦	000FFFF8н
System reservation	2	02	—	3F4⊦	000FFFF4н
System reservation	3	03		3F0н	000FFFF0н
System reservation	4	04	—	ЗЕСн	000FFFECH
System reservation	5	05		3E8н	000FFFE8н
System reservation	6	06		3E4н	000FFFE4H
Coprocessor absence trap	7	07		3E0н	000FFFE0н
Coprocessor error trap	8	08	—	3DCн	000FFFDCн
INTE instruction	9	09	4 fixed	3D8н	000FFFD8н
System reservation	10	0A		3D4н	000FFFD4н
System reservation	11	0B		3D0н	000FFFD0н
Step trace trap	12	0C	4 fixed	3ССн	000FFFCCн
System reservation	13	0D	—	3С8н	000FFFC8н
Exceptions to undefined instructions	14	0E		3C4н	000FFFC4н
NMI request	15	0F	15 (F <sub>H</sub> ) fixed	3С0н	000FFFC0н
System reservation	16	10	ICR00	3ВСн	000FFFBCн
System reservation	17	11	ICR01	3В8н	000FFFB8H
External interruption 0	18	12	ICR02	3B4н	000FFFB4н
External interruption 1	19	13	ICR03	3В0н	000FFFB0н
External interruption 2	20	14	ICR04	ЗАСн	000FFFACн
External interruption 3	21	15	ICR05	3А8н	000FFFA8H
External interruption 4	22	16	ICR06	3А4н	000FFFA4н
External interruption 5	23	17	ICR07	3А0н	000FFFA0н
External interruption 6	24	18	ICR08	39Сн	000FFF9Cн
External interruption 7	25	19	ICR09	398н	000FFF98⊦
System reservation	26	1A	ICR10	394н	000FFF94н
UART reception completion	27	1B	ICR11	390н	000FFF90⊦
System reservation	28	1C	ICR12	<b>38С</b> н	000FFF8Cн
System reservation	29	1D	ICR13	388н	000FFF88н
UART transmission completion	30	1E	ICR14	384н	000FFF84H
System reservation	31	1F	ICR15	380н	000FFF80н

	Interruption number		Interruption		Interruption vector
Interruption source	Decimal	Hexadeci- mal	level *1	Offset	address to TBR of default *2
System reservation	32	20	ICR16	<b>37С</b> н	000FFF7Cн
DMAC0 (end, error)	33	21	ICR17	378н	000FFF78⊦
DMAC1 (end, error)	34	22	ICR18	374н	000FFF74н
DMAC2 (end, error)	35	23	ICR19	370н	000FFF70н
DMAC3 (end, error)	36	24	ICR20	<b>36С</b> н	000FFF6Cн
DMAC4 (end, error)	37	25	ICR21	<b>368</b> н	000FFF68⊦
System reservation	38	26	ICR22	364н	000FFF64н
System reservation	39	27	ICR23	360н	000FFF60н
System reservation	40	28	ICR24	<b>35С</b> н	000FFF5Cн
A/D sequential conversion type	41	29	ICR25	358н	000FFF58⊦
Reload timer 0	42	2A	ICR26	354н	000FFF54н
Reload timer 1	43	2B	ICR27	350н	000FFF50н
16-bit PPG timer 0	44	2C	ICR28	<b>34С</b> н	000FFF4Cн
16-bit PPG timer 1	45	2D	ICR29	<b>348</b> н	000FFF48н
16-bit PPG timer 2	46	2E	ICR30	344 <sub>H</sub>	000FFF44н
16-bit PPG timer 3	47	2F	ICR31	340н	000FFF40н
16-bit PPG timer 4	48	30	ICR32	33Сн	000FFF3Cн
16-bit PPG timer 5	49	31	ICR33	338н	000FFF38н
System reservation	50	32	ICR34	334н	000FFF34н
System reservation	51	33	ICR35	330н	000FFF30н
System reservation	52	34	ICR36	<b>32С</b> н	000FFF2Cн
System reservation	53	35	ICR37	328н	000FFF28н
System reservation	54	36	ICR38	324н	000FFF24н
System reservation	55	37	ICR39	320н	000FFF20н
System reservation	56	38	ICR40	<b>31С</b> н	000FFF1Cн
System reservation	57	39	ICR41	318 <sub>H</sub>	000FFF18⊦
System reservation	58	ЗA	ICR42	314н	000FFF14
System reservation	59	3B	ICR43	310н	000FFF10н
System reservation	60	3C	ICR44	<b>30С</b> н	000FFF0Cн
System reservation	61	3D	ICR45	308н	000FFF08н
System reservation	62	3E	ICR46	304н	000FFF04н
Delay interruption factor bit	63	3F	ICR47	300н	000FFF00н
System reservation (used under REALOS) *3	64	40		2FCн	000FFEFCH

(Continued)

	Interruption number		Interruption		Interruption vector
Interruption source	Decimal	Hexadeci- mal	level *1	Offset	address to TBR of default *2
System reservation (used under REALOS) *3	65	41		2F8н	000FFEF8⊦
Used under INT instruction	66 to 255	42 to FF	_	2F4н to 000н	000FFEF4н to 000FFD00н

\*1 : ICR sets the interruption level for each interruption request using the register built into the interruption controller. ICR is prepared in accordance with each interruption request.

- \*2 : TBR is the register that indicates the starting address of the vector table for EIT. Addresses with added offset values that are specified per TBR and EIT factor will be the vector addresses.
- \*3: REALOS OS/FR uses 0X40, 0X41 interruptions for system codes.

#### **Reference :**

The vector area for EIT is 1 KB in accordance with the address shown by TBR.

The size per vector is 4 bytes, and the relationship between the vector numbers and their addresses is shown as follows.

- vctadr = TBR + vctofs
  - = TBR + (3FC<sub>H</sub> 4 × vct)
    - vctadr : vector address vctofs : vector offset vct : vector number

#### PERIPHERAL RESOURCES

#### 1. I/O Port

MB91110 series can be used as the I/O port when settings for resources that handle each pin do not to use the pins for input/output.

#### Block diagram



#### • I/O Port Registers

I/O port is composed of the Port Data Register (PDR) and Data Direction Register (DDR) .

• In cases where the input mode is DDR = "0"

For PDR reading : Level of external pins to be handled is read out.

For PDR writing : Set value is written in PDR.

• In cases where the output mode is DDR = "1"

For PDR reading : PDR value is read out.

For PDR writing : Set value is written in PDR and the PDR value is simultaneously output to the externally handled pin.

#### 2. Port Data Register (PDR)

Port Data Register (PDR2-I) is the input/output data register for the I/O port. Input/output control is carried out by the handled data direction register (DDR2-I).

#### PDR2 Initial value Access 2 0 6 5 4 3 1 7 Address : 000001H XXXXXXXX<sub>B</sub> R/W P27 P24 P23 P22 P21 P20 P26 P25 PDR6 Initial value Access 7 6 5 4 3 2 1 0 Address : 000005H XXXXXXXX<sub>B</sub> R/W P67 P66 P65 P64 P63 P62 P61 P60 PDR8 Initial value Access 7 5 2 1 0 6 4 3 Address : 00000BH R/W - - X- - XXXв P81 P85 P82 P80 \_\_\_ \_\_\_\_ \_\_\_\_ \_\_\_\_ PDRA Initial value Access 4 3 2 0 7 6 5 1 Address : 000009н R/W - ХХХХХ- в PA6 PA5 PA4 PA3 PA2 PA1 PDRB Initial value Access 7 6 5 4 3 2 1 0 Address : 000008H XXXXXXXX<sub>B</sub> R/W PB7 PB6 PB5 PB4 PB3 PB2 PB1 PB0 PDRE Initial value Access 2 0 7 5 4 3 1 6 Address : 000012H R/W ---- XXXX<sub>в</sub> PE3 PE2 PE1 PE0 PDRF Initial value Access 7 6 5 4 3 2 1 0 Address : 000013H R/W XXXXXXXX<sub>B</sub> PF7 PF6 PF5 PF4 PF3 PF2 PF1 PF0 PDRG Initial value Access 5 4 3 2 0 7 6 1 Address : 000014H - - XXXXXXв R/W PG5 PG4 PG3 PG2 PG1 PG0 \_\_\_\_ \_\_\_\_ PDRH Initial value Access 6 5 4 3 2 0 7 1 Address : 000015H XXXXXXXX<sub>B</sub> R/W PH7 PH6 PH5 PH4 PH3 PH2 PH1 PH0 PDRI Initial value Access 4 3 2 0 7 6 5 1 Address : 000016H XXXXXXXXB R/W PI7 PI6 PI5 PI4 PI3 PI2 PI1 PI0

#### Port Data Register (PDR)

#### 3. Data Direction Register (DDR)

The Data Direction Register (DDR2-I) controls the input/output direction of the I/O port per bit. 0 is used for input and 1 is used to execute output control.

#### • Data Direction Register (DDR)

DDR2	7	6	5	4	3	2	1	0	Initial value Access
Address : 000601H	P27	P26	P25	P24	P23	P22	P21	P20	0000000в W
DDR6	7	6	5	4	3	2	1	0	Initial value Access
Address : 000605н	P67	P66	P65	P64	P63	P62	P61	P60	0000000 <sub>в</sub> W
DDR8	7	6	5	4	3	2	1	0	Initial value Access
Address : 00060BH	_	_	P85	_	_	P82	P81	P80	0-000в W
DDRA	7	6	5	4	3	2	1	0	Initial value Access
Address : 000609н	_	PA6	PA5	PA4	PA3	PA2	PA1	—	- 000000 -в W
DDRB	7	6	5	4	3	2	1	0	Initial value Access
Address : 000608н	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0	0000000 <sub>B</sub> W
DDRE	7	6	5	4	3	2	1	0	Initial value Access
Address : 0000D2H	_		—	_	PE3	PE2	PE1	PE0	W
DDRF	7	6	5	4	3	2	1	0	Initial value Access
Address : 0000D3н	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0	0000000 <sub>B</sub> W
DDRG	7	6	5	4	3	2	1	0	Initial value Access
Address : 0000D4H	_		PG5	PG4	PG3	PG2	PG1	PG0	000000в W
DDRH	7	6	5	4	3	2	1	0	Initial value Access
Address : 0000D5H	PH7	PH6	PH5	PH4	PH3	PH2	PH1	PH0	0000000 <sub>B</sub> W
DDRI	7	6	5	4	3	2	1	0	Initial value Access
Address : 0000D6н	PI7	PI6	PI5	PI4	PI3	Pl2	PI1	PI0	0000000 <sub>в</sub> W

#### 4. Instruction Cache

The instruction cache is a temporary storage memory. In the event that the instruction codes are accessed from a low speed external memory, it holds the accessed codes internally, and is used to increase the access speed for all subsequent accesses.

Direct read or write access can not be done by instruction cache or instruction cache tag using software.

#### • Cacheable area of the instruction cache

Instruction cache allows all space to become a cacheable area.

- Even though details of the external memory are updated by DMA transfer, it is not coherent with the cache details. In this case, coherency should be established by flushing the cache.
- Instruction cache configuration
- Basic instruction length of FR series : 2 bytes
- Block layout : 2-way set associative type
- Block
  - 1 way is configured of 32 blocks.
  - 1 block is 16 bytes ( = 4 sub blocks)
  - 1 sub block is 4 bytes ( = 1 bus access unit)

#### The instruction cache configuration is shown in the following figure.


### 5. Instruction Cache Control Register (ICHCR)

The Instruction Cache Control Register (ICHCR) controls the operation of the instruction cache. Writing to ICHCR may effect the cache operation of instructions to be retrieved within the next three cycles.

#### • Instruction Cache Control Register (ICHCR)

Instruction Cache Control Register (ICHCR) is shared for use by ways 1 and 2.



#### 6. Clock Generator (Low power consumption mechanism)

The clock generation area is a module with the following functions.

- CPU clock generation (including gear function)
- Peripheral clock generation (including gear function)
- Reset generation and holding factors
- Standby function (including hardware standby)
- Restraining DMA request
- PLL (Phase Locked Loop) is built in
- Register list

)480н )481н	RSR	R/W	TCR				ST	CR				1XXXX- 00в 000111 в	R/W R/W
)482н )483н				PD	RR		СТ	BR				0000в XXXXXXXXB	R/W W
0484н 0485н	GCR	R					W	PR				110011- 1 <sub>в</sub> XXXXXXXX <sub>в</sub>	R/W W
0488н	PCT	R										00 0 в	R/W

# Block diagram



# 7. Bus Interface Outline

The bus interface controls the interface with external memory and external I/O.

#### • Bus Interface Characteristics

- 24-bit (16 MB) address output
- 6 individual banks using chip selection function Random positional setting is possible on the logical address space at minimum 64-KB units. Total 16 MB  $\times$  6 areas can be set using the address pin and chip selection pin.
- 16/8-bit bus width can be set per chip selection area.
- Insertion of programmable "automatic memory wait" (maximum of 7 cycles)
- Supports DRAM interface

3 types of DRAM interface Double CAS DRAM (Normal DRAM I/F) Single CAS DRAM Hyper DRAM
2-bank individual control (control signal i.e. RAS and CAS) DRAM can be selected from 2CAS/1WE or 1CAS/2WE.
Supports high-speed page mode
Supports CBR / self refresh
Programmable corrugation

- Unused addresses / data pins can be used as I/O ports.
- Supports "little endian" mode
- Using clock doubler : Internal 50 MHz, external bus 25 MHz operation

#### Chip Selection Area

A total of six types of chip selection areas are prepared for the bus interface. The position of each area can be randomly arranged per 64 KB at least using area selection registers (ASR1 to 5) and area mask registers (AMR1 to 5) in an area of 4 GB. In the event that access to an external bus is attempted in areas that are specified by those registers, the supported chip selection signals ( $\overline{CS0}$  to  $\overline{CS5}$ ) become activated to "L". Such pins other than  $\overline{CS0}$  are deactivated to "H" when reset.

Note : The area 0 is allocated to space outside the area specified by ASR1 to ASR5. External areas other than 0001 0000H to 0005 FFFFH are deemed area 0 on resetting.

#### • Interface

The bus interface has the following interface types.

- Normal bus interface
- DRAM interface

These interfaces can only be used in predetermined areas. The following table shows each chip selection area and the usable interface functions. Which interface is to be used is selected in the Area Mode Register (AMD). If no selection is made, it defaults to the normal bus interface.

Chip Selection Area and Selectable Bus Interfaces

Aroos	5	Selectable bus interfac	e	Remarks		
Aleas	Normal bus	Time division	DRAM	Remarks		
0	0	—	—	On resetting		
1	0	—	_			
2	0	_	_			
3	0	—	_			
4	0	—	0			
5	0		0			



# Register List

Эн Ен	ASR1 (Area S	Select Reg. 1)	AMR1 (Area	a Mode Reg. 1)	00000000	00000001 в 00000000 в	W
0н 2н	ASR2 (Area S	Select Reg. 2)	AMR2 (Area	a Mode Reg. 2)	00000000 00000000	00000010 в 00000000 в	W W
4н 6н	ASR3 (Area S	Select Reg. 3)	AMR3 (Area	a Mode Reg. 3)	00000000 00000000	00000011 в 00000000 в	W W
8н Ан	ASR4 (Area S	Select Reg. 4)	AMR4 (Area	a Mode Reg. 4)	00000000 00000000	00000100 в 00000000 в	W W
Сн Ен	ASR5 (Area S	Select Reg. 5)	AMR5 (Area	a Mode Reg. 5)	00000000 00000000	00000101 в 00000000 в	W W
0н 2н	AMD0 *1	AMD1 *1	AMD32 *1	AMD4 *1	00111 00000000	0 00000 в 0 00000 в	R/W R/W
4н 6н	AMD5 *1	DSCR *2	RFCR (Refresh	Control Register)	0 00000 XXXXXX	00000000 в 00000 в	R/W R/W
8н Ан	EPCR0 (Externa	al Pin Control 0)	EPCR1 (Exter	nal Pin Control 1)	1100	- 0000000 в 11111111 в	W W
Сн Ен	DMCR4 (DRAM	Control Reg. 4)	DMCR5 (DRA	M Control Reg. 5)	00000000 00000000	000000- в 000000- в	R/W R/W
					_		
Сн			LER *3	MODR *4	00	XXXXXXXX в	W
*1	: AMD (Area MoDe reg	uister)					

#### 8. 16-bit Reload Timer

The 16-bit timer is composed of a 16-bit down counter, 16-bit reload register, a pre-scalar for internal count clock preparation and a control register. Selection of the input clock can be made from three types of internal clock (machine clocks with 2, 8 and 32 cycles) and an external clock are selectable for input clock.

#### · Characteristics of the 16-bit reload timer

The Pin Output (TO) outputs a toggle waveform whenever underflow is generated in reload mode, and outputs rectangular waves indicating that it is counting in the case of one shot mode.

Pin Input (TI) can be used for event input in the case of external event count mode, trigger input or gate input for internal clock mode.

If the external event count function is used as the reload mode, it can be used as the cycle device for the external clock.

In this type, a 2-channel timer is built-in.

Channel 0 of the reload timer can start up DMA transfer using the interruption request signal.

The DMA controller clears the interruption flag of the reload timer at the same time as receiving the transfer request.

The TO output from channel 0 for the reload timer is connected to the A/D converter inside the LSI. Thus, A/D conversion can be started on a cycle set at the reload register.

• Block Diagram



# Register List

Control sta	atus regi	ster (TN	ICSR)							A
Address	15	14	13	12	11	10	9	8	Initial value	Access
000036н		—	_	_	CSL1	CSL0	MOD2	MOD1	0000в	R/W
	7	6	5	4	3	2	1	0		
000037н	MOD0	OUTE	OUTL	RELD	INTE	UF	CNTE	TRG	0000000в	R/W
<ul> <li>16-bit time Address</li> <li>00002AH</li> <li>000032H</li> <li>16-bit reloa</li> <li>Address</li> </ul>	r registe	er (TMR)	) RLR)					0	Initial value xxxxxxxx xxxxxxs xxxxxxxx xxxxxxxx Initial value	Access W Access
000028н 000030н	15							0	XXXXXXXX XXXXXXXXXXXXXXXXXXXXXXXXXXXXX	W

### 9. PPG Timer

The PPG timer can output pulses that are synchronized with soft triggers or externally. Also, the cycle and duty of the output pulses can be changed randomly by replacing the two 16-bit register values. In this type, there are 6 built-in channels with this function.

#### • PPG timer function

The PPG timer has two functions as follows.

• PWM function

This can be synchronized to the trigger and is programmable to output pulses while rewriting the above register values. It can also be used as a D/A converter by using an additional circuit.

• One-shot function

This detects the edge of the trigger input and outputs a single pulse.

#### • Block Diagram



Register List

• Cycle setti Address 000046н 00004Ен 000056н 00005Ен 000066н 00006Ен	bit	egister (PCSR)	8	7	0	Initial XXXXXXXX	value XXXXXXXB	Access W
• Duty settir Address 000048н 000050н 000058н 000060н 000068н 000068н 000070н	ng re	gister (PDUT) <sup>15</sup>	8	7	0	Initia XXXXXXXX	value XXXXXXX <sub>B</sub>	Access W
• Control/sta Address 00004Ан 000052н 00005Ан 000062н 00006Ан 000072н	atus bit	register (PCNH/ 15	PCNL) 8	7	0	Initia 0000000 -	l value 00000000₀	Access R/W

#### 10. External Interruption/NMI Control Area

The external interruption / NMI control area controls the external interruption requests to be input to the  $\overline{\text{NMI}}$  and INT0 to INT7. "H" or "L" and "rising edge" or "falling edge" can be selected as the requested detection level (except for NMI). Also, four requests from INT0 to INT3 can be used as the DMA request.

#### • Block diagram



#### Register list

External interval	errupti	on perm	nission r	egister	(ENIR)					Initial value	A
Address	DIL	7	6	5	4	3	2	1	0	Initial value	Access
000095н		EN7	EN6	EN5	EN4	EN3	EN2	EN1	EN0	0000000в	R/W
<ul> <li>External internal</li> </ul>	errupti	on facto	ors regis	ter (EIR	R)						
Address	bit	15	14	13	12	11	10	9	8		
000094н		ER7	ER6	ER5	ER4	ER3	ER2	ER1	ER0	0000000в	R/W
Request lev	vel sett	ing regi	ster (EL	.VR)							
Address	bit	15	14	13	12	11	10	9	8		
000098н		LB7	LA7	LB6	LA6	LB5	LA5	LB4	LA4	0000000в	R/W
	bit	7	6	5	4	3	2	1	0		
000099н		LB3	LA3	LB2	LA2	LB1	LA1	LB0	LA0	0000000в	R/W

# **11. Delay Interruption Modules**

This is a module to generate interruptions to switch tasks. This module can be used with software to generate/ cancel interruption requests to the CPU.

### Block diagram



Address	bit	7	6	5	4	3	2	1	0	Initial value Access
000430н			_	_	_	_	_	_	DLYI	0в R/W
	•			•			•			

### 12. Interruption Controller

The interruption controller carries out interruption reception and arbitration.

#### · Hardware configuration of the interruption controller

This module is configured for the following items.

- ICR register
- Interruption priority judgement circuit
- Interruption level, interruption number (vector) generation area
- Cancellation request generation area for HOLD request

#### • Major interruption controller functions

This module has the following functions.

- Detection of NMI request / interruption request
- Priority grade judgement (depending on the level and number)
- Transferring interruption level of factors for the judgement results (to CPU)
- Transferring interruption number of factors for the judgement results (to CPU)
- Recovery instruction from stop mode by generating NMI / interruption
- Cancellation of HOLD request to the bus master

• Block Diagram



\*3 : HLDCAN is the bus vacation request signal to bus masters other than the CPU.

# Register list

Address	bit 7	6	5	4	3	2	1	0		Initial value	Acces
000400н	—	—		ICR4	ICR3	ICR2	ICR1	ICR0	ICR00	11111	R/W
000401н	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR01	11111	R/W
000402н	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR02	11111	R/W
000403н	_			ICR4	ICR3	ICR2	ICR1	ICR0	ICR03	11111	R/W
000404н	_		_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR04	11111	R/W
000405н	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR05	11111	R/W
000406н	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR06	11111	R/W
000407н	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR07	11111	R/W
<b>000408</b> н	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR08	11111	R/W
000409н			_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR09	11111	R/W
00040Ан	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR10	11111	R/W
00040Bн	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR11	11111	R/W
00040CH	_	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR12	11111	R/W
00040DH		_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR13	11111	R/W
00040EH		_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR14	11111	R/W
00040FH	_		_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR15	11111	R/W
000410 <sub>H</sub>		<u> </u>	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR16	11111	R/W
000411 <sub>H</sub>				ICR4	ICR3	ICR2	ICR1	ICRO	ICR17	11111	R/W
000412				ICR4	ICR3	ICR2	ICR1	ICRO	ICR18	11111	R/W
000413					ICP3	ICR2				11111	P/M
000413											
0004148											
0004158			_		ICR3						
000410H					ICR3						
0004178			_		ICR3						
000416H			_	ICR4	ICR3	ICR2	ICRI	ICRU	ICR24	11111	R/W
000419H				ICR4	ICR3	ICR2	ICR1	ICRU	ICR25	11111	R/W
00041AH				ICR4	ICR3	ICR2	ICR1	ICR0	ICR26	11111	R/W
00041BH				ICR4	ICR3	ICR2	ICR1	ICR0	ICR27	11111	R/W
00041CH				ICR4	ICR3	ICR2	ICR1	ICR0	ICR28	11111	R/W
00041DH			—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR29	11111	R/W
00041Eн			—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR30	11111	R/W
00041Fн	_	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR31	11111	R/W
000420н	_	_	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR32	11111	R/W
000421н			—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR33	11111	R/W
000422н		—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR34	11111	R/W
000423н			—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR35	11111	R/W
000424н	_	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR36	11111	R/W
000425н	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR37	11111	R/W
000426н		—	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR38	11111	R/W
000427н	—	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR39	11111	R/W
000428н	_	—	—	ICR4	ICR3	ICR2	ICR1	ICR0	ICR40	11111	R/W
000429н		—		ICR4	ICR3	ICR2	ICR1	ICR0	ICR41	11111	R/W
00042Ан		_		ICR4	ICR3	ICR2	ICR1	ICR0	ICR42	11111	R/W
00042Bн		—	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR43	11111	R/W
00042Сн	—	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR44	11111	R/W
00042DH	—	_	_	ICR4	ICR3	ICR2	ICR1	ICR0	ICR45	11111	R/W
00042Eн	—	—		ICR4	ICR3	ICR2	ICR1	ICR0	ICR46	11111	R/W
00042Fн	—	—		ICR4	ICR3	ICR2	ICR1	ICR0	ICR47	11111	R/W
		•	•	R	R/W	R/W	R/W	R/W			
000431н	_		_	LVL4	LVL3	LVL2	LVL1	LVL0	HRCL	11111	R/W
	·	-		R	R/W	R/W	R/W	R/W			

# 13. Interruption Control Register (ICR)

This function is set up per interruption input and sets the interruption level of interruption requests to be handled.

#### Register list



#### [bit 4 to 0] ICR4 to 0

The interruption level of the interruption requests that are handled is specified by the interruption level setting bit. In cases where the interruption level that is set in this register is the same as or more than the level mask value that is set (has been set) in the ILM register of the CPU, the interruption request is masked at the CPU side. It is initialized to  $11111_B$  on resetting. The settable interruption level setting bit and interruption level are shown in following Table.

ICR4	ICR3	ICR2	ICR1	ICR0		Interruption level
0	0	0	0	0	0	A System reconvetion
0	1	1	1	0	14	▼ System reservation
0	1	1	1	1	15	NMI
1	0	0	0	0	16	Maximum settable level
1	0	0	0	1	17	♦ (High)
1	0	0	1	0	18	
1	0	0	1	1	19	
1	0	1	0	0	20	
1	0	1	0	1	21	
1	0	1	1	0	22	
1	0	1	1	1	23	
1	1	0	0	0	24	
1	1	0	0	1	25	
1	1	0	1	0	26	
1	1	0	1	1	27	
1	1	1	0	0	28	
1	1	1	0	1	29	
1	1	1	1	0	30	(Low)
1	1	1	1	1	31	Interruption is prohibited

#### Interruption Level Setting Bit and Interruption Level

Note: ICR 4 is fixed as "1" and can not be written as "0".

### 14. 10-bit A/D Converter

The A/D converter is the module that converts analog input voltages to a digital value.

#### • Characteristics of A/D Converter

- Minimum converting time : 5.6 µs/channel
- Sample & hold circuit is built-in.
- Resolution : 10 bits
- Selection can be made for analog input from 8 channels.

Single conversion mode	: 1 channel is selected for conversion
Scan conversion mode	: Converts multiple number of consecutive channels. Maximum 8 channels are programmable.
Consecutive conversion mode	: Repeatedly converts the specified channel.
Suspension / conversion mode	: Suspends after converting 1 channel and waits until the next one is started up (synchronization for starting conversion is possible)

- Initiation of DMA transfer by interruption is possible.
- Initiation factor can be selected from software, external trigger (falling edge) or reload timer (rising edge).

#### • Block Diagram



# Register List

<ul> <li>Control Status Address</li> </ul>	s Regi <sub>bit</sub>	ster (AD	OCS)							Initial value Access
		15	14	13	12	11	10	9	8	
00003Ан		BUSY	INT	INTE	PAUS	STS1	STS0	STRT	—	0000000 <sub>в</sub> R/W
	bit	7	6	5	4	3	2	1	0	
00003Вн		MD1	MD0	ANS2	ANS1	ANS0	ANE2	ANE1	ANE0	0000000 <sub>в</sub> R/W
• Data Register Address 000038⊦	· (ADC bit	2R) 15 	14	13	12	11	10	9	8	Initial value Access XX₅ R
000039н	bit	7	6	5	4	3	2	1	0	XXXXXXXXB R

### 15. UART

UART is the serial I/O port for carrying out asynchronous (start-stop synchronization) or CLK synchronous communication.

- Characteristics of UART
- FDX double buffer
- Asynchronous (start-stop synchronization) and CLK synchronous communication are possible.
- Supports multi processor mode
- Dedicated baud rate generator is built-in.
- Free baud rate can be set using an external clock.
- Error detection function (parity, framing, overrun)
- Transfer signal is NRZ code
- Initiation of DMA transfer is possible by interruption.

• Block Diagram



# Register List

Address	bit	7	6	5	4	3	2	1	0	Initial value	Access
000023н		MD1	MD0	CS2	CS1	CS0		SCKE	SOE	00000 - 00в	R/W
Serial Con	trol Re	gister (	SCR)								
	bit	15	14	13	12	11	10	9	8	Initial value	Access
000022н		PEN	Р	SBL	CL	A/D	REC	RXE	TXE	00000100в	R/W
Serial Inpu	it Data	Registe	er/Serial	Output	Data Re	egister (	SIDR/S	ODR)			
	bit	7	6	5	4	3	2	1	0	Initial value	Access
000021н		D7	D6	D5	D4	D3	D2	D1	D0	XXXXXXXXB	R/W
Serial Stat	us Reg	gister (S	SR)								
	bit	15	14	13	12	11	10	9	8	Initial value	Access
000020н		PE	ORE	FRE	RDRF	TDRE	_	RIE	TIE	00001 - 00в	R/W
Communio	cation F	Pre-scal	ar Cont	rol Regi	ster (CD	OCR)					
	bit	7	6	5	4	3	2	1	0	Initial value	Access
000025н		MD		_	DIV4	DIV3	DIV2	DIV1	DIV0	0 11111в	R/W

### 16. DMA Controller (DMAC)

The DMA controller is the module to realize Direct Memory Access (DMA) transfers with FR 30 series devices. DMA transfers controlled by this module enable quick and direct transfer of all data without using the CPU and thus system performance is increased.

#### • Hardware Configuration of DMA Controller

This module is mainly configured of the following items.

- Internal I/O access control circuit
- 32-bit address counters (possible reload specification : 10)
- 16-bit transfer number counters (possible reload specification : 5)
- External transfer request input pin : DREQ0, DREQ1, DREQ2
- External transfer request reception output pin : DACK0, DACK1, DACK2 (external bus synchronization)
- External transfer termination output pin : DEOP0, DEOP1, DEOP2 (external bus synchronization)

#### • Major Function of DMA Controller

There are the following functions for data transfer using this module.

- Independent data transfer of a number of channels is possible (5 ch)
- Priority ranking amongst channels
   Fixed ranking (ch.0 > ch.1 > ch.2 > ch.3 > ch.4)
   Ranking between channel 0 and 1 can be reversed.
- Transfer request

Dedicated external pin input (Edge detection / level detection selection are possible for channels 0 to 2 only.) Built-in peripheral request (interruption requests are shared. External interruption is included.) Software request (register writing)

- Transfer sequence Consecutive / burst transfer
   Step transfer / block transfer (Maximum 16 words are settable.)
- Addressing mode : 32-bit full address specification (increase / decrease / fix)
- Data types : Byte, half word, word length
- Single shot or reload can be selected.



# Register List

Address bit	31	0	Initial value	Access
000200н	ch.0 Control/status register	DMACS0	0-00-000000000 <sub>B</sub> XX-00000XX-Х <sub>в</sub>	R/W
000204н	ch.0 Addressing/transfer counting register	DMACC0	XXXX XXXX-XXXB XXXXXXXX XXXXXXXB	R/W
<b>000208</b> H	ch.0 Transfer originator address register	DMASA0	XXXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXXX	R/W
00020Cн	ch.0 Destination address register	DMADA0	XXXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXXXX	R/W
<b>000210</b> н	ch.1 Control/status register	DMACS1	0-00-000000000 XX-00000XX-Хв	R/W
000214 <sub>H</sub>	ch.1 Addressing/transfer counting register	DMACC1	XXXX XXXX-XXXB XXXXXXXX XXXXXXXB	R/W
000218 <sub>H</sub>	ch.1 Transfer originator address register	DMASA1	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXXB	R/W
00021Cн	ch.1 Destination address register	DMADA1	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXXB	R/W
000220н	ch.2 Control/status register	DMACS2	0-00-000000000 XX-00000XX-Хв	R/W
000224 <sub>H</sub>	ch.2 Addressing/transfer counting register	DMACC2	XXXX XXXX-XXXB XXXXXXXX XXXXXXXAB	R/W
000228н	ch.2 Transfer originator address register	DMASA2	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXXB	R/W
00022Cн	ch.2 Destination address register	DMADA2	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXXB	R/W
000230н	ch.3 Control/status register	DMACS3	0-00-000000000 XX-00000XX-Х <sub>в</sub>	R/W
000234н	ch.3 Addressing/transfer counting register	DMACC3	XXXX XXXX-XXXB XXXXXXXXX XXXXXXXB	R/W
000238н	ch.3 Transfer originator address register	DMASA3	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXXB	R/W
00023Cн	ch.3 Destination address register	DMADA3	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXXB	R/W
000240н	ch.4 Control/status register	DMACS4	0-00-000000000 XX-00000XX-Хв	R/W
000244 <sub>H</sub>	ch.4 Addressing/transfer counting register	DMACC4	XXXX XXXX-XXXB XXXXXXXX XXXXXXXB	R/W
000248 <sub>H</sub>	ch.4 Transfer originator address register	DMASA4	XXXXXXXXX XXXXXXXXB XXXXXXXXX XXXXXXXAB	R/W
00024Cн	ch.4 Destination address register	DMADA4	XXXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXXXX	R/W
000250н	Overall control register	DMACR	о 0в О 0Ов	R/W

\*: Shaded areas indicate where nothing exists.

### 17. Bit Search Module

Bit search module searches for 0, 1 or change points on data that has been written in the input register, and returns the detected bit position.

# Block Diagram



#### • Registers List

Address	31 0	Initial value	Access
0003F0н	Data register for 0 detection(BSD0)	$\begin{array}{c} XXXXXXXXX XXXXXXX_{B} \\ XXXXXXXX XXXXXXX_{B} \end{array}$	W
0003F4н	Data register for 1 detection(BSD1)	XXXXXXXXX XXXXXXXB XXXXXXXXX XXXXXXXB	R/W
0003F8н	Data Register for Change Point Detection(BSDC)	XXXXXXXXX XXXXXXXB XXXXXXXXX XXXXXXXB	W
0003FCн	Detection Results Register(BSRR)	XXXXXXXXX XXXXXXXB XXXXXXXXX XXXXXXXB	R

#### 18. I-RAM

This type has 16 KB of built-in I-RAM. Efficient processing becomes possible by pre-arranging interruption processing programs and such like in this area. Writing on I-RAM is possible via the data bus and is available as RAM for data.

#### Register List

IRMC	7	6	5	4	3	2	1	0	Initial value Access
Address : 0003EFH	_	—		_	_	—	—	IRMD	0 R/W

# ELECTRICAL CHARACTERISTICS

# 1. Absolute Maximum Ratings

(Vss = AVss = AVRL = 0 V)

Paramotor	Symbol Rating		ing	Unit	Pomarke	
Farameter	Symbol	Min	Мах	Unit		
Power veltage	Vcc5	Vcc3-0.3	Vss + 6.0	V	*1	
Fower voltage	Vcc3	Vss - 0.3	Vss + 3.6	V	*1	
Analog power voltage	AVcc	Vss - 0.3	Vss + 3.6	V	*2	
Standard analog voltage	AVRH, AVRL	Vss - 0.3	Vss + 3.6	V	*2	
Input voltage	Vı	Vss - 0.3	Vcc5 + 0.3	V		
Analog pin input voltage	VIA	Vss - 0.3	AVcc + 0.3	V		
Output voltage	Vo	Vss - 0.3	Vcc5 + 0.3	V		
Maximum "L" level output current	lol		10	mA	*3	
Average "L" level output current	OLAV		4	mA	*4	
Maximum total "L" level output current	ΣΙοι		100	mA		
Average "L" level total output current	ΣΙοιαν		50	mA	*5	
Maximum "H" level output current	Іон		-10	mA	*3	
Average "H" level output current	Іонач		-4	mA	*4	
Maximum total "H" level output current	ΣІон		-50	mA		
Average "H" level total output current	ΣΙοήαν		-20	mA	*5	
Electricity consumption	PD		650	mW		
Operating temperature	TA	0	+70	°C		
Storage temperature	Tstg	-55	+150	°C		

\*1 : Vcc3/Vcc5 must not be lower than Vss – 0.3 V.

\*2 : Care must be taken that AVcc, AVRH and AVRL do not exceed Vcc + 0.3 V when the power is turned on. Also care must be taken that AVRH and AVRL do not exceed AVcc, and keep AVRH  $\geq$  AVRL.

\*3 : Peak value of the pin concerned is regulated as the maximum output current.

\*4 : Average current within 100 ms flowing in the pin concerned is regulated as the average output current.

\*5 : Average current within 100 ms flowing in all pins concerned is regulated as the average total output current.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(Vss = AVss = AVRL = 0 V)

Paramatar	Symbol	Value		Unit	Pomorko
Farameter	Symbol	Min	Max	Unit	Rellidiks
	Vcc5	4.5	5.5	.,	Keeping RAM status in the
Power voltage	Vcc3	3.135	3.465	V	case of normal operations / stopping
Analog power voltage	AVcc	Vss - 3.0	Vss + 3.465	V	
Standard analog voltage	AVRH	AVss	AVcc	V	
Operating temperature	TA	0	+70	°C	

# 2. Recommended Operating Conditions

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

$(V_{CC}5 = 5 V \pm 10\%, V_{CC}3 = 3.3 V \pm 5\%, V_{SS} = AV_{SS} = AV_{RL} = 0 V, T_A = 0 °C to +70 °C)$										
Parameter	Sym	Bin nama	Conditions		Value		Unit	Bomarka		
Falameter	bol	Pin name	Conditions	Min	Тур	Max	Unit	Remarks		
"H" level	Vін	Input excluding following		0.65 × Vcc3		Vcc5 + 0.3	V			
input voltage	VIHS	Refer to *		0.8 × Vcc3		Vcc5 + 0.3	V	Hysteresis input		
"L" level	Vı∟	Input excluding following		$V_{\text{SS}} - 0.3$		0.25 × Vcc3	V			
input voltage	Vils	Refer to *		Vss - 0.3		0.2 × Vcc3	V	Hysteresis input		
"H" level output voltage	Vон	_	Vcc5 = 4.5 V Іон = -4.0 mA	Vcc5 – 0.5			V			
"L" level output voltage	Vol		Vcc5 = 4.5 V lo <sub>L</sub> = 4.0 mA	—		0.4	V			
Input leak current (Hi-Z output leak current)	Ιu		Vcc5 = 5.5 V 0.45 V < Vi < Vcc5	-5	_	+5	μΑ			
Pull-up resistance value	Rpull	RST	$V_{CC}5 = 5.5 V$ $V_{I} = 0.45 V$	25	50	200	kΩ			
		Vcc5	fc = 12.5 MHz		50	70	mA	(4 times) in		
	Icc	Vcc3	Vcc5 = 5.5 V Vcc3 = 3.465 V		100	150	mA	case of 50 MHz operation		
<b>.</b> .		Vcc5	fc = 12.5 MHz		20	30	mA	In case of		
Power current	Iccs	Vcc3	Vcc5 = 5.5 V Vcc3 = 3.465 V		50	70	mA	sleeping		
		Vcc5	T <sub>A</sub> = 25 °C	—	10	20	μA	In case of		
	Іссн	Vcc3	Vcc5 = 5.5 V Vcc3 = 3.465 V		200	900	μΑ	stopping		
Input capacity	CIN	Other than Vcc, Avcc, Avss and Vss		—	10	_	pF			

\* : Hysteresis input pins : RST, HST, NMI, PE0/ATG, PE1/TRG0, 3, PE2/TRG1, 4, PE3/TRG2, 5, PF0/INT0 to PF7/INT7, PG0/DREQ0, PG3/DREQ1, PH0/DREQ2, PH3/SI, PH5/SCK, PH6/TI0, PI0/TI1, BGRNT/P81, WR1/P85, CS1/PA0 to CLK/PA6, RAS0/PB0 to DW1/PB7

### 4. AC Characteristics

### **Measurement Conditions**

The following conditions are applied to items without particular specifications.



# (1) Clock Timing

$(V_{cc}5 = 5 V \pm 10\%, V_{cc}3 = 3.3 V \pm 5\%, V_{ss} = AV_{ss} = AV_{RL} = 0 V, T_A = 0 °C to +70 °C)$											
Paramotor	Sym-	Pin	Conditions	Va	lue	Unit	Remarks				
Falailletei	bol	Name	Conditions	Min	Max	Unit					
Clock frequency (1)	fc	X0 X1		10.0	12.5	MHz	Self oscillation 12.5 MHz				
Clock cycle time	tc	X0 X1		80	100	ns	Internal 50 MHz operation (via PLL, 4 times)				
Clock frequency (2)	fc	X0 X1		10	25	MHz	Self oscillation (1/2 cycle input)				
Clock frequency (3)	fc	X0 X1		10	25	MHz	External clock (1/2 cycle input)				
Clock cycle time	tc	X0 X1		40	100	ns					
Input clock pulse width	Р <sub>WH</sub> Pw∟	X0 X1		10		ns	Clock is input to X0/X1				
	Рѡн	X0		25		ns	Clock is input to X0 only				
Input clock rising/falling time	tcr tcf	X0 X1			8	ns	(tcr + tcf)				
	fср			0.625*1	50		CPU system				
Internal operation	fсрв			0.625*1	25* <sup>2</sup>	MHz	Bus system				
clock frequency	fсрр			0.625*1	25		Peripheral system				
laternal en enstien	<b>t</b> CP			20	<b>1600</b> *1		CPU system				
Internal operation	tсрв			40*2	1600* <sup>1</sup>	ns	Bus system				
	<b>t</b> CPP			40	1600* <sup>1</sup>		Peripheral system				

\*1 : This is the value when 10 MHz, which is the minimum value of the clock frequency, is input to X0 and 1/2 cycle of the oscillation circuit and gearing of 1/8 are used.

\*2 : This is the value when doubler is used with a 50 MHz CPU.





#### (2) Clock Output Timing

$(V_{CC}5 = 5 V \pm 10\%, V_{CC}3 = 3.3 V \pm 5\%, V_{SS} = AV_{SS} = AV_{RL} = 0 V, T_A = 0 °C to +70 °C_{C}$												
Parameter	Sym-	Pin	Condi-	Va	lue	Unit	Pomarks					
	bol	Name	tions	Min	Max	Unit	Remarks					
Cycle time			CLK	tcp	—		*1					
	tcyc	CLK		2 × tcp		ns	In case of using doubler					
$CLK \uparrow \to CLK \downarrow$	<b>t</b> cHc∟	CLK		$1/2 \times t_{CYC} - 10$	$1/2 \times t_{CYC} + 10$	ns	*2					
$CLK \downarrow \rightarrow CLK \uparrow$	<b>t</b> CLCH	CLK		$1/2 \times t$ cyc $-10$	$1/2 \times t_{CYC} + 10$	ns	*3					



\*1 : torc is frequency of 1 clock cycle including the gear cycle.

\*2 : This standard value is in the case where the gear cycle is 1. If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.

- Minimum :  $(1 n / 2) \times t_{CYC} 10$
- Maximum : (1 n / 2) × tcyc + 10

Gear cycle of 1 should be taken when using a doubler.

- \*3 : This standard value is in the case where the gear cycle is 1. If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.
  - Minimum : n / 2 × tcyc 10
  - Maximum : n /  $2 \times t_{CYC} + 10$

Gear cycle of 1 should be taken when using a doubler.

The relationship between the CLK pin set using CHC/CCK1/CCK0 bit of the "Gear Control Register" (GCR) and original oscillation input is as follows. However, original oscillation input indicates "X0 input clock" in this figure.



# (3) Reset / Hardware Standby Input ( $V_{CC5} = 5 \text{ V} \pm 10\%$ . $V_{CC3} = 3.3 \text{ V} \pm 5\%$ , Vs

$(V_{cc}5 = 5 V \pm 10\%, V_{cc}3 = 3.3 V \pm 5\%, V_{ss} = AV_{ss} = AV_{RL} = 0 V, T_{A} = 0 °C to +70 °C)$											
Paramotor	Sym-	Pin	Conditions	Value		Value		Unit	Pomarke		
Falameter	bol Name		Conditions	Min	Max	Onit	itema ka				
Reset input time	<b>t</b> rstl	RST		$t_{\text{CP}}  imes 5$	_	ns					
Hardware standby input time	<b>t</b> HSTL	HST		$t_{\text{CP}}  imes 5$		ns					



~ /

#### (4) Power On Reset

$(V_{CCS} = 5 V \pm 10\%, V_{CCS} = 5.5 V \pm 5\%, V_{SS} = AV_{SS} = AV_{RL} = 0 V, T_{A} = 0 C (0 + 70 C)$												
Paramotor	Sym-	Pin	Conditions	Val	lue	Unit	Pomarks					
Tarameter	bol	Name	me	Min	Max	Unit	Renarks					
Power startup time	tĸ		Vcc5 = 5 V		30	ms	Vcc is less than					
		Vcc5	Vcc3 = 3.3 V		18		0.2 V before power is turned on.					
Power cut time	toff	Vcc3		1		ms	Repeated operation					

A 0 A 1

A) (D)


#### (5) Normal Bus Access Read/Write Operation ( $Vcc5 = 5 V \pm 10\%$ , $Vcc3 = 3.3 V \pm 5\%$ , Vss = AVss = AVRL = 0 V, $T_A = 0 \circ C$ to +70 $\circ C$ )

	(***	<u> </u>	$\pm 10/0, 0000 -$	$0.0 V \pm 0$	$10, v_{33} - Av_{33}$	= 7.01 $L = 0.0, 1$	. – U C	
Parameter		Sym-	Pin Name	Condi-	Va	lue	Unit	Romarks
Farameter		bol		tions	Min	Max	Unit	
CS0 to CS5 delay time	;	<b>t</b> CHCSL	CLK		—	15	ns	
CS0 to CS5 delay time	;	<b>t</b> chcsh	CS0 to CS5			15	ns	
Address delay time		<b>t</b> CHAV	CLK A23 to A00		_	15	ns	
Data delay time (write)		<b>t</b> CHDV	CLK D31 to D16		_	15	ns	
RD delay time		<b>t</b> CLRL	CLK			10	ns	
RD delay time		<b>t</b> CLRH	RD		_	10	ns	
WR0 to WR1 delay tim	ie	<b>t</b> CLWL	CLK		_	10	ns	
WR0 to WR1 delay tim	ie	<b>t</b> clwh	WR0 to WR1			10	ns	
Valid address $\rightarrow$ Valid data input time		<b>t</b> avdv	A23 to A00 D31 to D16			$3/2 \times t_{CYC} - 40$	ns	*1 *2
$\overline{RD} \downarrow \rightarrow$ Valid data input time	Pood	<b>t</b> rldv				tcyc – <b>25</b>	ns	*1
$\begin{array}{l} \text{Data setup} \rightarrow \\ \overline{\text{RD}} \uparrow \text{time} \end{array}$	iteau	<b>t</b> dsrh	RD D31 to D16		25		ns	
$\overline{RD} \uparrow \rightarrow$ Data holding time		<b>t</b> RHDX			0		ns	

\*1 : Time (tcvc × number of cycles extended) needs to be added to this standard if the bus is extended by automatic waiting insertion and RDY input.

\*2 : Values of this standard are in case of gear cycle × 1.
 If the gear cycle is set to 1/2, 1/4 or 1/8, calculations should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.

• Calculation formula :  $(2 - n / 2) \times t_{CYC} - 40$ 



### (6) Ready Input Timing

(Vcc	5 = 5 V ±	= 10%, Vcc3 =	$= 3.3 \text{ V} \pm 5\%$ , V	Vss = AVss =	= AVRL = 0 \	/, T <sub>A</sub> = 0	0 °C to +70 °C
Parameter	Sym-	Din Nama	Conditions	Value		Unit	Domorko
	bol		Conditions	Min	Max	Unit	Remarks
$\begin{array}{l} RDY \text{ setup time} \\ \rightarrow CLK \downarrow \end{array}$	<b>t</b> rdys	RDY CLK		20	_	ns	
$CLK \downarrow \rightarrow$ RDY holding time	<b>t</b> rdyh	RDY CLK		0		ns	



### (7) Holding timing

	(Vcc5 =	$= 5 \text{ V} \pm 10\%, \text{ Vc}$	$c3 = 3.3 V \pm$	5%, Vss = AV	ss = AVRL = (	) V, Ta	$= 0 \circ C$ to $+70 \circ C$
Paramotor	Sym-	Din Nama	Condi-	Val	ue	Unit	Pomarks
Falameter	bol	Fininame	tions	Min	Max	Unit	Remarks
BGRNT delay time	<b>t</b> CHBGL	CLK			10	ns	
BGRNT delay time	<b>t</b> снвдн	BGRNT			10	ns	
$\begin{array}{l} \text{Pin floating} \rightarrow \\ \overline{\text{BGRNT}} \downarrow \text{time} \end{array}$	<b>t</b> xhal	BGPNT	—	tcyc - 10	tcyc + 10	ns	
$\overline{BGRNT} \uparrow \rightarrow$ Pin valid time	<b>t</b> HAHV	BGRINI		tcyc – 10	tcyc + 10	ns	

Note : It takes at least one cycle from loading the BRQ to when  $\overline{\text{BGRNT}}$  is changed.



#### (8) Read/Write Cycle of the Normal DRAM Mode 5 X + 40 ~ X - 0 \_

$(V_{cc}5 = 5 V \pm 10\%, V_{cc}3 = 3.3 V \pm 5\%, V_{ss} = AV_{ss} = AV_{RL} = 0 V, T_A = 0 °C to +70 °C)$											
Paramotor	Sym-	Pin Name	Condi-	Va	lue	Unit	Pomarke				
Farameter	bol		tions	Min	Max	Unit	Neillai K5				
RAS delay time	<b>t</b> clrah	CLK			10	ns					
RAS delay time	<b>t</b> CHRAL	RAS			10	ns					
CAS delay time	<b>t</b> CLCASL	CLK			10	ns					
CAS delay time	<b>t</b> CLCASH	CAS			10	ns					
ROW address delay time	<b>t</b> CHRAV	CLK			15	ns					
COLUMN address delay time	<b>t</b> CHCAV	A23 to A00	3 to A00		15	ns					
DW delay time	<b>t</b> CHDWL	CLK			15	ns					
DW delay time	<b>t</b> CHDWH	DW			15	ns					
Output data delay time	tchdv1	CLK D31 to D16			15	ns					
$RAS \downarrow \rightarrow valid  data input time$	<b>t</b> rldv	RAS D31 to D16		_	5 / 2 × tcyc – 20	ns	*1 *2				
$CAS \downarrow \rightarrow valid data input time$	<b>t</b> CLDV	CAS			tcyc – 17	ns	*1				
$CAS \uparrow \rightarrow data holding time$	<b>t</b> CADH	D31 to D16		0		ns					

\*1 : If either the Q1 or A4 cycle is extended for one cycle, the toyc time needs to be added to this standard.

\*2 : Values of this standard are in case of gear cycle  $\times$  1.

If the gear cycle is set to 1/2, 1/4 or 1/8, calculation should be made using the following formula and replacing n with 1/2, 1/4 or 1/8.

• Calculation formula :  $(3 - n / 2) \times t_{CYC} - 20$ 



### (9) High Speed Page Read/Write Cycle of the Normal DRAM Mode

$(V_{cc}5 = 5 V \pm 10\%, V_{cc}3 = 3.3 V \pm 5\%, V_{ss} = AV_{ss} = AV_{RL} = 0 V, T_{A} = 0 °C to +70 °C)$											
Paramotor	Sym-	Pin Name	Condi-	Va	lue	Unit	Pomarke				
Faranielei	bol		tions	Min	Max	Unit	Remarks				
RAS delay time	<b>t</b> clrah	CLK, RAS		—	10	ns					
CAS delay time	<b>t</b> CLCASL	CLK			10	ns					
CAS delay time	<b>t</b> CLCASH	CAS			10	ns					
COLUMN address delay time	<b>t</b> CHCAV	CLK A23 to A00			15	ns					
DW delay time	<b>t</b> CHDWH	CLK, DW			15	ns					
Output data delay time	tchdv1	CLK D31 to D16			15	ns					
$CAS \downarrow \rightarrow valid  data input time$	<b>t</b> CLDV	CAS			tcvc - 17	ns	*				
CAS $\uparrow \rightarrow$ data holding time	<b>t</b> CADH	D31 to D16		0		ns					

\*: When Q4 cycle is extended for 1 cycle, add toyc time to this rating.



### (10) Single DRAM Timing

(***		- 10/0, 1000		,	,		
Paramotor	Sym-	Din Namo	Condi-	Va	lue	Unit	Remarks
Faidilietei	bol		tions	Min	Max		IVEIII al KS
RAS delay time	tclrah2	CLK		—	10	ns	
RAS delay time	tCHRAL2	RAS		_	10	ns	
CAS delay time	tchcasl2	CLK			n / 2 × tcyc + 8	ns	
CAS delay time	tchcash2	CAS		—	10	ns	
ROW address delay time	tCHRAV2	CLK		—	15	ns	
COLUMN address delay time	tchcav2	A23 to A00		—	15	ns	
DW delay time	tCHDWL2	CLK		—	15	ns	
DW delay time	tchdwh2	DW		—	15	ns	
Output data delay time	tchdv2	CLK D31 to D16			15	ns	
$CAS \downarrow \rightarrow valid  data  input  time$	tCLDV2	CAS			(1 – n / 2) × tcyc – 17	ns	
$CAS \uparrow \to data \text{ holding time}$	tCADH2	0010010		0		ns	



### (11) Hyper DRAM Timing

		· · · ·		<u> </u>			
Parameter	Sym-	Pin Name	Condi-	Va	lue	Unit	Remarks
i di dillotto i	bol		tions	Min	Max	0	Romanio
RAS delay time	tclrah3	CLK		—	10	ns	
RAS delay time	tchral3	RAS			10	ns	
CAS delay time	tchcasl3	CLK			n / 2 × tcyc + 8	ns	
CAS delay time	<b>t</b> снсаѕнз	040			10	ns	
ROW address delay time	tchrav3	CLK			15	ns	
COLUMN address delay time	<b>t</b> снсаvз	A23 to A00			15	ns	
RD delay time	tCHRL3	<b>0</b>			15	ns	
RD delay time	tснкнз				15	ns	
RD delay time	tclrl3				15	ns	
DW delay time	tchdwl3	CLK			15	ns	
DW delay time	tсноwнз	DW			15	ns	
Output data delay time	tchdv3	CLK D31 to D16		_	15	ns	
$CAS \downarrow \rightarrow valid  data input time$	tcldv3	CAS			tcvc - 20	ns	
$CAS \downarrow \rightarrow data holding time$	tcadh3	D31 to D16		0		ns	



#### (12) CBR Refresh

(V	cc5 = 5 V	$\pm$ 10%, Vcc3	$= 3.3 \text{ V} \pm 59$	%, Vss = AVss =	= AVRL $=$ 0 V,	$T_A = 0$ °	°C to +70 °C)
Parameter	Sym- bol	Pin Name	Condi- tions	Va	lue	Unit	Remarks
				Min	Мах		
RAS delay time	<b>t</b> clrah	CLK			10	ns	
RAS delay time	<b>t</b> CHRAL	RAS	-		10	ns	
CAS delay time	<b>t</b> CLCASL	CLK			10	ns	
CAS delay time	<b>t</b> clcash	CAS	-		10	ns	



### (13) Self Refresh

$(V_{cc}5 = 5 V \pm 10\%, V_{cc}3 = 3.3 V \pm 5\%, V_{ss} = AV_{ss} = AV_{RL} = 0 V, T_{A} = 0 °C to +70 °C)$											
Parameter	Sym- bol	Pin Name	Condi- tions	Va	lue	Unit	Remarks				
				Min	Max	Unit					
RAS delay time	<b>t</b> clrah	CLK			10	ns					
RAS delay time	<b>t</b> CHRAL	RAS			10	ns					
CAS delay time	<b>t</b> CLCASL	CLK		—	10	ns					
CAS delay time	<b>t</b> clcash	CAS			10	ns					



### (14) UART Timing

(V	/cc5 = 5 V =	± 10%, Vcc3	$= 3.3 \text{ V} \pm 5\%$ , Vs	s = AVss = A'	VRL = 0 V, -	$T_A = 0^{\circ}$	C to +70 °C)
Paramotor	Symbol	Din Namo	Conditions	Value		Unit	Pomarks
Farameter	Symbol		Conditions	Min	Max	Onit	Remarks
Serial clock cycle time	<b>t</b> scyc	—		8 tcycp	—	ns	
$SCLK \downarrow \to SOUT$ Delay time	<b>t</b> slov	_	Internal shift	-80	80	ns	
$Valid\;SIN\toSCLK\;\uparrow$	tıvsн	—	clock mode	100	—	ns	
$SCLK \uparrow \rightarrow Valid$ SIN holding lock	tsнıx			60		ns	
Serial clock "H" pulse width	ts∺s∟	—		4 tcycp	—	ns	
Serial clock "L" pulse width	<b>t</b> slsh	—		4 tcycp	—	ns	
$SCLK \downarrow \to SOUT$ Delay time	<b>t</b> slov		External shift clock mode		150	ns	
$Valid\;SIN\toSCLK\;\uparrow$	tıvsн	—		60	—	ns	
SCLK	tsнıx			60		ns	

Notes : • This is the AC standard in the case of CLK synchronous mode.

• tcycp is the cycle time of the peripheral system clock.



# (15) Trigger System Input Timing $(V_{CC}5 = 5 V + 10\%, V_{CC}3)$

$(Vcc5 = 5 V \pm 10\%, Vcc3 = 3.3 V \pm 5\%, Vss = AVss = AVRL = 0 V, T_A = 0 °C to +70 °C)$											
Parameter	Sym-	Pin Name	Condi- tions	Va	Unit	Pomarke					
Parameter	bol			Min	Max	Unit	itema ka				
A/D initiation trigger input time		ATG				ns					
PPG initiation trigger input time	<b>t</b> trg	TRG0 to TRG5	—	5 tcycp	_	ns					

Note :  $t_{\mbox{\scriptsize CYCP}}$  is the cycle time of the peripheral system clock.



### (16) DMA Controller Timing

	(Vc	$c5 = 5 V \pm 10\%$ , Vcc	$3 = 3.3 \text{ V} \pm 5$	5%, Vss = AVss	= AVRL $=$ 0 V,	$T_{\text{A}}=0$	°C to +70 °C)
Paramotor	Sym-	Din Namo	Condi-	Va	lue	Unit	Pomarke
Faianletei	bol	Fill Name	tions	Min	Max	Unit	Remarks
DREQ input pulse width	<b>t</b> drwh	DREQ0 to DREQ2		2 tcyc		ns	
DACK delay time	tCLDL	CLK			6	ns	
(Normal bus) (Normal DRAM)	<b>t</b> CLDH	DACK0 to DACK2			6	ns	
EOP delay time	<b>t</b> CLEL	СГК		_	6	ns	
(Normal bus) (Normal DRAM)	<b>t</b> cleh	DEOP0 to DEOP2	—	_	6	ns	
DACK delay time	<b>t</b> CHDL	CLK			$n / 2 \times t_{CYC}$	ns	
(Single DRAM) (Hyper DRAM)	(Single DRAM) (Hyper DRAM)	DACK0 to DACK2			6	ns	
EOP delay time	<b>t</b> CHEL	CLK			$n / 2 \times t_{CYC}$	ns	
(Single DRAM) (Hyper DRAM) tcнен		DEOP0 to DEOP2			6	ns	



### 5. A/D Converter Electrical Characteristics

(Vcc5 = 5 V ± 10%, Vcc3 = AVcc = AVRH = 3.3 V ± 5%, Vss = AVss = AVRL = 0 V, T<sub>A</sub> = 0 °C to +70 °C) Value Sym-Unit Parameter Pin Name bol Тур Min Max 10 10 BIT Resolution LSB Conversion error \_\_\_\_ ±3.0 \_\_\_\_ \_\_\_\_ \_\_\_\_ Linearity error ±2.5 LSB Differential linearity error LSB ±1.9 Zero transition error Vот -1.5 +2.5 LSB AN0 to AN7 +0.5Full-scale transition error VFST AN0 to AN7 AVRH - 4.5 AVRH - 1.5 AVRH + 0.5 LSB 5.6<sup>\*1</sup> Conversion time \_\_\_\_ \_\_\_\_ μs Analog port input current AIN AN0 to AN7 \_\_\_\_ 0.1 10 μΑ VAIN AN0 to AN7 AVss AVRH V Analog input voltage \_\_\_\_ V Standard voltage AVRH AVss **AVcc** \_\_\_\_ A 4 \_\_\_\_ mΑ \_\_\_\_ Power supply current AVcc AH 5\*<sup>2</sup> μΑ \_\_\_\_ IR 110 μΑ Standard voltage current supplied AVRH **I**RH 5\*<sup>2</sup> μΑ Tolerance between channels AN0 to AN7 4 LSB \_\_\_\_ \_\_\_\_

\*1 : In case of Vcc3 = AVcc = 3.3 V  $\pm$  5%, machine clock 25 MHz

\*2 : This is the current in the case that the A/D converter is not activated and the CPU is stopped (in case of Vcc3 = Avcc = AVRH = 3.465 V)

Notes : • As the AVRH becomes smaller, the tolerance becomes relatively larger.

• Output impedance of external circuits other than analog input must be used under the following condition.

Output impedance of external circuits  $< 7 \text{ k}\Omega$ 

If the output impedance of the external circuits is too high, the sampling time for the analog voltage may be insufficient.



#### **Definition of A/D Converter Terms**

Resolution

Analog changes that can be identified by A/D converter

- Linearity error
  Difference between the straight line linking the zero transition point (00 0000 0000 ←→ 00 0000 0001) to the full-scale transition point (11 1111 1110 ←→ 11 1111 1111) and actual conversion characteristics.
- Differential linearity error
  Difference compared to the ideal input voltage value required to change the output code 1LSB



### • Total error

This indicates the difference between the actual and theoretical values and includes zero transition, full-scale transition and linearity error.



### EXAMPLE CHARACTERISTICS









CODE

### ORDERING INFORMATION

Part number	Package	Remarks
MB91110PMT2	144-pin plastic LQFP (FPT-144P-M08)	
MB91V110CR	PGA-299C-A01	



# FUJITSU LIMITED

#### All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0204 © FUJITSU LIMITED Printed in Japan