FUJITSU SEMICONDUCTOR
MICROCONTROLLER

MB90M405

F^{2}MC-16LX FAMILY
16-BIT MICROCONTROLLERS
HARDWARE MANUAL ABSTRACTS

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Preface

■ Objective of Manual and Target Audience

The MB90M405 Series is a general-purpose semiconductor device in the F^2MC-16LX family. It is a 16-bit single-chip microcontroller ASIC (Application Specific IC). This manual explains the functions and operations of the MB90M405 Series for engineers who design products using this device.

How to Read This Manual

■ Page Organization

A summary is given below the title of each section. A title of the main section is noted in the sub-section to recognize a current-reading section.

■ Index Organization

(1) Register map index

The register map index format is similar to the I/O map and it allows search for the page explaining the bits of each register from the address, register abbreviation, register name, and resource macro name. Use the register map index at searching for the register function when designing a resource macro.

(2) Pin function index

The pin function index is similar to the explanation of the pin function and it allows serch for the block diagram of each resource macro, the explanation of the pin function, and notes from the package pin number, pin name, circuit type, and resource macro name. Use the pin function index when creating the system board, etc. (The pin function index will be provided in the next revision of this manual).

■ Organization of Notes and Checks

Notes : Reference information is given here. Use this as a hint or note when using the MB90M405. This also gives a section(s) to refer.

Check : Precautions when using the MB90M405 are given here. Specification restrictions, etc., are included.

1. GENERAL

This chapter explains the features and basic specifications of the Monolith (MB90M405).

The MB90M405 Series is a general-purpose 16-bit microcontroller developed for applications requiring fluorescent lamp panel control and contains 60 high-voltage withstand output pins required for a fluorescent lamp.
As with the original F^{2}MC-8L and F^{2}MC-16L families, the instruction system inherits the AT architecture, and has extended high-level language interface instructions and the extended addressing modes, enhanced multiplication/division instructions (signed), and enhanced bit processing. In addition, a 32-bit accumulator enables handle long word processing.

1.1 Features

- Clock:
  - PLL Clock multiplication circuit built-in
  - Operating clock (PLL clock) generated by dividing original oscillation by 2 or by multiplying original oscillation by 1 to 4 (2.1 MHz to 16.8 MHz at original oscillation of 4.2 MHz). Can be selected.
  - Minimum instruction execution time is 59.5 ns (when the original oscillation is 4.2 MHz, the PLL clock is generated by multiplying the original oscillation by 4, and Vcc = 3 V).
  - It is possible to generate an external output as a clock output by dividing the original oscillation by 16, 32, 64, or 128.
- Maximum memory space: 16 Mbytes
  - 24-bit addressing in memory space
- Instruction system suited for controller
  - Applicable data types (bit, byte, word, long-word)
  - Various addressing modes: 23 types
  - High code efficiency
  - High-precision operation with 32-bit accumulator
  - Signed multiplication and division instructions and enhanced **RETI** instruction
- Powerful instruction system applicable to high-level language (C) or multitasking
  - System stack pointer
  - Symmetric instruction set and barrel shift instruction
- Program patch function (2-address pointer)
- Shortened execution time: 4-byte instruction queue
- Powerful interrupt function (eight programmable priority levels)
  - Powerful interrupt function for 32 interrupt factors
- Data transfer function (extended intelligent I/O service function: 16 channels maximum)
- Low-power consumption (standby mode)
  - Sleep mode (stops CPU operating clock)
  - Pseudo-timer mode (stops everything except original oscillation and time-base timer)
  - Stop mode (stops original oscillation)
  - CPU Intermittent operation mode
- Package
  - QFP-100 (FPT-100P-M06: 0.65 mm pin pitch)
- Process
  - CMOS technology

1.2 Resources

- I/O port: 26 pins maximum (All 26 pins can also serve as resource pins).
- 18-bit time-base timer: 1 channel
- Watchdog timer: 1 channel
- 16-bit reload timer: 3 channels
- 16-bit free-run timer: 1 channel
- 16-bit output compare: 1 channel
- 16-bit input capture: 2 channels
  - When the count value of the 16-bit free-run timer matches the setting value of the output compare, the timer is cleared and an interrupt request is issued.
- Serial I/O: 2 channels
- UART: 2 channels
  - Clock-synchronous serial transfer (I/O extended serial) can be used.
  - The direction of the shift clock level can be selected arbitrarily (MSB or LSB).
- DTP/external interrupt (4 channels)
  - Start extended intelligent I/O services by an external input, and generate an external interrupt.
- Delayed interrupt generation module
  - A task-switching interrupt request is generated.
- 8-/10-bit A/D converter (16 channel)
  - 8- or 10-bit resolution can be selected.
- FL controller
  - Enables FL driver control. (The auto display control is performed for 32 digits max. and 59 segments max.)
    1 to 32 digits can be set (can be set on a digit-by-digit basis).
    The dimmer can be set.
  - Enables LED driver control (Auto display control is performed for 16 segments maximum).
    The auto display control can be performed for 16 segments max. at 1/2 duty.
- Timer clock divider
  - The original oscillation can be divided by 32, 64, 128, or 256.

1.3 Product Lineup

Table 1-1 lists the Monolith (MB90M405) series product lineup. Functions other than the ROM/RAM capacity are shared.

Table 1-1 MB90M405 Series Product Lineup

Product name	MB90MV405	MB90MF408	MB90M408	MB90M407
Classification	Evaluate	Flash Type ROM	Mass-produced product (mask ROM)	
ROM capacity	Not provided	128 Kbytes		96 Kbytes
RAM capacity	4 Kbytes	4 Kbytes		4 Kbytes
CPU Function	Count of basic instructions: 351 Minimum instruction execution time: 59.5 ns (at original oscillation of 4.2 MHz, with PLL clock generated by multiplying original oscillation by 4) Addressing types: 23 Program patch function: 2-address pointer Maximum memory space: 16 Mbytes			
Port	I/O port (CMOS) 26 pins (all of 26 pins also serve as resource pins)			
FL Controller	60 FL output pins can be used (Under LED control, 43 FL output pins and 17 LED control pins are required). Enables FL driver control and LED driver control can be performed. Under FL driver control, the dimmer can be set for both digits and segments.			
Serial I/O (UART)	Can also be used as the clock-synchronous method extended I/O serial. A dedicated baud rate generator is built-in. Four channels are built-in (two channels also serve as UART channels).			
16-bit reload timer	16-bit reload timer operation (Toggle output or one-shot output can be selected.) An event count function can be selected. Three channels are built-in.			
16-bit free-run timer	16-bit output compare x 1 channel (for clearing free-run timer) 16-bit input capture x 2 channels			
8-/10-bit A/D converter	8-/10-bit resolution x 16 channels (input multiplex) Minimum conversion time: 6.2 µs (at internal operation of 16 MHz)			
Timer clock divider	The external input clock can be divided and output to the outside. Clock division rates: 16, 32, 64, or 128 (programmable)			
External interrupt	Four independent channels (also serve for A/D input) Interrupt factor: L → H edge, H → L edge, L level, or H level			
Low power consumption mode	Sleep mode, stop mode, CPU intermittent mode, or pseudo-timer mode			
Process	CMOS			
Package	PGA256	QFP-100 (0.65 mm pitch)		
Operating voltage	3.3 V ±0.3 V(16.8 MHz: 4.2 MHz multiplied by 4)			

1.4 Block Diagram

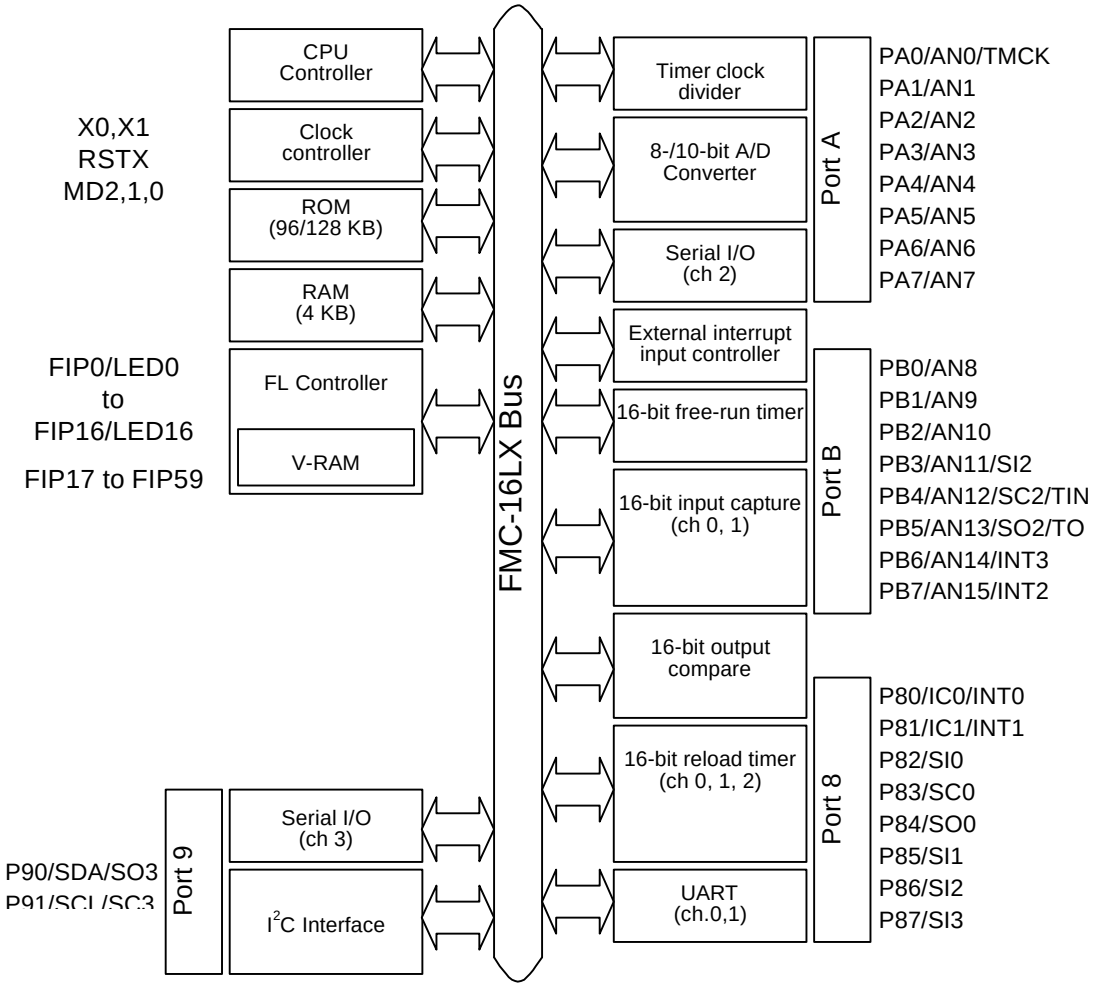
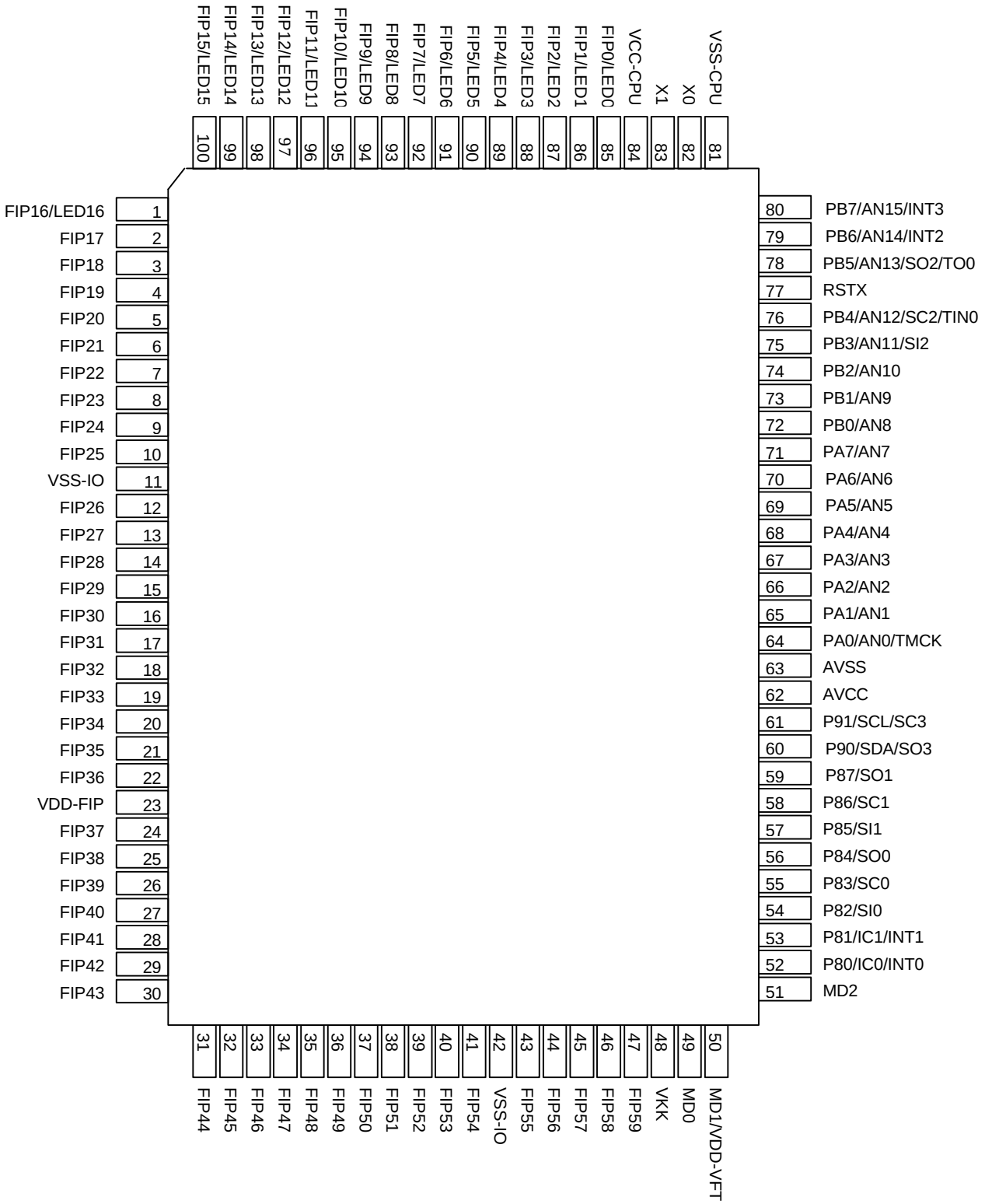


Fig. 1.1 Block Diagram (MB90M405)

1.5 Pin Assignment

FPT-100P-M06 Pin Assignment



1.6 Pin Description

Tables 1-2, 1-3 and ***1-4*** list the pin name, function, circuit type, and reset-time state/function.

Table 1-2 Pin Description

Pin No. QFP-100M06	Pin Name	Circuit Type	State/function at reset	Function
82, 83	X0, X1	A	Oscillation state	Oscillation input pins.
77	RSTX	B	Reset input	External reset input pin
85 to 100	FIP0 to FIP15	C	VKK Pull-down output	This function is selected when the FL driver is enabled.
	LED0 to LED15			This function is selected when the LED driver is enabled.
1	FIP16			This function is selected when the FL driver is enabled.
	LED16			This function is selected when the LED driver is enabled.
2 to 10 12 to 19	FIP17 to FIP33			Dedicated pins for the FL driver output.
20 to 22 24 to 41 43 to 47	FIP34 to FIP59	D		
52	P80		Hi-Z	General-purpose I/O port
	IC0			External trigger input pin for input capture 0
	INT0			External factor input pin for external interrupt input 0 This pin is only accepted when it is enabled by the EN0 bit.
53	P81			General-purpose I/O port
	IC1			External trigger input pin for input capture 1
	INT1			External factor input pin for external interrupt input 1 This pin is only accepted when it is enabled by the EN1 bit.
54	P82			General-purpose I/O port
	SI0			Serial data input pin for serial I/O channel 0 This pin is always effective when channel 0 is under input operation.
55	P83			General-purpose I/O port
	SC0			Serial clock I/O pin for serial I/O channel 0 This pin is effective when the channel-0 clock output is enabled.
56	P84			General-purpose I/O port
	SO0			Serial data output pin for serial I/O channel 0 This pin is effective when the channel-0 serial data output is enabled.
57	P85			General-purpose I/O port
	SI1			Serial data input pin for serial I/O channel 1 This pin is always effective when channel 0 is under input operation.
58	P86			General-purpose I/O port
	SC1			Serial clock I/O pin for serial I/O channel 1 This pin is effective when the channel-0 clock output is enabled.
59	P87			This pin is a general-purpose I/O port.
	SO1			Serial data output pin for serial I/O channel 1 This pin is effective when the channel-0 serial data output is enabled.
60	P90	G		General-purpose I/O port (However, the N ch is open drain.)
	SDA			Data I/O pin for the I²C interface. This function is effective when operation of the I²C interface is enabled. Also, set the port output to the Hi-Z state when operating the I²C interface.
	SO3			Serial data output pin for serial I/O channel 3 This pin is effective when the channel-3 serial data output is enabled.

Table 1-3 Pin Description

Pin No. QFP-100M06	Pin Name	Circuit Type	State/function at reset	Function
61	P91	G	Hi-Z	General-purpose I/O port (However, the N ch is open drain.)
	SCL			Clock I/O pin for the I^2C interface This function is effective when operation of the I^2C interface is enabled. Also, set the port output to the Hi-Z state when operating the I^2C interface.
	SC3			Serial clock I/O pin for serial I/O channel 3 This pin is effective when the channel-3 clock output is enabled.
64	PA0	F	Analog input	General-purpose I/O port
	AN0			Analog input pin 0 for the A/D converter This function is effective when the analog input specification is enabled (using ADER).
	TMCK			Timer clock output pin This pin is only effective when output is enabled. This pin is null when analog input is enabled using ADER.
65 to 74	PA1 to PB2			General-purpose I/O port
	AN1 to AN10			Analog input pins (1 to 10) for the A/D converter This function is effective when the analog input specification is enabled (using ADER).
75	PB3			General-purpose I/O port
	AN11			Analog input pin (11) for the A/D converter This function is effective when the analog input specification is enabled (using ADER).
	SI2			Serial data input pin for serial I/O channel 2 This pin is always effective when channel 2 is under input operation.
76	PB4			General-purpose I/O port
	AN12			Analog input pin (12) for the A/D converter This function is effective when the analog input specification is enabled (using ADER).
	SC2			Serial clock I/O pin for serial I/O channel 2 This pin is effective when the channel-2 clock output is enabled.
	TIN0			External clock input pin for reload timer channel 0 This pin is enabled when the external clock input is effective (ADER takes precedence).
78	PB5			General-purpose I/O port
	AN13			Analog input pin (13) for the A/D converter This function is effective when the analog input specification is enabled (using ADER).
	SO2			Serial data output pin for serial I/O channel 2 This pin is effective when the channel-2 serial data output is enabled.
	TO0			External event output pin for reload timer channel 0 This pin is effective when the external event output is enabled (ADER takes precedence).
79, 80	PB6 and PB7			General-purpose I/O port
	AN14 and AN15			Analog input pins (14, 15) for the A/D converter This function is effective when the analog input specification is enabled (using ADER).
	INT2 and INT3			External factor input pins for external interrupt inputs 2 and 3 These pins are accepted only when they are enabled using the EN2 bit and the EN3 bit.
62	AVCC	H	Power input	Vcc power input pin for the analog macro
63	AVSS			Vss power input pin for the analog macro
48	VKK	—		Power pin on the pull-down side at high-voltage withstand output.

Table 1-4 Pin Description

Pin No. QFP-100M06	Pin Name	Circuit Type	State/function at reset	Function
49	MD0	B	Mode pin	Input pin for specifying the operating mode Connect this pin to Vcc. Also, always switch this pin to Vss at boot programming to flash memory.
50	MD1/VDD-VFT			Input pin for specifying the operating mode Connect this pin to Vcc. This pin also serves as the VDD-VFT pin.
51	MD2			Input pin for specifying the operating mode Connect this pin to Vss. Also, always switch this pin to Vcc at boot programming to flash memory.
11, 42	VSS-IO	—	Power input	Power (0 V: GND) input pins for I/O
23	VDD-FIP			Power (3 V: Vcc) input pin for the FIP
81	VSS-CPU			Power (0 V: GND) input pin for the controller
84	VCC-CPU			Power (3 V: Vcc) input pin for the controller

1.7 I/O Circuit Type

Tables ***1-5*** and ***1-6*** show the circuit type for each pin.

Table 1-5 I/O Circuits

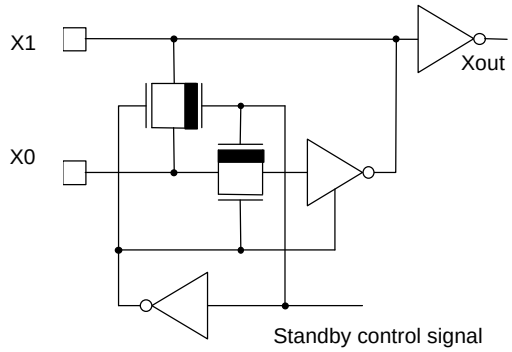
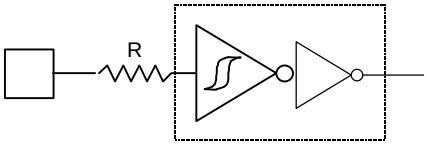
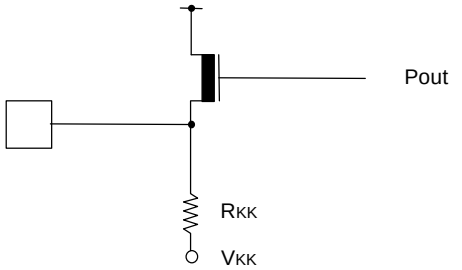
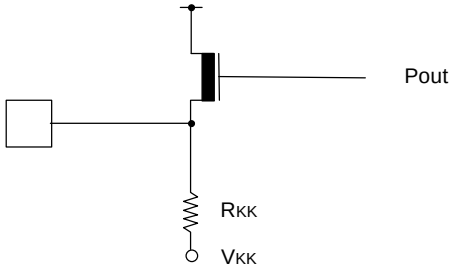
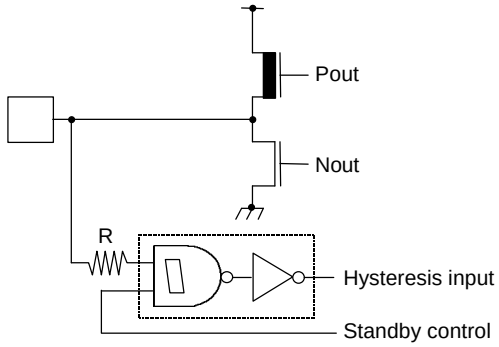
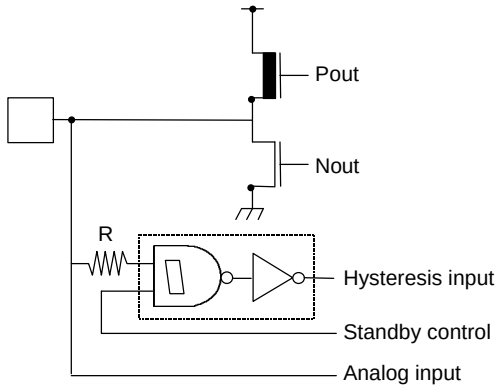
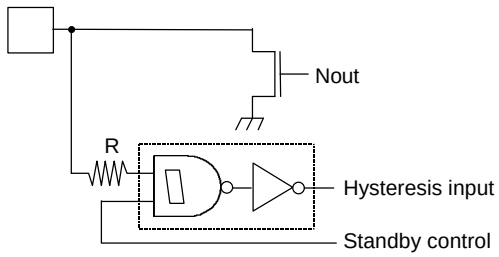
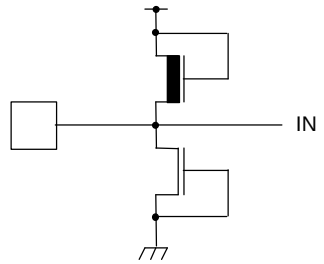
Classification	Circuit	Remarks
A		• Oscillator • Oscillation feedback resistor: about 1 MΩ
B		• Hysteresis input pin • Resistor value: about 50 kΩ (TYP)
C		• P-ch open-drain output - High-voltage withstand port output IOL = -25 mA When using the pin as a normal port, connect a diode clamp, etc., to prevent application of VKK voltage to the pin at output of the L level (see ***Handling notes***).
D		• P-ch open-drain output - High-voltage withstand port output IOL = -12 mA When using the pin as a normal port, connect a diode clamp, etc., to prevent application of VKK voltage to the pin at output of the L level (see ***Handling notes***).

Table 1-6 I/O Circuits

Classification	Circuit	Remarks
E		• CMOS hysteresis I/O pin • CMOS-level output • CMOS Hysteresis input (The input cutoff function is provided in the standby mode.) I_{OL} = 4 mA
F		• Analog/CMOS hysteresis I/O pin • CMOS-level output • CMOS hysteresis input (The input cutoff function is provided in the standby mode.) • Analog input (Analog input is effective when the corresponding bit of ADER is 1.) I_{OL} = 4 mA
G		• N-ch open drain output • CMOS Level hysteresis input (The input cutoff function is provided in the standby mode.) Unlike the CMOS I/O pin, there is no P-ch transistor at this pin. Consequently, even when an external voltage is applied to this pin with the power to the device set to OFF, no current flows to the device power (Vcc-IO/Vcc-CPU).
H		• Analog power input protector

1.8 Notes on Handling Devices

(1) Be careful not to exceed the maximum rated voltage (Prevention of latch up).

For a CMOS IC, latch-up may occur if a voltage higher than Vcc or a voltage lower than Vss is applied to the I/O pin other than medium-/high-voltage withstand I/O pins, or when a voltage that exceeds the rated voltage is applied between Vcc and Vss.

Latch up rapidly increases the power current, and the device may be destroyed by heat.

When using the device, take care not to exceed the maximum rating. Also, take care that the analog power (AVcc) and the analog input do not exceed the digital power (Vcc) when turning the AC/DC power on or off.

(2) Design the device so the supply voltage is as stable as possible.

A sudden change in the power voltage may cause a malfunction even within the operating assurance range of the VCC power supply voltage. For safety, the VCC ripple (p-p) of the commercial frequency (50/60 MHz) must be 10% or less of the standard VCC value, and the transient fluctuation at instantaneous power switching must be 0.1 V/ms or less. Also, take countermeasures to power noise, etc.

(3) Notes at power-on

The voltage rise time at power-on must be 50 µs or more (0.2 to 2.7 V).

(4) Setting unused input pins

Leaving unused input pins open may cause a malfunction. Therefore, these pins must be set to the pull-up or pull-down state.

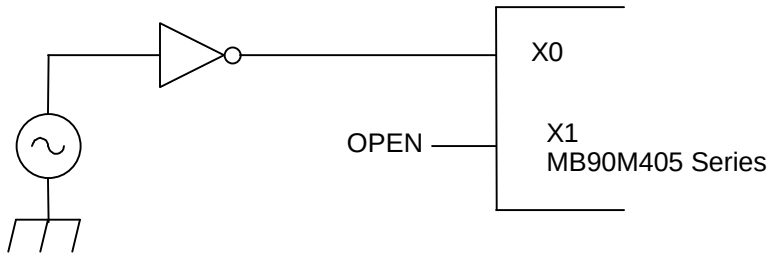
(5) Handling of power pins for A/D converter

Even when the A/D converter is not used, connect the pins so that the following relationships are established: $AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$.

(6) Notes on using external clock

Even when an external clock is used, the oscillation stabilization wait time is required at the power-on reset or the cancellation of the stop mode. In this case, drive the X0 pin only and leave the X1 pin open.

Example of using external clock



(7) Power pins

When two or more Vcc pins and Vss pins are provided, pins are designed to be at the same electric potential are internally connected to the device to prevent malfunctions such as latch-up. However, always connect all same electric potential pins to power and ground outside the device to prevent decrease of extraneous and radiation the malfunction of the strobe signal due to a ground level rise, and follow the standards on total output current, etc. Also, consider to connecting the pins to Vcc and Vss of this device at the lowest possible impedance from the current supply source (It is recommended to connect a bypass capacitor of about 0.1 μF of the device between Vcc and Vss).

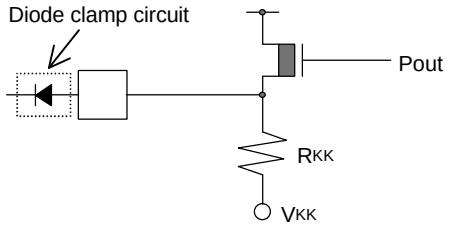
(8) Application sequence for power analog inputs for A/D converter

Apply the digital power (Vcc) first, and then apply the power (AVcc) and analog inputs (AN0 to AN15) for the A/D converter. Disconnect the power and analog inputs for the A/D converter first, and then disconnect the digital power (Vcc).

Also, do not allow the input voltage to exceed AVcc even when using a pin shared with an analog input as an input port (Simultaneous application and disconnection of analog power and digital power is allowed).

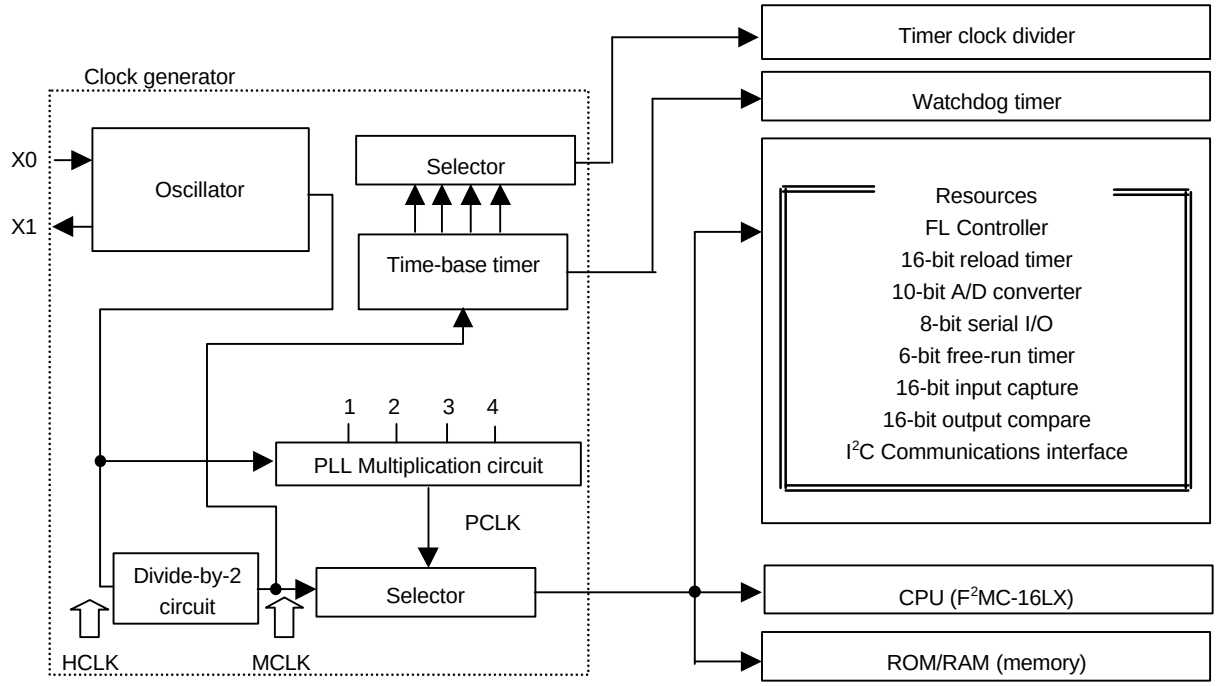
(9) Output of high-voltage withstand output pin (circuit type C or D)

When the high-voltage withstand output pin (circuit type is C or D) is used as an ordinary output port, the port outputs the VKK pin voltage pull-down value at the L level output. In this case, the VKK pin level voltage is applied to the external circuit, so it is recommended to add a diode clamp circuit as shown in the figure below.



1.9 Clock Supply Map

The clock supply map for this device (Monolith: MB90M405) is shown below.



HCLK: Oscillation clock

MCLK: Main clock (operating clock: clock generated by dividing oscillation clock by 2)

PCLK: PLL clock

1.10

This section provides an overview of the low power consumption mode.

The onolith (MB90M405) has the following modes that stop various functions and clocks ***Chapter 4***.

• Relationships between operating modes and power

Operating mode	Main clock	PLL Clock	CPU	Resources	Timer clock
PLL Run	Operates	Operates	Operates	Operates	Operates
Main Run	Operates	Stops	Operates	Operates	Operates
PLL Sleep	Operates	Operates	Stops	Operates*	Operates
Main sleep	Operates	Stops	Stops	Operates*	Operates
Pseudo-time	Operates	Stops	Stops	Stops	Operates
Stop	Stops	Stops	Stops	Stops	Stops

In the above table, the power consumption decreases as the operating mode goes down from the top of the table.

In the PLL Run mode, operation is performed on the PCLK generated by multiplying the original oscillation by 1 to 4. In the Main Run mode, operation is performed on the MCLK generated by dividing the original oscillation by 2.

*: In the sleep mode, the CPU stops, so resources cannot be accessed from the CPU.

May 19, 2000

Preliminary Version 1

Data sheet

MB90M405 Series

Electric Specification Table

■ Electrical Characteristics

1. Absolute Maximum Rating

($V_{SS-CPU} = V_{SS-IO} = AVss = 0.0$ V)

Parameter	Symbol	Rated Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC-CPU}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	Power supply pin for control circuit
	V_{DD-FIP}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	Power supply pin for FIP
	AV_{CC}	$V_{SS} - 0.3$	$V_{SS} + 4.0$	V	$Vcc \geq AVcc$ *1
	V_{KK}	$V_{CC} - 45$	$V_{CC} + 0.3$	V	Pull-down side power supply pin for high voltage resistance output.
Input voltage	V_I	Vss – 0.3	Vss + 4.0	V	*2
	$•_{I2}$	Vss – 0.3	Vss + 5.5	V	*3
Output voltage	V_O	Vss – 0.3	Vss + 4.0	V	*2
	V_{O2}	Vss – 0.3	Vss + 5.5	V	*•(Open drain output)
"L" level max. output current	I_{OL}	—	15	mA	*4, *5
"L" level avg. output current	I_{OLAV}	—	4	mA	Average value (Operating current × Operating rate) *5
"L" level max. overall output current	ΣI_{OL}	—	100	mA	*5
"L" level avg. overall output current	ΣI_{OLAV}	—	50	mA	Average value (Operating current × Operating rate) *5
"H" level max. output current	I_{OH}	—	–15	mA	*4, *5
	I_{OHFIP1}	—	–27	mA	FIP00 to FIP33 pins
	I_{OHFIP2}	—	–14	mA	FIP34 to FIP59 pIns
"H" level avg. output current	I_{OHAV}	—	–4	mA	Average value (Operating current × Operating rate) *5
"H" level max. overall output current	ΣI_{OH}	—	–100	mA	*5
"H" level avg. overall output current	ΣI_{OHAV}	—	–50	mA	Average value (Operating current × Operating rate) *5
	$\Sigma I_{OHFIPAV}$	—	–180	mA	Average value (Operating current × Operating rate) *6
Power consumption	P_{D_CPU}	—	300	mW	For CPU_Chip individual operation
	P_{D_FL}	—	1176	mW	For FL_Chip individual output operation
Operating temperature	T_A	–40	+85	°C	
Storage temperature	T_{STG}	–55	+150	°C	

*1: AV_{CC} should not exceed V_{CC} when turning on the power supply.

*2: V_I and V_O should not exceed V_{CC} + 0.3 V.

*3: The 5 V withstandable voltage pin for I^2C. Applies to P90/SDA, P91/SCL only.

*4: The maximum output current is standard at the peak value of the corresponding 1 pin.

*5: Excludes currents on the FIP00 to FIP59 pins.

*6: FIP00 to FIP59 pins are targeted.

Cautions:

1. The V_{CC} specification in the table means: $V_{DD\text{-}FIP}$ = $V_{DD\text{-}VFT}$ = $V_{CC\text{-}CPU}$. Use with the same power supply level as the three pins described above. Also, V_{SS} means: $V_{SS\text{-}IO}$ = $V_{SS–CPU}$. Connect this pin to the GND.

2. This device contains circuity to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltage to this high impedance circuit.

2. Recommended Conditions

(V_{SS-IO} = V_{SS-CPU} = AVss = 0.0 V)

Parameter	Symbol	Rated value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC-CPU}	3.0	3.6	V	Under normal operation
	V_{DD-FIP}	3.0	3.6	V	Under normal operation
	Vcc	2.5	3.6	V	Maintains status of stop operation
"H" level input voltage	V_{IHS}	0.8 Vcc	Vcc + 0.3	V	CMOS Hysterisis input pins other than I^2C
	V_{IHS2}	0.8 Vcc	5.8	V	CMOS Hysterisis input pins of I^2C (5 V withstandable voltage)*1
	V_{IHM}	Vcc – 0.3	Vcc + 0.3	V	MD pin input
"L" level input voltage	V_{ILS}	Vss – 0.3	0.2 Vcc	V	CMOS Hysterisis input pins other than I^2C
	V_{ILS2}	Vss – 0.3	0.2 Vcc	V	CMOS Hysterisis input pins of I^2C (5 V withstandable voltage)*1
	V_{ILM}	Vss – 0.3	Vss + 0.3	V	MD pin input
Operation temperature	T_A	–40	+85	°C	

*1: On the 1st ES product of MB90MF408, the withstandable voltage is 3 V (can be used up to 4.5 V at the test lab level).

Caution: The V_{CC} specification in the table means: V_{DD-FIP} = V_{DD-VFT} = V_{CC-CPU}. Use with the same power supply level as the three pins described above. Also, V_{SS} means: V_{SS-IO} = V_{SS-CPU}. Connect this pin to the GND.

3. DC Specifications

(T_A = –40° to 85°C, $V_{DD-FIP} = V_{DD-VFT} = V_{CC-CPU} = AV_{CC}$ = 3.0 to 3.6 V, $V_{SS-IO} = V_{SS-CPU} = AV_{SS}$ = 0 V)

Parameter	Symbol	Pin	Test Condition	Rated value			Unit	Remarks
				Min.	Typ.	Max.		
Output H voltage	V_{OH5}	FIP00 to FIP33	V_{CC} = 3.3 V I_{OH5} = –23 mA	Vcc – 2.5	—	—	V	
	V_{OH4}		V_{CC} = 3.3 V I_{OH4} = –12 mA	Vcc – 1.3	—	—	V	
	V_{OH3}	FIP34 to FIP59	V_{CC} = 3.3 V I_{OH3} = –12 mA	Vccv – 2.0	—	—	V	
	V_{OH2}		V_{CC} = 3.3 V I_{OH2} = –5 mA	Vcc – 1.0	—	—	V	
	V_{OH1}	SDA/SCL	I_{OH1} = –4 mA	—	—	5.5	V	Open drain pin *2
	V_{OH0}	All output pins other than the above	I_{OH} = –2.0 mA	Vcc – 0.5	Vcc– 0.3	—	V	
Output L voltage	V_{OL1}	SDA/SCL	I_{OL} = 15 mA	—	0.5	0.8	V	
	V_{OL}	All output pins other than the above	I_{OL} = 2.0 mA	—	0.2	0.4	V	
Input leak current	I_{IL}	Input pins other than FIP00-59	V_{CC} = 3.0 V (V_S.<V_I<V_{CC})	–5	–1	5	µA	
Output leak current	I_{LO3}	FIP00 to FIP33	V_{CC} = 3.3 V (V_{CC} – 43<V_I<V_{CC})	—	—	20	µA	
	I_{LO2}	FIP34 to FIP59	V_{CC} = 3.3 V (V_{CC}– 43<V_I< V_{CC})	—	—	10	µA	
Power supply current	I_{CC}	Vcc	Vcc = 3.3 V, and internal operation at 16 MHz, and normal operation	—	32	40	mA	MB90M407/8 (argeted standard values)*1
			Vcc = 3.3 V, and internal operation at 16 MHz, and A/D operation	—	37	45	mA	MB90M407/8 (targeted standard values)*1
			Vcc = 3.3 V, and internal operation at 16 MHz, and normal operation	—	40	50	mA	MB90MF408 MB90MV405 (F targeted standard values)*1
			Vcc = 3.3 V, and internal operation at 16 MHz, and A/D operation	—	45	55	mA	MB90MF408 MB90MV405 (F targeted standard values)*1
			Flash programming/erasing	—	40	50	mA	MB90MF408
	I_{CCS}		Vcc = 3.3 V, and internal operation at 16 MHz, and sleep operation	—	15	20	mA	*1

(Continue)

(Continued)

Parameter	Symbol	Pin	Test Condition	Rated value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current	I_{CCH}		T_A = +25°C, and operation stopped	—	15	20	μA	(Targeted standard values)
Pull-up resistor	R_{UP}	RSTX	—	20	65	200	kΩ	
Pull-down resistor	R_{DW1}	MD2	—	20	65	200	kΩ	
	R_{DW1}	FIP00 to FIP59	When there are settings	80	120	160	kΩ	

*1: Current values that are specified do not include the consumption current on the high withstandable voltage pins. They indicate the consumption current internally on the circuit.

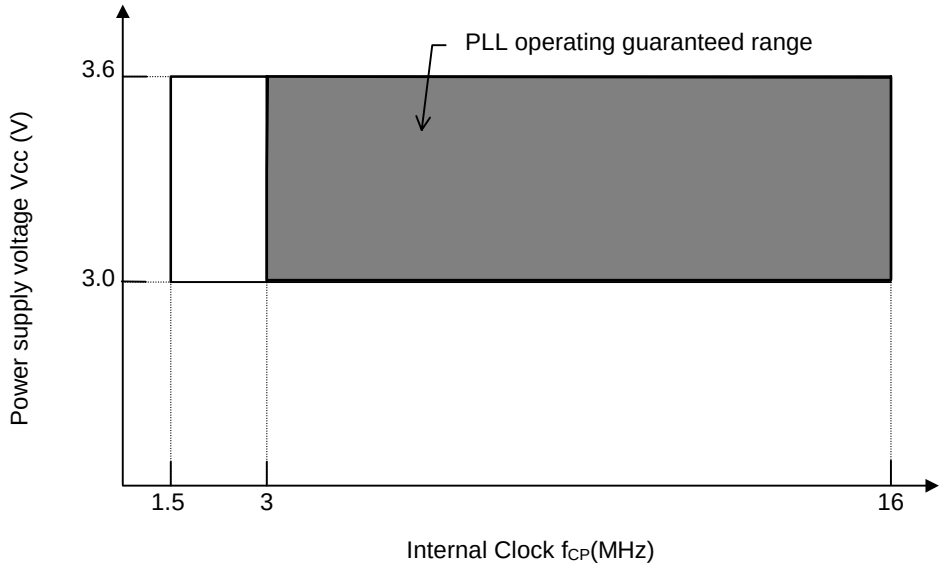
*2: On the 1st ES product of MB90MF408, the Max. standard value is 3.6 V (can be used up to 4.5 V at the test lab level).

Notes:

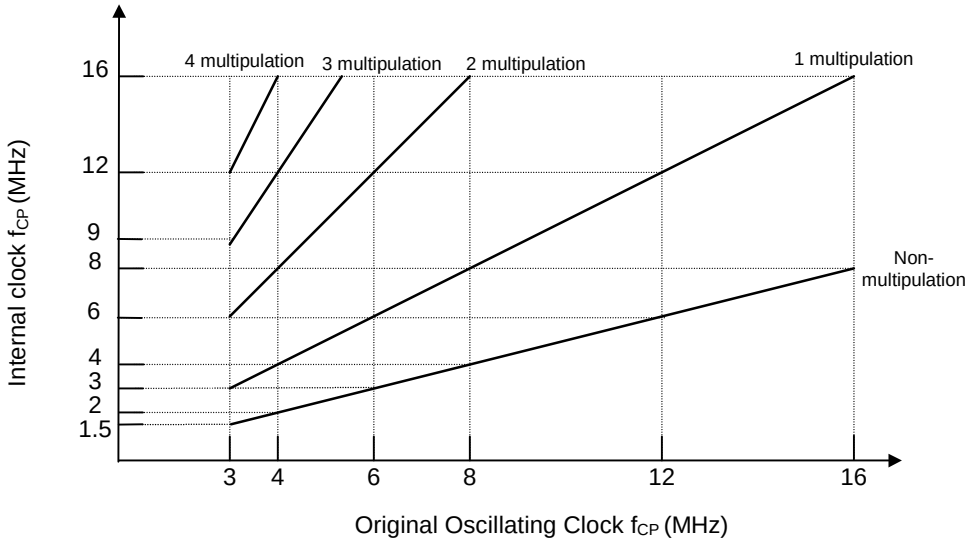
1. The V_{CC} specification in the table means: $V_{DD\text{-}FIP}$ = $V_{DD\text{-}VFT}$ = $V_{CC\text{-}CPU}$. Use with the same power supply level as the three pins described above. Also, V_{SS} means: $V_{SS\text{-}IO}$ = $V_{SS\ -\ CPU}$. Connect this pin to the GND.
2. There can be changes in the current value according to improvements in performance. The measuring condition of the power supply current is the external clock.

- PLL operating guaranteed range

Relationship between internal-operation clock frequency and power supply voltage



Relationship between original oscillation frequency and internal-operation clock frequency



4. A/D Conversion Unit Electrical Characteristics

(T_A = –40 to +85°C, $V_{CC-CPU} \leq$ AVcc = 3.0 V to 3.6 V, $V_{SS-CPU} = V_{SS-IO}$ = AVss = 0 V)

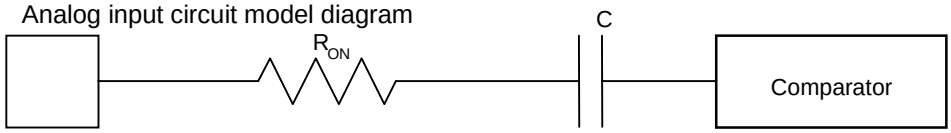
Parameter	Symbol	Pin	Rated value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	Can switch to 8 bits
Overall error	—	—	—	—	±3.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN15	Avss –1.5 LSB	A•ss +0.5 LSB	Avss +2.5 LSB	mV	1LSB= AVcc/1022
Full scale transition voltage	V_{FST}	AN0 to AN15	AVcc –3.5 LSB	AVcc –1.5 LSB	Avcc +0.5 LSB	mV	
Conversion time (Sampling + Compare)	—	—	98 t_{CP} *2	—	—	ns	16 MHz operation
Sampling time	—	—	32 t_{CP} *2	—	—	ns	16 MHz operation
Compare time	—	—	66 t_{CP} *2	—	—	ns	16 MHz operation
Analog port input current	I_{AIN}	AN0 to AN15	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN15	0	—	AVcc	V	
Reference voltage	—	AVcc	3.0	—	AVcc	V	
Power supply current	I_A	AVcc	—	—	5	mA	
	I_{AH}	AVcc	—	—	5	µA	*1
Reference voltage supply current	I_R	AVcc	—	100	200	µA	
	I_{RH}	AVcc	—	—	5	µA	*1
Channel differences	—	AN0 to AN15	—	—	4	LSB	

*1: When not operating A/D converter, this is the current ($V_{CC-CPU} = AV_{CC}$ = 3.3 V) when the CPU is stopped.

*2: t_{CP} means: 1/internal operating frequency. When the internal operating frequency is 16 MHz, t_{CP} is 1/16 MHz = 62.5 ns.

Notes:
1. The reference L value is fixed at AV_{SS}; the reference H value is fixed at AV_{CC}. The error is relatively large as the AV_{CC} becomes smaller.
2. Analog input external circuit output impedance should use the following conditions.
   External Circuit Output Impedance ≤ 10 kΩ
3. If the external circuit output impedance is too high, there maybe insufficient time for sampling of the analog voltage.

- Analog input circuit model diagram



Analog input

MB90M407/M408
R_{ON}= About 1.5 kΩ
C = About 30 pF
MB90MF408, MB90MV405
R_{ON} = About 3.0 kΩ
C = About 65 pF

Note: Numeric values herein should be used as a guide.

6. Handling Device

- **Preventing latch-up**

  Latch-up may occur in CMOSIC when a voltage higher than V_{CC-CPU} or lower than V_{SS-CPU} is applied to the input or output pins, or a voltage exceeding the rated value is applied between V_{CC-CPU} and V_{SS-CPU}. Latch-up may cause a rapid increase in the supply current, sometimes resulting in thermal damage to the device. Therefore, keep the used voltage within the maximum ratings.

  When turning the power on and off the analog supply voltage (AV_{CC}) analog input should not exceed the digital supply voltage (V_{CC-CPU}).

- **Voltage supplies should be stabilized.**

  A sudden change of the power supply voltage may cause a malfunction even within the guaranteed range of operation of the V_{CC-CPU} power supply voltage.

  For reference of stabilization, voltage variations are recommended to be restrained so that V_{CC-CPU} ripple variations (P-P values) are below 10% of the standard V_{CC-CPU} value in commercial frequencies (50 to 60 Hz), and so that transient variation is below 0.1 V/ms in sudden changes during power switchovers.

- **Precautions when turning on the power supply**

  Ensure a minimum of 50 μs (between 0.2 to 2.7 V) for voltage rise times when turning on the power supply to prevent malfunction of the built-in power reduction circuit.

- **Handling of unused input pins**

  Leaving unused input pins open may cause a malfunction. Therefore, these pins should be connected to a pull-up or a Pull-down resistor.

- **Handling of A/D converters power supply pins**

  Connect power supply pins with $AV_{CC} = V_{CC-CPU}$, $AV_{SS} = V_{CC-IO}$ even when not using the A/D converters.

- **Precautions when using the external clock**

  Oscillating stability waiting time is required when resetting from the Power On Reset, Stop Mode when using the external clock.

- **Order of turning on the power**

  Turn off the digital power supply (V_{CC-CPU}) after turning off the A/D converter power supplie ($AV_{CC,}$ AV_{SS}) and analog input (AN0 to AN15).

  Do not allow the input voltage to exceed AV_{CC} when using the analog input pins as an input port.