FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-28827-1E

ASSP For Screen Display Control

CMOS

On-Screen Display Controller

MB90098A

■ DESCRIPTION

The FUJITSU MB90098A on-screen display controller is designed for use with LCD monitors, operates at a maximum dot clock frequency of 140 MHz, and provides demultiplexed output (2-pixel parallel output) .

The maximum display screen configuration is 32 characters × 16 rows, with a maximum resolution of 24 × 32 dots per character making the MB90098A ideal for use with SVGA, XGA, SXGA etc. LCD displays.

A variety of display functions are enabled including sprite characters, background characters, graphics functions etc.

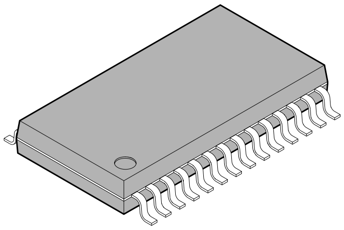
■ FEATURES

• Main screen display capacity	Maximum 32 characters × 16 rows
• Character configuration	L size : 24 dots (h) × 2h* dots (v) M size : 18 dots (h) × 2h* dots (v) S size : 12 dots (h) × 2h* dots (v) * : h = 9 to 16 L, M, S sizes can be selected by character h can be set to 2 values per screen
• Character type	512 character types built in

(Continued)

■ PACKAGE

28-pin plastic SOP



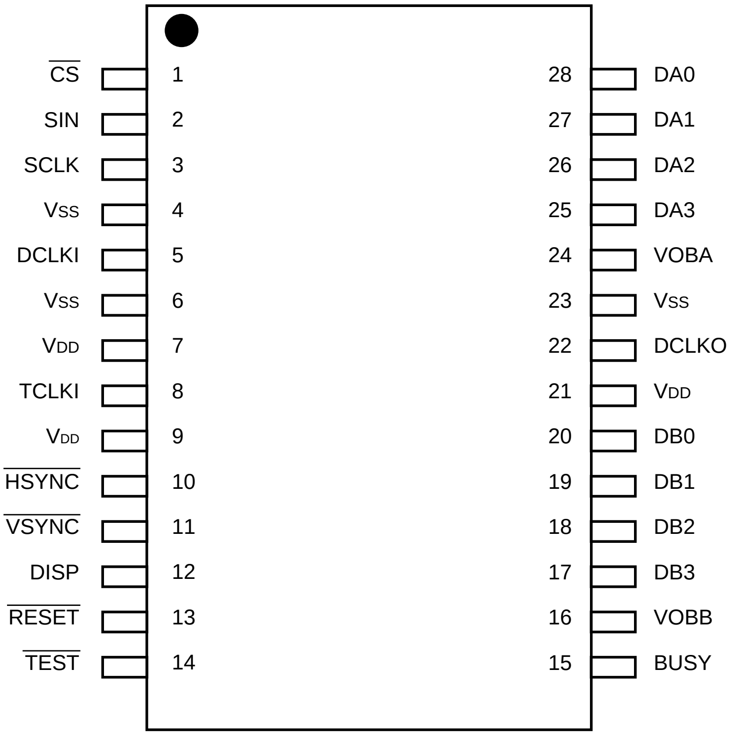
(FPT-28P-M17)

(Continued)

• Display modes	Normal/graphic characters	(set for each character)
	Border display (horizontal border /pattern background)	(set for each screen)
	Character background (solid-fill/shaded)	(set for each character)
	Row background (solid-fill/shaded)	(set for each row)
	Enlarged (standard, double height, double width, double height & width)	(set for each row)
	Blinking : Select blinking character, period, duty ratio	(set for each character) (set for each screen)
• Sprite character display (graphic display only)	Can display 1 block on main screen (Max. 2 characters wide × 2 high) . Only the first 256 characters can be used (code : 000_H to $0FF_H$)	
• Screen background character display (graphic display only)	Repeated pattern below main screen (Max. 2 characters wide × 2 high) . Only the first 256 characters can be used (code : 000_H to $0FF_H$)	
• Display color	Character color/background color	16 colors each (set for each character)
	Row background/character border color	16 colors each (set for each row)
	Screen background color	16 colors (set for each screen)
	Graphic character dot color	16 colors (set for each dot)
	Shadow background border color	16 colors (set for each screen)
• Display position control	Horizontal display start position	Control in 4-dot units (set for each screen)
	Vertical display start position	Control in 4-dot units (set for each screen)
	Row spacing control	Control in 2-dot units (set for each row)
• Character/color signal output	Choice of straight output or demultiplexed output DA3-DA0 (color signal) , VOBA (OSD display period output signal) DB3-DB0 (color signal) , VOBB (OSD display period output signal)	
• Clock frequency	140 MHz	
• Microcontroller interface	16-bit serial input (3 signal input pins)	
• Package	SOP-28	
• Supply voltage	+3.3 V	

■ PIN ASSIGNMENT

(TOP VIEW)

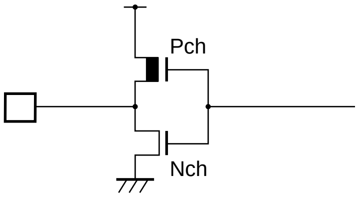
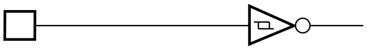
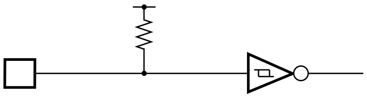

$\overline{\text{CS}}$ 1
SIN 2
SCLK 3
V_{SS} 4
DCLKI 5
V_{SS} 6
V_{DD} 7
TCLKI 8
V_{DD} 9
$\overline{\text{HSYNC}}$ 10
$\overline{\text{VSYNC}}$ 11
DISP 12
$\overline{\text{RESET}}$ 13
$\overline{\text{TEST}}$ 14
15 BUSY
16 VOBB
17 DB3
18 DB2
19 DB1
20 DB0
21 V_{DD}
22 DCLKO
23 V_{SS}
24 VOBA
25 DA3
26 DA2
27 DA1
28 DA0

(FPT-28P-M17)

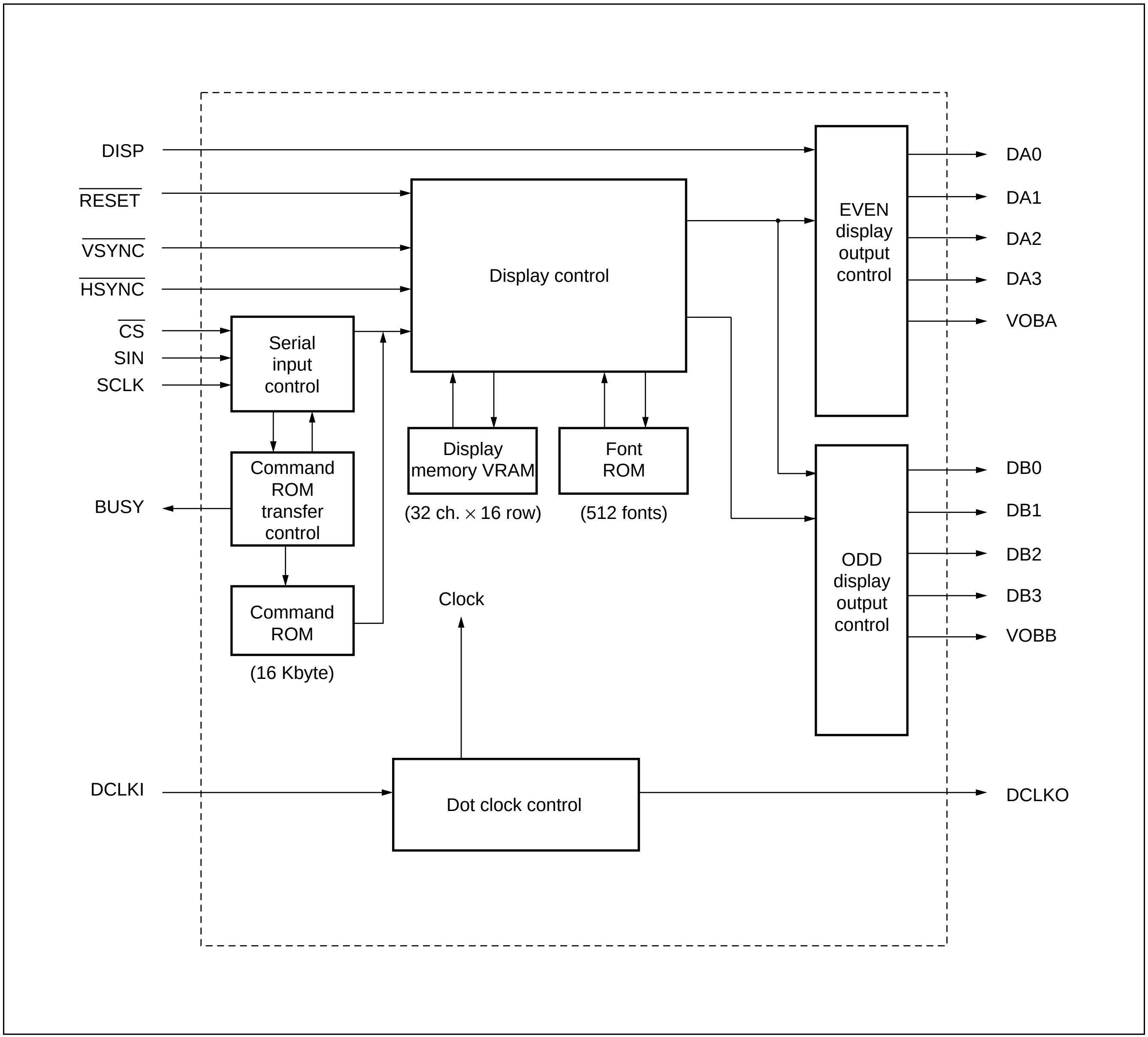
■ PIN DESCRIPTIONS

Pin	Pin no.	I/O	Circuit type	Description
DCLKI	5	Input	B	Dot clock input pin
DCLKO	22	Output	A	Dot clock output pin
$\overline{\text{HSYNC}}$	10	Input	B	Horizontal sync signal input pin. The active level is programmable.
$\overline{\text{VSYNC}}$	11	Input	B	Vertical sync signal input pin. The active level is programmable.
DISP	12	Input	B	Display output control signal input pin. Input a high level signal to enable display output. Input a low level signal to set the display output (DA3-0, VOBA, DB3-0, VOBB pin output) to inactive level. The active level is programmable.
DA3 DA2 DA1 DA0	25 26 27 28	Output	A	Color signal output pins. In straight output mode, the all-dot signal is output. In demultiplexed output mode, the even dot signal is output. The active level is programmable.
VOBA	24	Output	A	Display period signal output pin. In straight output mode, the all-dot display period signal is output. In demultiplexed output mode, the even dot display period signal is output. The active level is programmable.
DB3 DB2 DB1 DB0	17 18 19 20	Output	A	Color signal output pins. In demultiplexed output mode, the odd dot signal is output. In straight output mode, the output is fixed at inactive level. The active level is programmable.
VOBB	16	Output	A	Display period signal output pin. In demultiplexed output mode, the odd dot display period signal is output. In straight output mode, the output is fixed at inactive level. The active level is programmable.
BUSY	15	Output	A	Busy signal output pin. During internal VRAM fill operation, or internal command ROM transfer, a high level signal is output.
$\overline{\text{CS}}$	1	Input	C	Chip select pin. During serial instruction transfer, a low level signal is input.
SIN	2	Input	C	Serial data input pin.
SCLK	3	Input	C	Shift clock input pin for serial transfer.
$\overline{\text{RESET}}$	13	Input	C	Reset signal input pin. Input a low level signal at power-on.
$\overline{\text{TEST}}$	14	Input	C	Test signal input pin. Input a (fixed) high level signal during normal operation.
V_{DD}	7, 9, 21	—	—	+3.3 V power supply pins.
V_{SS}	4, 6, 23	—	—	Ground pins
TCLKI	8	Input	B	Test clock input pin. Input a (fixed) low level signal during normal operation.

■ INPUT/OUTPUT CIRCUIT TYPES

Type	Circuit diagram	Remarks
A		- CMOS output
B		- CMOS hysteresis input
C		- CMOS hysteresis input with pull-up resistance (approx. 50 kΩ)

■ BLOCK DIAGRAM


DISP
RESET
VSYNC
HSYNC
CS
SIN
SCLK
BUSY
DCLKI
Serial input control
Command ROM transfer control
Command ROM
(16 Kbyte)
Display control
Display memory VRAM
(32 ch. × 16 row)
Font ROM
(512 fonts)
Clock
Dot clock control
EVEN display output control
ODD display output control
DA0
DA1
DA2
DA3
VOBA
DB0
DB1
DB2
DB3
VOBB
DCLKO

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0 V Typ.)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{DD}	V_{SS} – 0.5	V_{SS} + 4.0	V	
Input voltage	V_{IN}	V_{SS} – 0.5	V_{DD} + 0.5	V	
Output voltage	V_{OUT}	V_{SS} – 0.5	V_{DD} + 0.5	V	
Power consumption	Pd	—	400	mW	
Operating temperature	Ta	0	70	°C	
Storage temperature	Tstg	–55	+125	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0 V Typ.)

Parameter	Symbol	Values		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{DD}	3.0	3.6	V	
“H” level input voltage	V_{IH}	0.8 × V_{DD}	V_{DD} + 0.3	V	
“L” level input voltage	V_{IL}	V_{SS} – 0.3	0.2 × V_{DD}	V	
Operating temperature	Ta	0	70	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(V_{SS} = 0 V, Ta = 0 to 70 °C)

Parameter	Symbol	Pin	Conditions	Values			Unit
				Min.	Typ.	Max.	
"H" level output voltage	V_{OH}	All output pins	V_{DD} = 3.3 V I_{OH} = –8.0 mA	V_{DD} – 0.5	—	—	V
"L" level output voltage	V_{OL}	All output pins	V_{DD} = 3.3 V I_{OL} = 8.0 mA	—	—	0.4	V
Pull-up resistance	R_P	$\overline{\text{CS}}$, SIN, SCLK, $\overline{\text{RESET}}$, $\overline{\text{TEST}}$	V_{DD} = 3.3 V	25	50	200	kΩ
Input leak current	I_{IL}	DCLKI $\overline{\text{HSYNC}}$ $\overline{\text{VSYNC}}$ DISP	V_I = 0 V to V_{DD}	–0.5	—	5.0	µA
Power supply current	I_{DD}	V_{DD}	V_{DD} = 3.6 V Dot clock 140 MHz	—	—	95	mA
			V_{DD} = 3.6 V Dot clock 100 MHz	—	—	70	mA
			V_{DD} = 3.6 V Dot clock 60 MHz	—	—	45	mA
			V_{DD} = 3.6 V Dot clock 10 MHz	—	—	15	mA

2. Input/Output Pin Capacitance

Parameter	Symbol	Measurement conditions	Values		Unit
			Min.	Max.	
Input pins	C_{IN}	V_I = 0 V, V_{DD} = 0 V f = 1 MHz, Ta = 25 °C	—	16	pF
Output pins	C_{OUT}		—	16	pF

3. AC Characteristics

AC characteristics are measured under the following conditions :

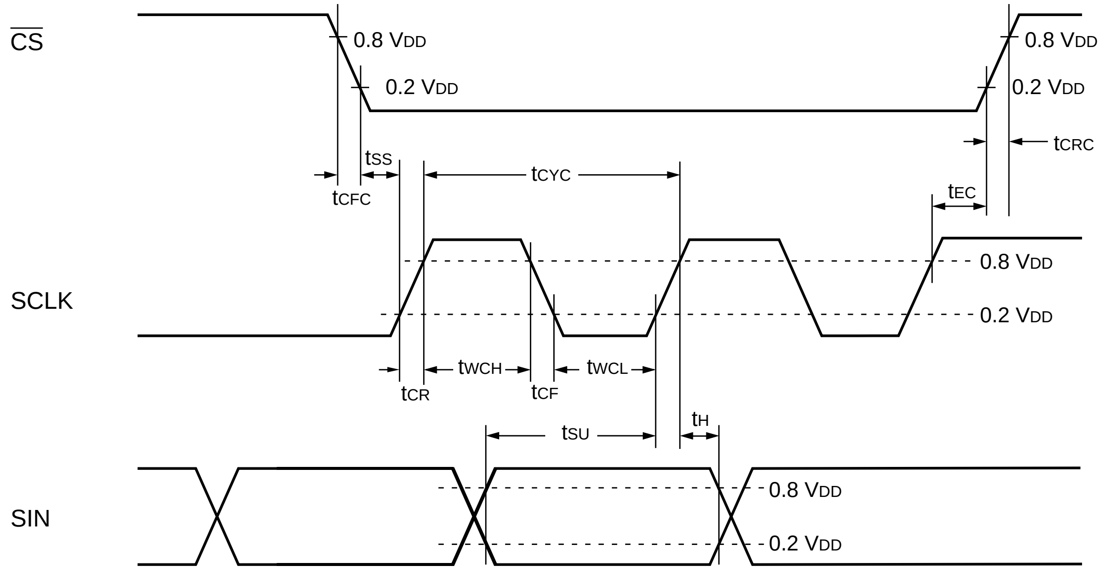
Measurement conditions : C = 28 pF, t_r = 1 ns , t_f = 1 ns, V_{OH} = 0.8 V_{DD}, V_{OL} = 0.2 V_{DD}, V_{IH} = 0.8 V_{DD}, V_{IL} = 0.2 V_{DD}

(1) Serial Input Timing

(V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70 °C)

Parameter	Symbol	Pin	Values		Unit	Remarks
			Min.	Max.		
Shift clock cycle time	t_{CYC}	SCLK	250	—	ns	
Shift clock pulse width	t_{WCH}	SCLK	100	—	ns	
	t_{WCL}		100	—	ns	
Shift clock signal rise-fall time	t_{CR}	SCLK	—	200	ns	
	t_{CF}		—	200	ns	
Shift clock start time	t_{SS}	SCLK	100	—	ns	
Data setup time	t_{SU}	SIN	100	—	ns	
Data hold time	t_H	SIN	50	—	ns	
Chip select end time	t_{EC}	$\overline{CS}$	100	—	ns	
Chip select signal rise-fall time	t_{CRC}	$\overline{CS}$	—	200	ns	
	t_{CFC}		—	200	ns	

- **Serial input timing**


$\overline{CS}$
0.8 V_{DD}
0.2 V_{DD}
0.8 V_{DD}
0.2 V_{DD}
t_{CRC}
t_{SS}
t_{CFC}
t_{CYC}
t_{EC}
SCLK
0.8 V_{DD}
0.2 V_{DD}
t_{WCH}
t_{WCL}
t_{CR}
t_{CF}
t_H
t_{SU}
SIN
0.8 V_{DD}
0.2 V_{DD}

(2) Vertical Synchronization, Horizontal Synchronization, Display Output Control Signal Input Timing

(V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70 °C)

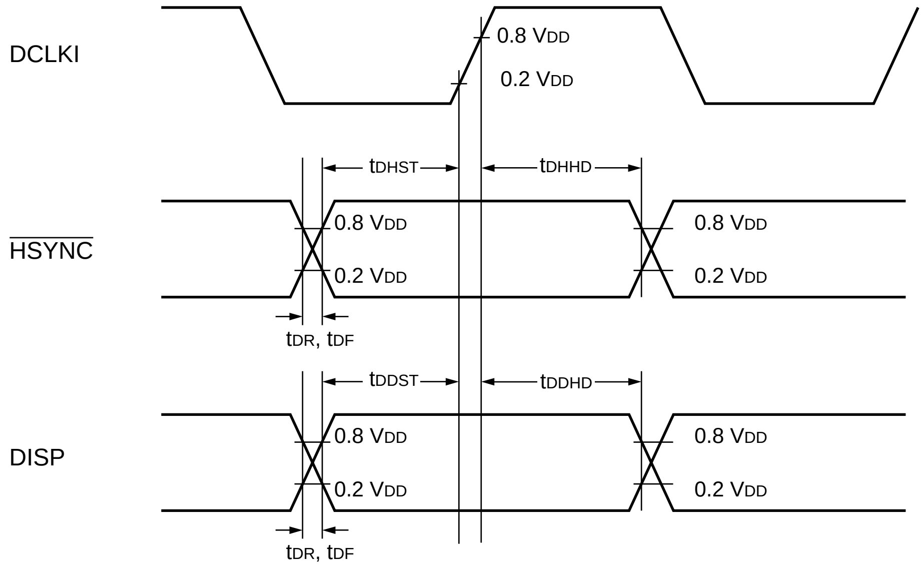
Parameter	Symbol	Pin	Values		Unit	Remarks
			Min.	Max.		
Horizontal sync signal cycle time	t_{HCYC}	$\overline{\text{HSYNC}}$	100 + t_{WH}	—	Dot clock	
Horizontal sync signal pulse width	t_{WH}	$\overline{\text{HSYNC}}$	20	—	Dot clock	*
			—	6	µs	
Horizontal sync signal setup time	t_{DHST}	$\overline{\text{HSYNC}}$	4	—	ns	
Horizontal sync signal hold time	t_{DHHD}		0	—	ns	
Vertical sync signal setup time	t_{HVST}	$\overline{\text{VSYNC}}$	5	1H – 5	Dot clock	
Vertical sync signal hold time	t_{HVHD}		3	—	H	
Display output control signal setup time	t_{DDST}	DISP	4	—	ns	
Display output control signal hold time	t_{DDHD}		0	—	ns	
Input sync signal rise-fall time	t_{DR} t_{DF}	$\overline{\text{HSYNC}}$ $\overline{\text{VSYNC}}$ DISP	—	2	ns	

* : During the horizontal synchronization pulse width, the MB90098A internal operations are temporarily paused and writing to the internal VRAM is disabled. For this reason it is necessary to set both the horizontal synchronization signal pulse width and the VRAM write cycle so that :

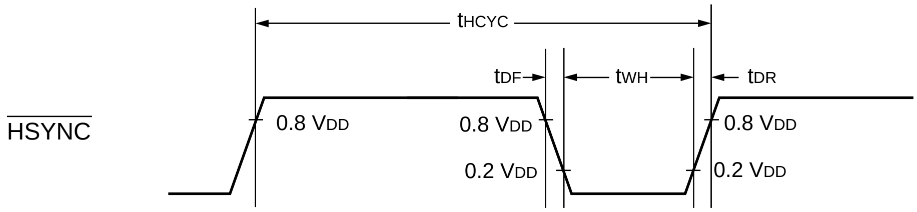
Horizontal sync signal pulse width < VRAM write cycle

Specifically, the period between instructions should be adjusted so that instruction 2 or instruction 4 (the VRAM write instruction) is not repeated during the period of one horizontal sync signal pulse width.
If the above condition is not satisfied, writing to VRAM will not be executed normally.

- **Horizontal synchronization signal, display output control signal input timing**

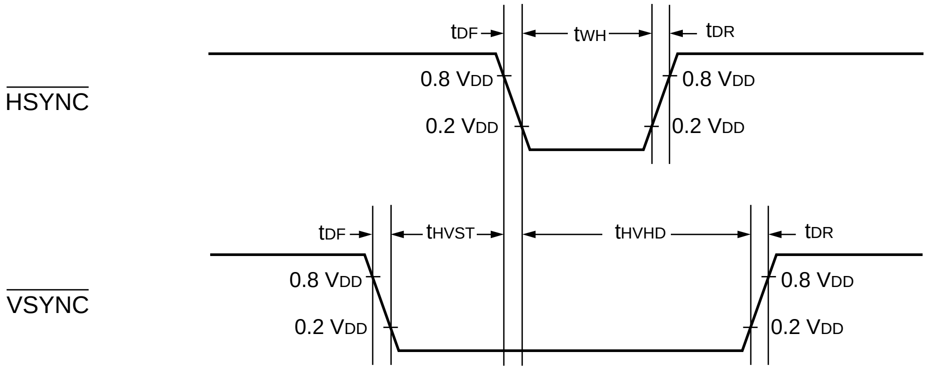


- **Horizontal synchronization signal input**

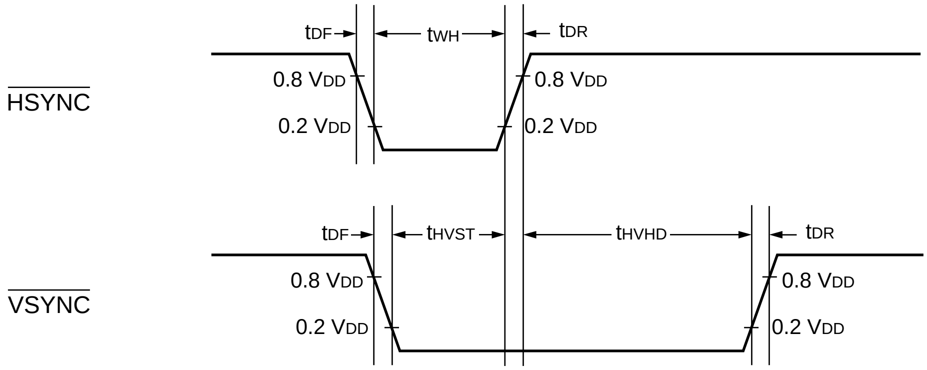

t_{HCYC}
t_{DF}
t_{WH}
t_{DR}
$\overline{\text{HSYNC}}$
0.8 V_{DD}
0.8 V_{DD}
0.8 V_{DD}
0.2 V_{DD}
0.2 V_{DD}

- **Vertical synchronization signal input timing**

VSYNC detection at HSYNC leading-edge


t_{DF}
t_{WH}
t_{DR}
$\overline{\text{HSYNC}}$
0.8 V_{DD}
0.8 V_{DD}
0.2 V_{DD}
0.2 V_{DD}
t_{DF}
t_{HVST}
t_{HVHD}
t_{DR}
$\overline{\text{VSYNC}}$
0.8 V_{DD}
0.8 V_{DD}
0.2 V_{DD}
0.2 V_{DD}

VSYNC detection at HSYNC trailing edge


t_{DF}
t_{WH}
t_{DR}
$\overline{\text{HSYNC}}$
0.8 V_{DD}
0.8 V_{DD}
0.2 V_{DD}
0.2 V_{DD}
t_{DF}
t_{HVST}
t_{HVHD}
t_{DR}
$\overline{\text{VSYNC}}$
0.8 V_{DD}
0.8 V_{DD}
0.2 V_{DD}
0.2 V_{DD}

(3) Display Signal Timing

(V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70 °C)

Parameter	Symbol	Pin	Values		Unit	Remarks
			Min.	Max.		
Dot clock input cycle time (straight output)	t_{DIFS}	DCLKI	10	90	MHz	* 1 * 3
Dot clock input pulse width (straight output)	t_{DIWHS}	DCLKI	5	—	ns	* 1 * 3
	t_{DIWLS}		5	—	ns	
Dot clock input cycle time (demultiplexed output)	t_{DIFD}	DCLKI	10	140	MHz	* 2 * 3
Dot clock input pulse width (demultiplexed output)	t_{DIWHD}	DCLKI	3	—	ns	* 2 * 3
	t_{DIWLD}		3	—	ns	
Display output control on/off delay time	t_{DON}	DA3 to DA0, VOBA DB3 to DB0, VOBB	6	—	Dot clock	*4
	t_{DOFF}		—	6		
Dot clock output delay time 1	t_{PDCS}	DCLKO	3	6	ns	*1
Dot clock output delay time 2	t_{PDCD}	DCLKO	3	7	ns	*2
Display signal output delay time I1 (straight output)	t_{PDIS1}	DA3 to DA0, VOBA DB3 to DB0, VOBB	2	7	ns	*1
Display signal output delay time I2 (straight output)	t_{PDIS2}	DA3 to DA0, VOBA DB3 to DB0, VOBB	1	6	ns	*1
Display signal output delay time O1 (straight output)	t_{PDOS1}	DA3 to DA0, VOBA DB3 to DB0, VOBB	–4	5	ns	*1
Display signal output delay time O2 (straight output)	t_{PDOS2}	DA3 to DA0, VOBA DB3 to DB0, VOBB	–5	4	ns	*1
Display signal output delay time I1 (demultiplexed output)	t_{PDID1}	DA3 to DA0, VOBA DB3 to DB0, VOBB	2	7	ns	*2
Display signal output delay time I2 (demultiplexed output)	t_{PDID2}	DA3 to DA0, VOBA DB3 to DB0, VOBB	1	6	ns	*2
Display signal output delay time O1 (demultiplexed output)	t_{PDOD1}	DA3 to DA0, VOBA DB3 to DB0, VOBB	–5	5	ns	*2
Display signal output delay time O2 (demultiplexed output)	t_{PDOD2}	DA3 to DA0, VOBA DB3 to DB0, VOBB	–6	4	ns	*2

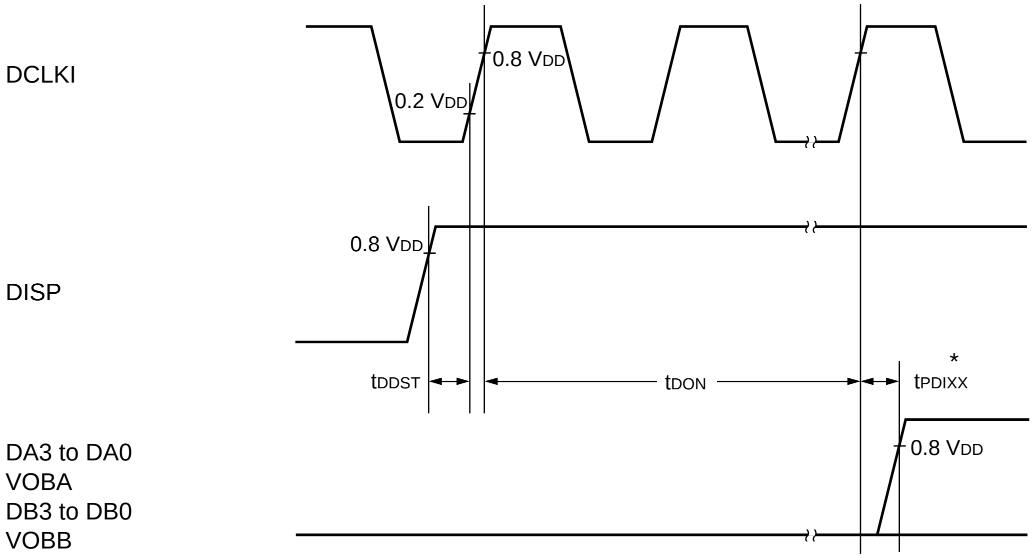
*1 : The maximum output frequency for straight output is 90 MHz.

*2 : The maximum output frequency for demultiplexed output is 70 MHz.

*3 : Use a continuous dot clock input signal without interruptions.

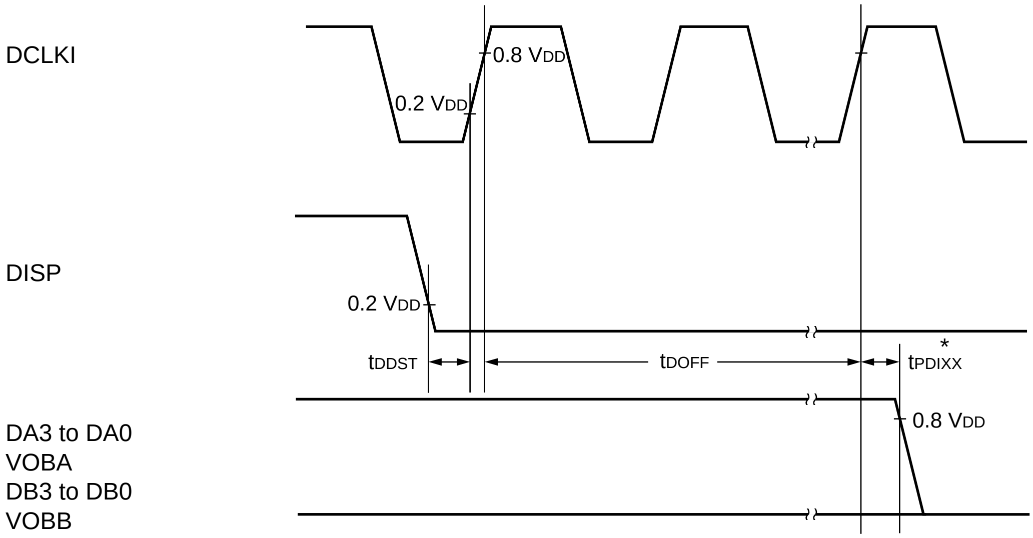
*4 : Actual display output varies according to control content, including display output control for each display layer, display position control, etc.

- **Display output control ON timing**


DCLKI
0.8 VDD
0.2 VDD
DISP
0.8 VDD
tDDST
tDON
tPDIXX
*
DA3 to DA0
VOBA
DB3 to DB0
VOBB
0.8 VDD

* : t_{PDIXX} represents t_{PDIS1}, t_{PDIS2}, t_{PDID1}, or t_{PDID2} depending on the operating mode.

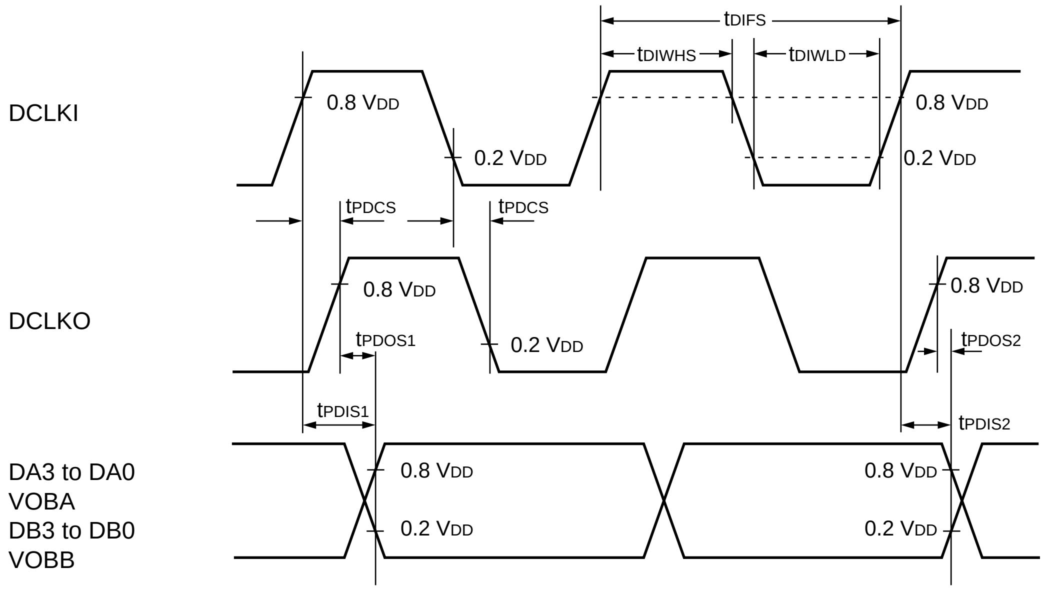
- **Display output control OFF timing**


DCLKI
0.8 VDD
0.2 VDD
DISP
0.2 VDD
tDDST
tDOFF
tPDIXX
*
DA3 to DA0
VOBA
DB3 to DB0
VOBB
0.8 VDD

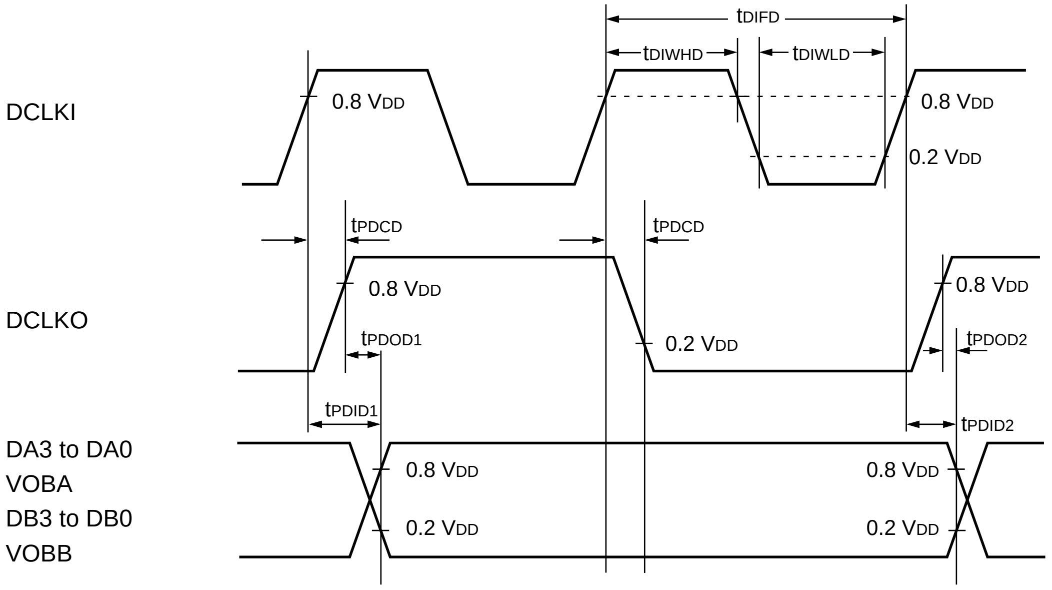
* : t_{PDIXX} represents t_{PDIS1}, t_{PDIS2}, t_{PDID1}, or t_{PDID2} depending on the operating mode.

- **Display signal output timing**

Straight output

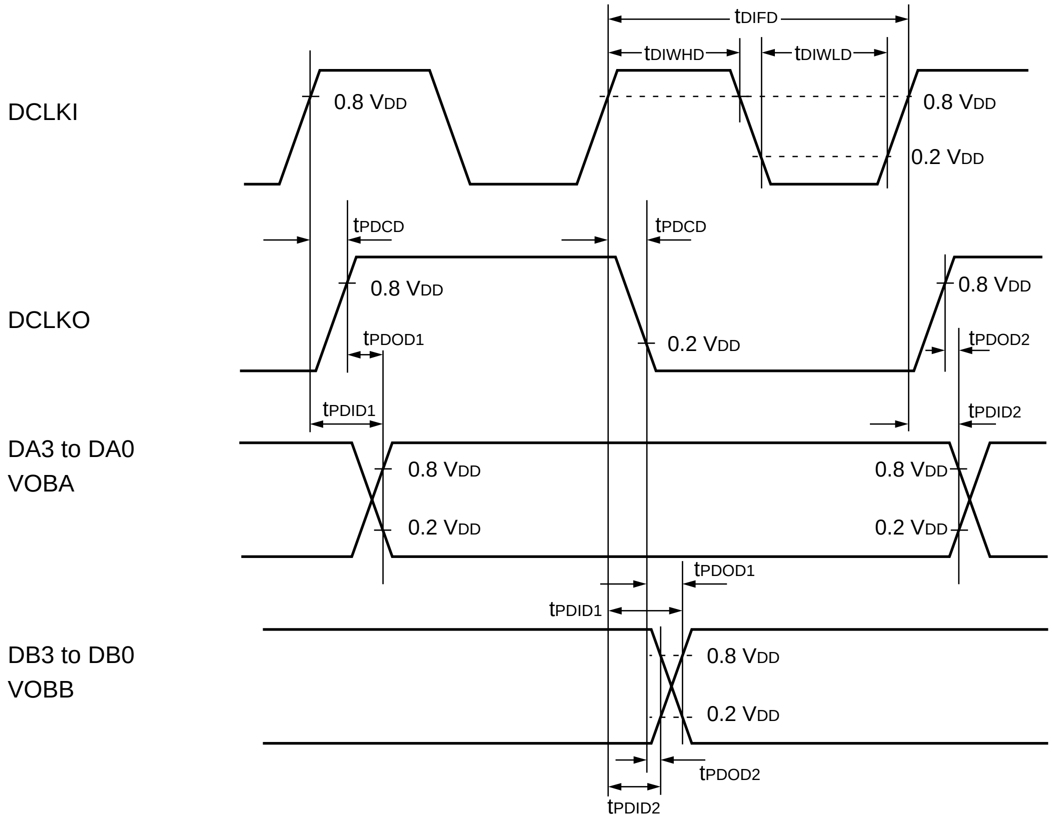

tDIFS
tDIWHS
tDIWLD
DCLKI
0.8 VDD
0.2 VDD
0.8 VDD
0.2 VDD
tPDCS
tPDCS
DCLKO
0.8 VDD
0.2 VDD
0.8 VDD
tPDOS1
tPDOS2
tPDIS1
tPDIS2
DA3 to DA0
VOBA
DB3 to DB0
VOBB
0.8 VDD
0.2 VDD
0.8 VDD
0.2 VDD

Demultiplexed output (single phase mode)


tDIFD
tDIWHD
tDIWLD
DCLKI
0.8 VDD
0.8 VDD
0.2 VDD
tPDCD
tPDCD
DCLKO
0.8 VDD
0.2 VDD
0.8 VDD
tPDOD1
tPDOD2
tPDID1
tPDID2
DA3 to DA0
VOBA
DB3 to DB0
VOBB
0.8 VDD
0.2 VDD
0.8 VDD
0.2 VDD

- **Display signal output timing**

Demultiplexed output (2 phase mode)

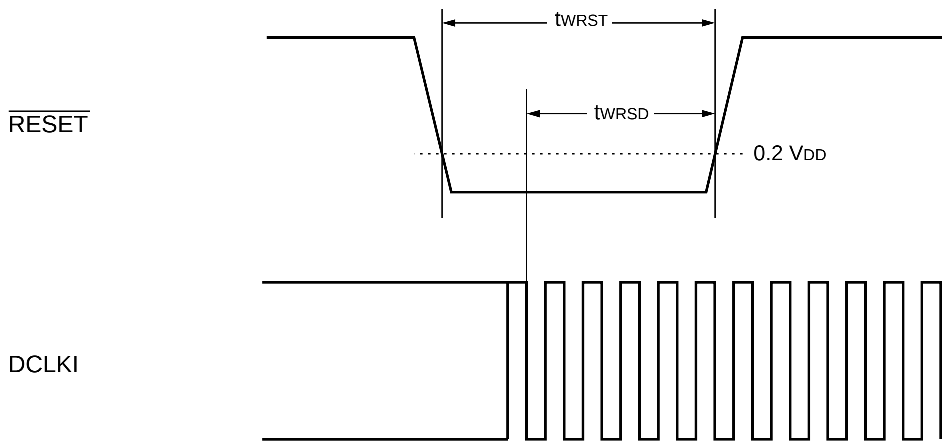

tDIFD
tDIWHD
tDIWLD
DCLKI
0.8 VDD
0.8 VDD
0.2 VDD
tPDCD
tPDCD
DCLKO
0.8 VDD
0.8 VDD
tPDOD1
0.2 VDD
tPDOD2
tPDID1
tPDID2
DA3 to DA0
VOBA
0.8 VDD
0.2 VDD
0.8 VDD
0.2 VDD
tPDOD1
tPDID1
DB3 to DB0
VOBB
0.8 VDD
0.2 VDD
tPDOD2
tPDID2

(4) Reset Input Timing

(V_{DD} = 3.3 V ± 0.3 V, V_{SS} = 0 V, Ta = 0 to 70 °C)

Parameter	Symbol	Pin	Values		Unit	Remarks
			Min.	Max.		
Reset pulse width	t_{WRST}	$\overline{\text{RESET}}$	1	—	µs	
Clock input	t_{WRSD}	DCLKI	5	—	Dot clock	

- **Reset input timing**


t_{WRST}
$\overline{\text{RESET}}$
t_{WRSD}
0.2 V_{DD}
DCLKI

■ DISPLAY CONTROL COMMANDS

1. Command List

Com-mand No.	Function	Command Code/Data												
		15-12	11	10	9	8	7	6	5	4	3	2	1	0
0	VRAM write address setting	0000	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0
1	Character data 1 setting	0001	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0
2	Character data 2 setting	0010	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0
3	Row control data 1 setting	0011	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0
4	Row control data 2 setting	0100	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0
5-00	Screen output control 1A	0101	0	0	0	0	SDS	UDS	PDS	DSP	0	0	0	0
5-03	Screen output control 1B	0101	0	0	1	1	0	0	0	0	EOD	EOT	EOP	EOO
5-1	Screen output control 2	0101	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0
5-2	Vertical display position control	0101	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0
5-3	Horizontal display position control	0101	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0
6-0	Character vertical size control	0110	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA0
6-1	Shaded background frame color control	0110	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0
6-2	Transparent color control	0110	1	0	TC	0	TC3	TC2	TC1	TC0	0	0	0	0
6-3	Graphic color control	0110	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0
7-1	Screen background character control 1	0111	0	1	PD1	PD0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0
7-3	Screen background character control 2	0111	1	1	1	0	0	PH2	PH1	PH0	U3	U2	U1	U0
8-1	Sprite character control 1	1000	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0
8-2	Sprite character control 2	1000	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0

(Continued)

(Continued)

Command No.	Function	Command Code/Data												
		15-12	11	10	9	8	7	6	5	4	3	2	1	0
9-0	Sprite character control 3	1001	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0
9-1	Sprite character control 4	1001	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0
11-0	Synchronization control	1011	0	0	0	0	EG1	1	0	0	0	0	0	0
11-2	Dot clock control 1	1011	1	0	DO	0	0	0	0	0	0	0	0	0
13-0	Input/output pin control 1	1101	0	0	0	VHE	HE	0	0	0	0	0	DBX	DCX
13-1	Input/output pin control 2	1101	0	1	0	0	0	0	0	0	0	IHX	IVX	IDX
14-0	CROM transfer start address 1	1110	0	0	0	0	0	0	TSD	TSC	TSB	TSA	TS9	TS8
14-1	CROM transfer start address 2	1110	0	0	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	0
14-2	CROM transfer end address 1	1110	0	1	0	0	0	0	TED	TEC	TEB	TEA	TE9	TE8
14-3	CROM transfer end address 2	1110	0	1	1	TSV	TE7	TE6	TE5	TE4	TE3	TE2	TE1	1

Note : When a reset signal is input (L level signal input to the $\overline{\text{RESET}}$ pin) , the screen output control 1A bits SDS, UDS, PDS, DSP and the input/output pin control 1 bits DBX and DCX are initialized to “0.” Other register bits and VRAM contents are undefined.

After reset input/release is completed, set all register bits except for the command ROM transfer address settings (commands 14-0, 14-1, 14-2, 14-3) and set all VRAM settings (character data and row control data) .

2. Command Descriptions

- **Command 0 (VRAM write address setting)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	AY3	AY2	AY1	AY0	FL	0	0	AX4	AX3	AX2	AX1	AX0

AY3-AY0 : Row address (0_H-F_H)

AX4-AX0 : Column address (0_H-$1F_H$)

FL : VRAM fill (0 : Off, 1 : On)

[Function]
This command sets the VRAM write address and turns VRAM fill on or off.

It is used to make row/column address settings before setting character data (issuing commands 1, 2) or to make row address settings before setting line control data (issuing commands 3, 4) .

VRAM fill is activated by executing the character data setting 2 (command 2) .

[Additional information]

- For normal write operation (writing 1 character data or 1 row control data) the VRAM fill setting should be “Off” (FL = 0) .
- VRAM write address settings entered using this command are automatically incremented after each execution of the character data setting 2 command (command 2) . (After the last column the address increment is to the first column of the next row, and after the last column of the last row the address increment is to the first column of the first row.)
- The VRAM fill function is a function that sets the same character data specified by the character data command setting 1, 2 (command 1, 2) to character VRAM starting from the row and column address specified by command 0 to the final row (row 16) and final column (column 32) . The VRAM fill function is activated by the execution of the character data setting 2 command (command 2) .
- During activation and execution of VRAM fill, the BUSY pin outputs an H level signal.
- During VRAM fill execution, do not issue commands 1-4.

(Caution)

- During row control data setting (command 3, 4) the column address (AX4-AX0) is ignored. Also, the address is not incremented automatically after row control data setting.
- The VRAM fill setting is effective only during character data setting (command 1, 2) .

- **Command 1 (Character data 1 setting)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	1	MS1	MS0	MM1	MM0	MB3	MB2	MB1	MB0	MC3	MC2	MC1	MC0

MC3-MC0 : Character color (16 colors)

MB3-MB0 : Background color (16 colors)

MM1, MM0 : Character background control
(0, 0 : Off)
(0, 1 : Solid fill)
(1, 0 : concaved shaded)
(1, 1 : convexed shaded)

MS1, MS0 : Character horizontal size control

(0, 0 : 12 dots)
(0, 1 : 18 dots)
(1, 0 : 24 dots)
(1, 1 : Setting prohibited)

[Function]
This command sets character data. Settings are entered in VRAM and reflected on the screen by executing the character data setting 2 command (command 2) .

[Additional information]

- Character color, character background color, character background control and character horizontal size can be set in any combination for each character separately.
- Shadow effects can be set for any combination of top, bottom, left, and right directions using the combination of the character data setting 2 (command 2) MR bit and the row control data setting 2 (command 4) LD and LE bits.
- Shadow background frame color settings are made by shaded background frame color control (command 6-1) .

- **Command 2 (Character data setting 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	0	MR	MG	MBL	M8	M7	M6	M5	M4	M3	M2	M1	M0

MR : Shaded background succeeding character merge control
(0 : Not merged with succeeding character)
(1 : Merged with succeeding character)

M8-M0 : Character code

MG : Character/graphic character control
(0 : Character, 1 : Graphic character)

MBL : Blink control (0 : Off, 1 : On)

[Function]
This command writes the character data set by the character data setting 1 command (command 1) together with the settings in this command, to VRAM at the address specified by the VRAM write address setting command (command 0) .

After this command is executed, the VRAM write address is automatically incremented.

[Additional information]
- Setting the blink control bit to “On” (MBL = 1) causes the display to blink according to the setting of the screen output control 2 (command 5-1) BT1, BT0, BD1, BD0 bits.
- The shadow background right character combination control bit (MR) is used only with characters for which the shadow background is specified by the character data setting 1 (command 1) bit (MM1 = 1) .

(Caution)
- At power-on, the contents of VRAM are undefined. Be sure to set all RAM data before the display is started.

- **Command 3 (Row control data setting 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1	LHS	LW2	LW1	LW0	LFD	LFC	LFB	LFA	LF3	LF2	LF1	LF0

LHS : Row character vertical size type control
  (0 : Character vertical size A)
  (1 : Character vertical size B)

LW2-LW0 : Row spacing control
  (0-14 dots, in 2-dot units)

LF3-LF0 : Border color (16 colors)

LFD, LFC : Border output control
  (0, 0 : All off)
  (0, 1 : No character background, character only border on)
  (1, 0 : No character background, solid fill character only border on)
  (1, 1 : Border output on)

LFB, LFA : Border control
  (0, 0 : Border off)
  (0, 1 : Right border)
  (1, 0 : Left border)
  (1, 1 : Left, right border)

[Function]
This function sets row control data.

Settings are written to row VRAM and reflected on the screen when the row control data setting 2 command (command 4) is executed.

[Additional information]
- The character vertical size A/B setting selected by the row character vertical size type control bit (LHS) applies the character vertical size type control setting (command 6-0) .
- The border format setting applies the border format control setting (FM1, FM0) in the screen output control 2 command (command 5-1) .

- **Command 4 (Row control data setting 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	LDS	0	LG1	LG0	LD	LE	LM1	LM0	L3	L2	L1	L0

LDS : Row character output control
(0 : Off, 1 : On)

LG1, LG0 : Row enlargement control
(0, 0 : Normal)
(0, 1 : Double width)
(1, 0 : Double height)
(1, 1 : Double height & width)

LE : Character background extention control
(0 : Normal, 1 : Extended)

LD : Shadow background lower row link control
(0 : Separate, 1 : Lower row link)

LM1, LM0 : Row background control
(0, 0 : Off)
(0, 1 : Solid display)
(1, 0 : Shadow concave)
(1, 1 : Shadow convex)

L3-L0 : Row background color (16 colors)

[Function]
This command writes the data set in the row control data setting 1 command (command 3) , together with the settings in this command, to VRAM at the address specified by the set VRAM write address command (command 0) .

[Additional Information]
- The shadow background lower row link control bit (LD bit) applies to the character background shadow and row background shadow effects.

(Caution)
- At power-on, the contents of VRAM are undefined. Be sure to set all RAM data before the display is started.
- After this command is executed, the VRAM write address is not automatically incremented. It is necessary to set the VRAM write address (command 0) for each row for which row control data is set.

- **Command 5-00 (Screen output control 1A)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	0	0	SDS	UDS	PDS	DSP	0	0	0	0

SDS : Sprite character output control
(0 : Off, 1 : On)

UDS : Screen background output control
(0 : Off, 1 : On)

PDS : Screen background character output control
(0 : Off, 1 : On)

DSP : Display output control
(Character + border + character background + row background control)
(0 : Off, 1 : On)

[Function]
This command controls screen display output.

- **Command 5-03 (Screen output control 1B)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	0	1	1	0	0	0	0	EOD	EOT	EOP	EOO

EOD : Demultplexed output synchronization control
(0 : Internal HSYNC sychronization)
(1 : DISP synchronization)

EOT : Demultiplexed output timing control
(0 : Synchronized timing + 0 clock)
(1 : Synchronized timing + 1 clock)

EOP : Demultiplexed output phase control
(0 : Synchronized output)
(1 : 2-phase output)

EOO : Straight/demultiplexed output control
(0 : Straight output)
(1 : Demultiplexed output)

[Function]
This function controls screen display output.

[Additional information]

- By setting the straight/demultiplexed output selection to demultiplexed output (EOO = 1) , the display signal is output in parallel from the DA3-0, VOBA pins and the DB3-0, VOBB pins.
- When the demultiplexed output synchronization control selection is “Internal HSYNC synchronization” (EOD = 0) , the horizontal sync operating edge selection is determined by the horizontal sync operating edge setting (HE bit) in the input/output pin control 1 command (command 13-0) .

- **Command 5-1 (Screen output control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	0	1	FM1	FM0	BT1	BT0	BD1	BD0	0	0	0	0

BT1, BT0 : Blink period control
    (0, 0 : 16 V)
    (0, 1 : 32 V)
    (1, 0 : 48 V)
    (1, 1 : 64 V)

BD1, BD0 : Blink duty control
    (0, 0 : On : Off = 1 : 0 always on)
    (0, 1 : On : Off = 1 : 1)
    (1, 0 : On : Off = 1 : 3)
    (1, 1 : On : Off = 3 : 1)

FM1, FM0 : Border format control
    (0, 0 : Side border 1 dot)
    (0, 1 : Side border 2 dot)
    (1, 0 : Pattern background 1)
    (1, 1 : Pattern background 2)

[Function]
This function controls screen display output.

[Additional Information]
- The blink period control and blink duty control settings apply to control of characters specified for blink control (MBL = 1) in the character data setting 2 command (command 2) as well as to sprite characters specified for sprite character blink control (SBL = 1) in the sprite character control 2 command (command 8-2) .

- **Command 5-2 (Vertical display position control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	0	0	Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

Y8-Y0 : Vertical display position control
    (0-2044, 4-dot units)

[Function]
This function controls the vertical display position on the screen.

- **Command 5-3 (Horizontal display position control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	X8	X7	X6	X5	X4	X3	X2	X1	X0

X8-X0 : Horizontal display position control
    (0-2044, 4-dot units)

[Function]
This function controls the horizontal display position on the screen.

- **Command 6-0 (Character vertical size control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	0	0	0	0	HB2	HB1	HB0	0	HA2	HA1	HA0

HB2-HB0 : Character vertical size control B
(18-32 dots, 2-dot units)

HA2-HA0 : Character vertical size control A
(18-32 dots, 2-dot units)

[Function]
This function controls the character vertical size A and B settings.

[Additional Information]
- The main screen display allows a selection between character sizes A and B by row. In the set row data 1 command (command 3) , the selection of character size A or B is made by the row character vertical size type control (LHS bit) . This command is used to set the vertical display dot count of both type A and B.

- **Command 6-1 (Shaded background frame color control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	0	1	0	0	BH3	BH2	BH1	BH0	BS3	BS2	BS1	BS0

BH3-BH0 : Shadow background frame highlight color (16 colors)

BS3-BS0 : Shadow background frame shadow color (16 colors)

[Function]
This function controls the shadow background border color.

[Additional Information]
- The shadow background border color is determined by the shadow character background designation (MM1 = 1) in the character data setting 1 command (command 1) , as well as the shadow row background designation (LM1 = 1) in the row control data setting 2 command (command 4) .
- The shadow background border highlight color and shadow color are shown in the following areas :

	Character background		**Row background**	
	Shadow background concave	**Shadow background convex**	**Shadow background concave**	**Shadow background convex**
Shadow background frame highlight color	Lower edge, right edge	Upper edge, left edge	Lower edge	Upper edge
Shadow background frame shadow color	Upper edge, left edge	Lower edge, right edge	Upper edge	Lower edge

- **Command 6-2 (Transparent color control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	0	TC	0	TC3	TC2	TC1	TC0	0	0	0	0

TC : Transparent color control
(0 : Off, 1 : On)

TC3-TC0 : Transparent color code (16 colors)

[Function]
This function controls the transparent color.

[Additional Information]

- The transparent color code (TC3-TC0) may be set to any desired color code, and the transparent color control set to On (TC = 1) so that any display area of the specified color will be rendered invisible. Areas of the specified color will be output as the underlying layer display.

- **Command 6-3 (Graphic color control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	1	GF	GC	GF3	GF2	GF1	GF0	GC3	GC2	GC1	GC0

GF : Graphic color border color replacement control
(0 : Off, 1 : On)

GC : Graphic color character color replacement control
(0 : Off, 1 : On)

GF3-GF0 : Border color replacement color code (16 colors)

GC3-GC0 : Character color replacement color code (16 colors)

[Function]
This function replaces a specified color in graphic characters with a character color or border color in the display.

[Additional information]

- The graphic character display color is fixed and registered in font ROM. This command can be used to replace any specified graphic character display color with the border color or character color.
- Any desired color in a graphic character (specified by the GF3-GF0 bits) can be replaced by the border color (LF3-LF0) set in the row control data setting 1 command (command 3) .
- Any desired color in a graphic character (specified by the GC3-GC0 bits) can be replaced by the character color (MC3-MC0) set in the character data setting 1 command (command 1) .
- If the graphic color border color replacement control is on (GF bit = 1) and the transparent color control is on (TC bit = 1 in command 6-2) , and also the graphic color border color replacement color code is the same as the transparent color code (TC3-0 in command 6-2) , the border color replacement has priority.
- If the graphic color border color replacement control is on (GF bit = 1) and the transparent color control is on (TC bit = 1 in command 6-2) , and also the border color of the border color replacement color code (LF3-LF0 in command 3) is the same as the transparent color code (TC3-0 in command 6-2) , the color will be transparent and the lower layer color will be displayed.
- If the graphic color character color replacement control is on (GC bit = 1) and the transparent color control is on (TC bit = 1 in command 6-2) , and also the graphic color character color replacement color code is the same as the transparent color code (TC3-0 in command 6-2) , the character color replacement has priority.
- If the graphic color character color replacement control is on (GC bit = 1) and the transparent color control is on (TC bit = 1 in command 6-2) , and also the characterer color of the characterer color replacement color code (MC3-MC0 in command 1) is the same as the transparent color code (TC3-0 in command 6-2) , the color will be transparent the the lower layer color will be displayed.
- If the graphic color character color replacement control is on (GC bit = 1) and the graphic color border color replacement control is on (GF bit = 1) , the character color replacement color code (GC3-GC0 bits) and border color replacement color code (GF3-GF0 bits) should be set to different colors.

(Caution)

- This command applies only to the color of main screen graphic characters. It has no affect on the color of sprite characters of screen background character dot colors.

- **Command 7-1 (Screen background character control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	0	1	PD1	PD0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

PD1, PD0 : Screen background character configuration control
(0, 0 : 1 character)
(0, 1 : 2 characters horizontal)
(1, 0 : 2 characters vertical)
(1, 1 : 2 characters horizontal × 2 vertical)

PM7-PM0 : Screen background character code
(000_H to $0FF_H$, 256 types)

[Function]
This function controls screen background characters.

[Additional Information]
- Screen background character control is applied when the screen background character output control bit is turned On (PDS = 1) in the screen output control 1A command (command 5-00) .
- The vertical size of screen background characters can be controlled by setting the screen background character vertical size control bits (PH2-PH0) in the screen background character control 2 command (command 7-3) .

(Caution)
- Screen background characters can be displayed only as graphic characters.
- The screen background character code (PM7-PM0) can be set to only 256 code settings from 000h to 0FFh.
- The screen background character graphic color cannot be controlled by the graphic color control (command 6-3) graphic color border color replacement control or graphic color character color replacement control.

- **Command 7-3 (Screen background character control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	1	0	0	PH2	PH1	PH0	U3	U2	U1	U0

PH2-PH0 : Screen background character vertical size control
(18-32 dots in 2-dot units)

U3-U0 : Screen background color (16 colors)

[Function]
This function controls screen background characters and screen background colors.

[Additional Information]
- The screen background color is displayed by setting the screen output control (command 5-00) screen background output control bit to on (UDS = 1) .
- Screen background characters are displayed by setting the screen output control (command 5-00) screen background character output control bit to on (PDS = 1) .

- **Command 8-1 (Sprite character control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	SD1	SD0	SM7	SM6	SM5	SM4	SM3	SM2	SM1	SM0

SD1, SD0 : Sprite character configuration control
(0, 0 : 1 character)
(0, 1 : 2 characters horizontal)
(1, 0 : 2 characters vertical)
(1, 1 : 2 characters horizontal × 2 vertical)

SM7-SM0 : Sprite character code
(000$_H$ to 0FF$_H$, 256 types)

[Function]
This function controls sprite characters.

[Additional Information]
- Sprite characters are displayed by setting the screen output control (command 5-00) sprite character output control bit to on (SDS = 1) . This will start sprite character display.
- The sprite character display position is determined by setting the sprite character control 3 command (command 9-0) and sprite character control 4 command (command 9-1) .
- The vertical size of the sprite character display is determined by the sprite character vertical size control bits (SH2-SH0) in the sprite character control 2 command (command 8-2) .
- The sprite character blink control bit (SBL) turns sprite character blinking on and off.
- The sprite character blink period and duty are controlled by the settings of the BT1, BT0, BD1, BD0 bits in the screen output control command (command 5-1) .

(Caution)
- Sprite characters can only be displayed as graphic characters.
- The sprite character code (PM7-PM0) can be set to only 256 code settings from 000h to 0FFh.
- The sprite character graphic color cannot be controlled by the graphic color control (command 6-3) graphic color border color replacement control or graphic color character color replacement control.

- **command 8-2 (Sprite character control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	0	1	0	1	SBL	0	SH2	SH1	SH0	0	0	0	0

SBL : Sprite character blink control
(0 : Off, 1 : On)

SH2-SH0 : Sprite character vertical size control
(18-32 dots, in 2-dot units)

[Function]
This function controls sprite characters.

[Additional Information]
- See the additional information under sprite character control 1 (command 8-1) .

- **Command 9-0 (Sprite character control 3)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	0	0	SY9	SY8	SY7	SY6	SY5	SY4	SY3	SY2	SY1	SY0

Y9-SY0 : Sprite character vertical display position control
(0-2046, 2-dot units)

[Function]
This function controls sprite characters.

[Additional Information]
- See the additional information under sprite character control 1 (command 8-1) .

- **Command 9-1 (Sprite character control 4)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0	1	1	0	SX9	SX8	SX7	SX6	SX5	SX4	SX3	SX2	SX1	SX0

SX9-SX0 : Sprite character horizontal display position control
(0-2046, 2-dot units)

[Function]
This function controls sprite characters.

[Additional Information]
- See the additional information under sprite character control 1 (command 8-1) .

- **Command 11-0 (Synchronization control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	0	0	0	EG1	1	0	0	0	0	0	0

EG1 : Vertical enlargement control
(0 : Normal, 1 : Double)

[Function]

This function controls vertical enlargement in the synchronization system.

[Additional information]
- The vertical enlargement control bit (EG1) adjusts the vertical display size by controlling the horizontal synchronization count. This control affects the vertical size of the entire display, not only the display position.

- **Command 11-2 (Dot Clock Control)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	1	0	DO	0	0	0	0	0	0	0	0	0

DO : Dot clock pin output control
(0 : Off, 1 : On)

[Function]
This function controls dot clock output.

[Additional information]
- The internal dot clock signal can be output from the DCLKO pin by setting the dot clock pin output control bit to on (DO = 1) .

- **Command 13-0 (Input/Output Pin Control 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	0	0	VHE	HE	0	0	0	0	0	DBX	DCX

VHE : HSYNC edge selection for vertical sync detection
(0 : Leading edge, 1 : Trailing edge)

HE : Edge selection for horizontal sync operation
(0 : Trailing edge, 1 : Leading edge)

DCX : Display color signal output logic control
(0 : Positive logic, 1 : Negative logic)

DBX : Display output period signal output logic control
(0 : Positive logic, 1 : Negative logic)

[Function]
This function controls the input/output pins.

[Additional Information]

- Vertical vibration phenomena can be avoided by adjusting the input phase timing of the vertical sync signal and horizontal sync signal, using the VHE bit to select the HSYNC edge for vertical sync detection.

- **Command 13-1 (Input/Output Pin Control 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0	1	0	1	0	0	0	0	0	0	0	IHX	IVX	IDX

IHX : Horizontal sync signal input logic control
(0 : Negative logic, 1 : Positive logic)

IVX : Vertical sync signal input logic control
(0 : Negative logic, 1 : Positive logic)

IDX : Display period signal logic control
(0 : Positive logic, 1 : Negative logic)

[Function]
This function controls the input pins.

- **Command 14-0 (Command ROM Transfer Start Address 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	0	0	0	0	TSD	TSC	TSB	TSA	TS9	TS8

TSD-TS8 : Command ROM transfer start address 1 (Upper address values)

[Function]
This function sets the command ROM transfer start address 1.

[Additional Information]
- This function determines the upper address value of the starting address for command ROM transfer.

- **Command 14-1 (Command ROM Transfer Start Address 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	0	1	0	TS7	TS6	TS5	TS4	TS3	TS2	TS1	0

TS7-TS1 : Command ROM transfer start address 2 (Lower address value)

[Function]
This function sets the command ROM transfer start address 2.

[Additional Information]
- This function determines the lower address value of the starting address for command ROM transfer.

- **Command 14-2 (Command ROM Transfer End Address 1)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	0	0	0	0	TED	TEC	TEB	TEA	TE9	TE8

TED-TE8 : Command ROM transfer end address 1 (Upper address values)

[Function]
This function sets the command ROM transfer end address 1.

[Additional Information]
- This function determines the upper address value of the ending address for command ROM transfer.

- **Command 14-3 (Command ROM Transfer End Address 2)**

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1	0	0	1	1	TSV	TE7	TE6	TE5	TE4	TE3	TE2	TE1	1

TSV : Command ROM transfer sync control
(0 : Asynchronous, 1 : Synchronous)

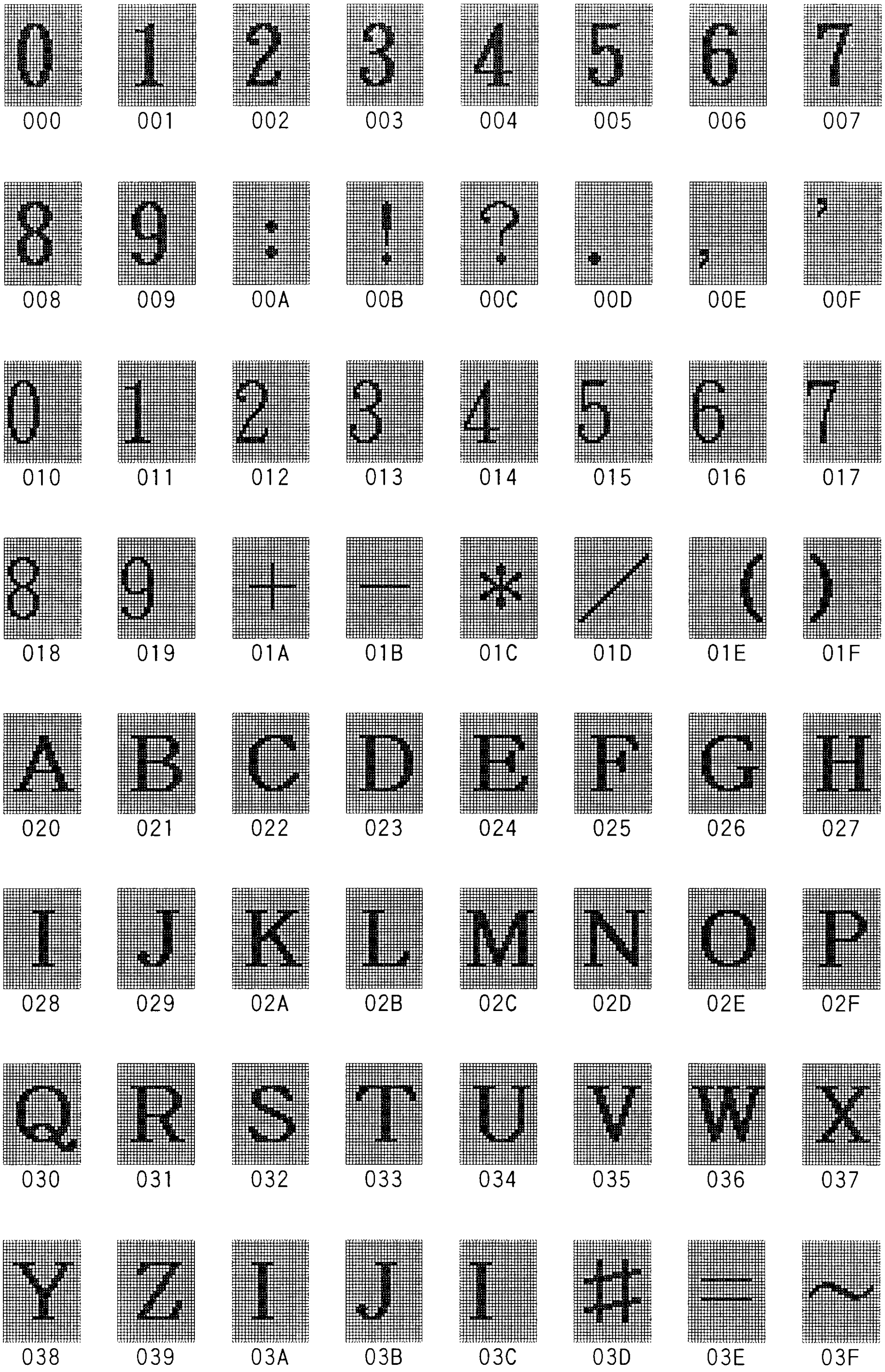
TE7 -TE1 : Command ROM transfer end address 2 (Lower address value)

[Function]

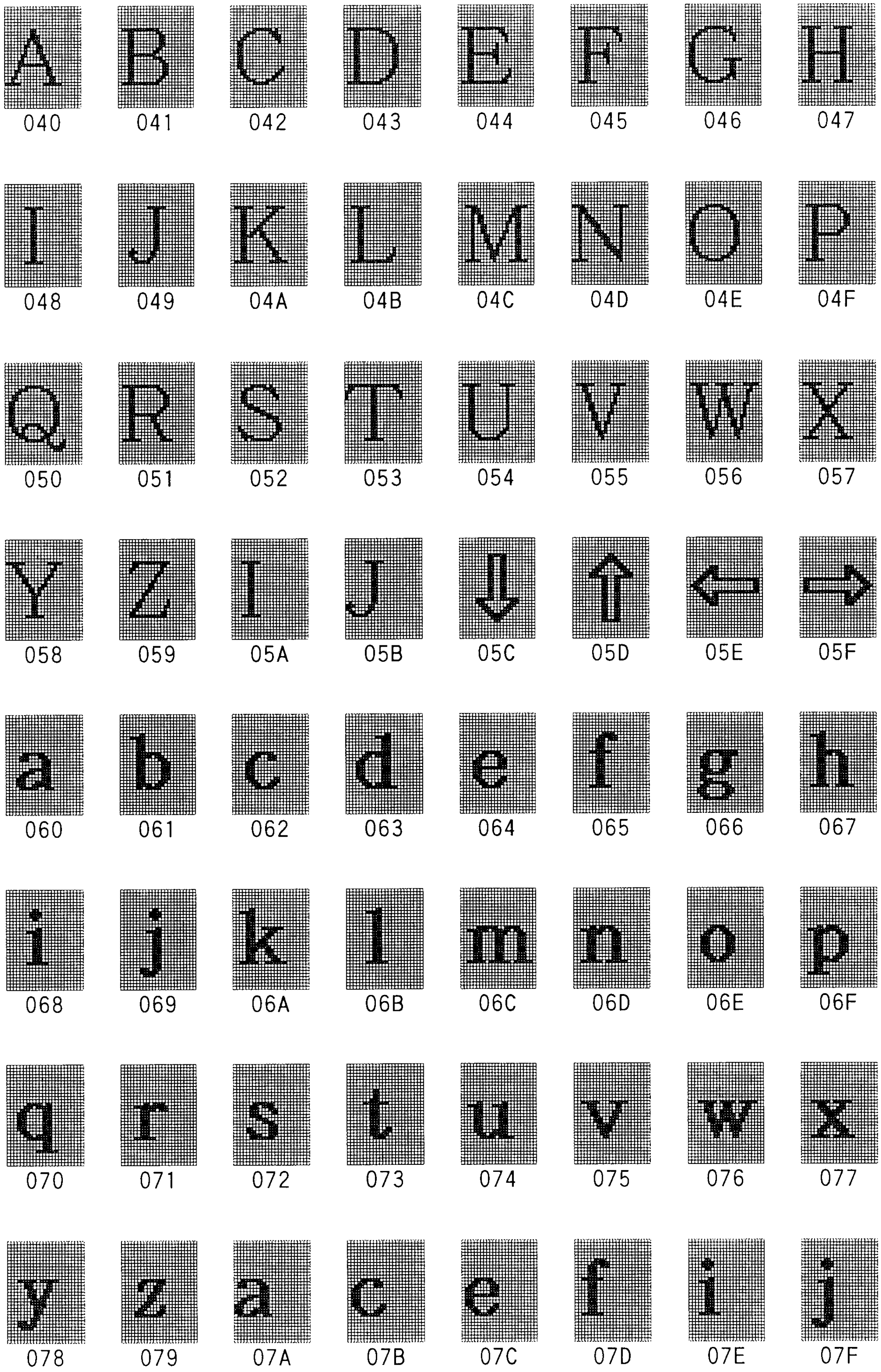
This function sets the command ROM transfer end address 2.

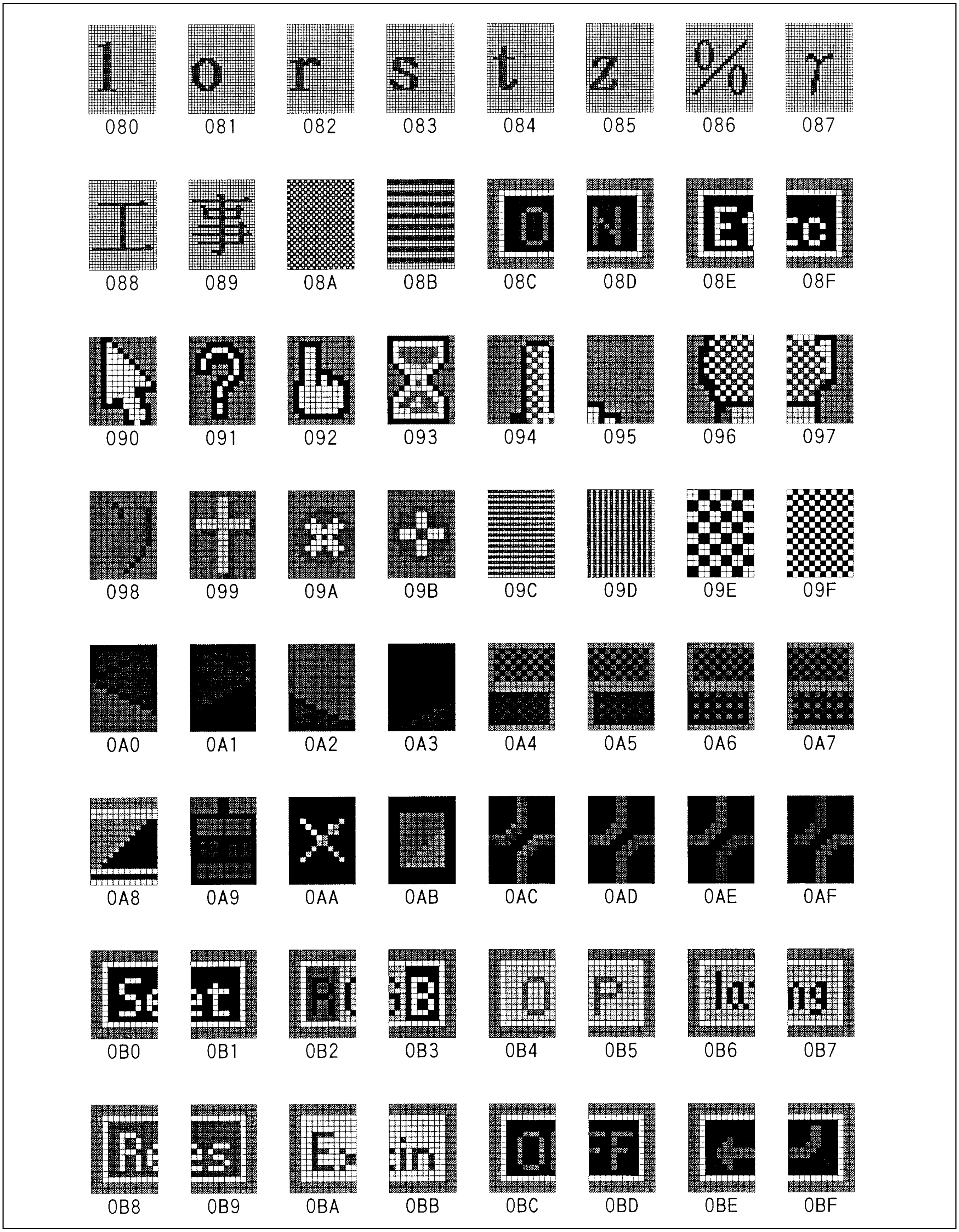
[Additional Information]
- This function determines the lower address value of the ending address for command ROM transfer.
- When the command ROM transfer synchronization control bit is on (TSV = 1) , command ROM transfer is activated and executed synchronously with the detection of the vertical sync signal.
- When the command ROM transfer synchronization control bit is off (TSV = 0) , command ROM transfer is activated and executed with the issuance of this command.

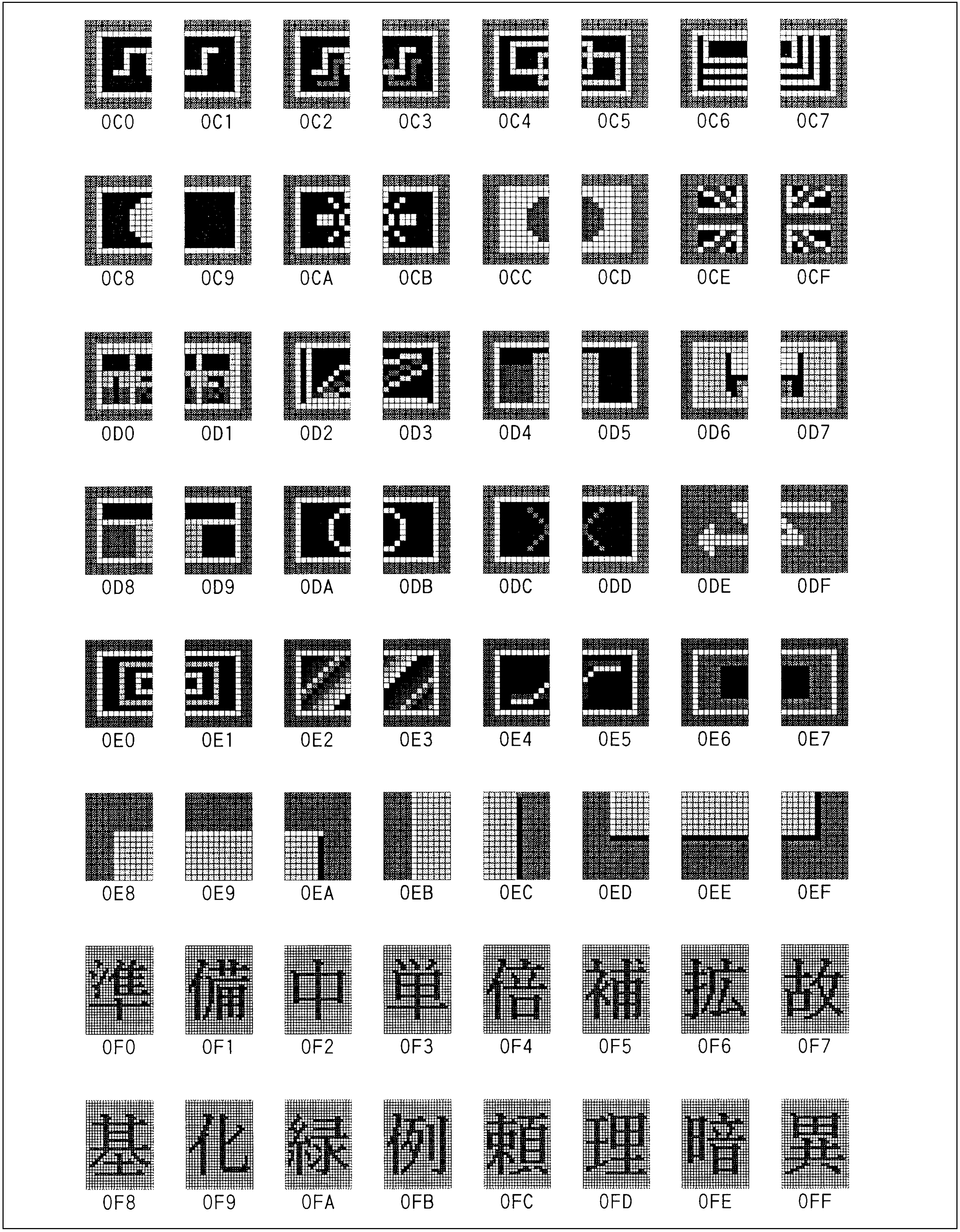
■ CONTENTS OF MB90098A-001 (STANDARD PRODUCT) FONT DATA



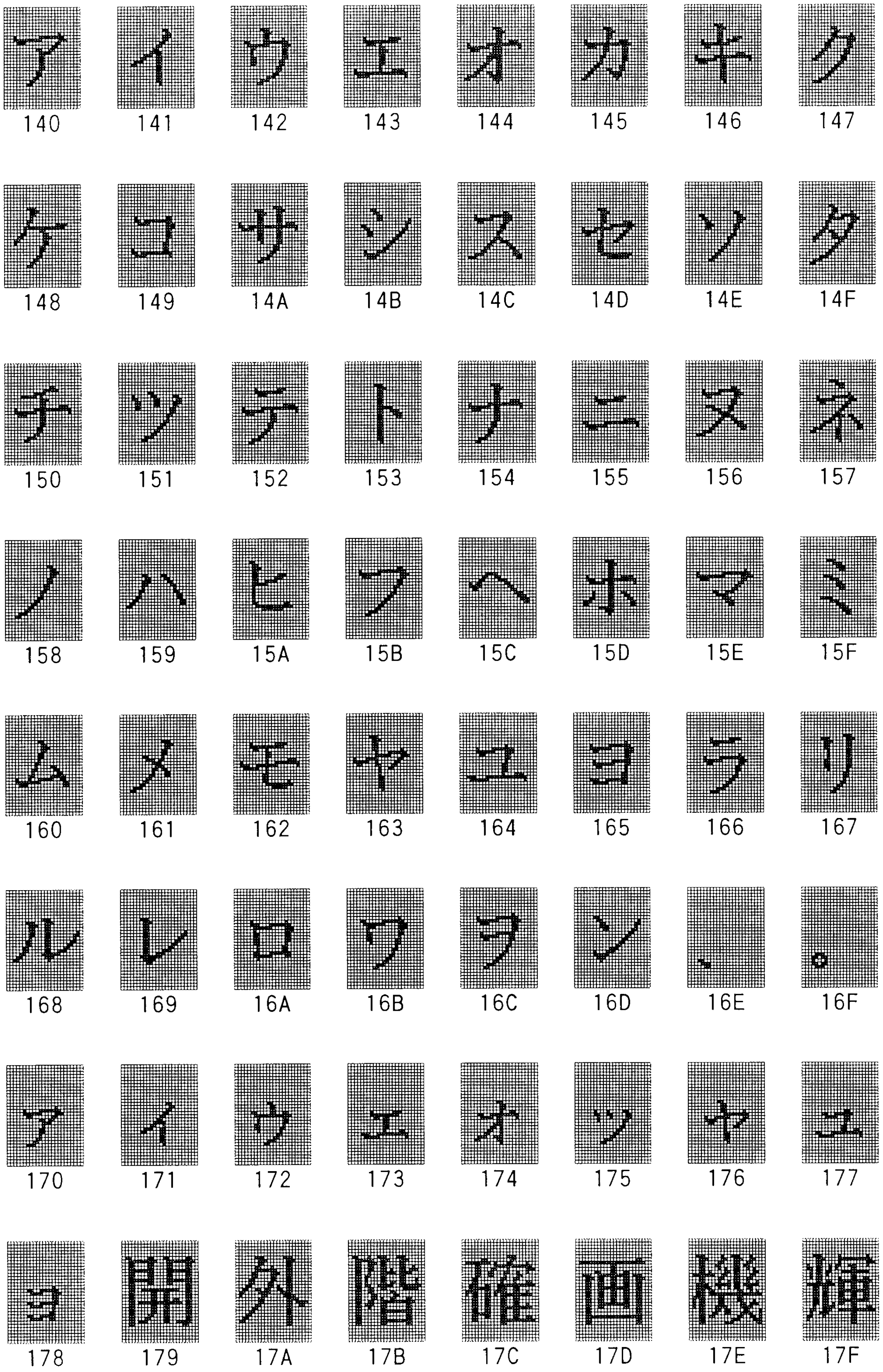
0	1	2	3	4	5	6	7
000	001	002	003	004	005	006	007
8	9	:	!	?	.	,	’
008	009	00A	00B	00C	00D	00E	00F
0	1	2	3	4	5	6	7
010	011	012	013	014	015	016	017
8	9	+	−	*	/	(	)
018	019	01A	01B	01C	01D	01E	01F
A	B	C	D	E	F	G	H
020	021	022	023	024	025	026	027
I	J	K	L	M	N	O	P
028	029	02A	02B	02C	02D	02E	02F
Q	R	S	T	U	V	W	X
030	031	032	033	034	035	036	037
Y	Z	I	J	I	#	=	~
038	039	03A	03B	03C	03D	03E	03F


A 040
B 041
C 042
D 043
E 044
F 045
G 046
H 047
I 048
J 049
K 04A
L 04B
M 04C
N 04D
O 04E
P 04F
Q 050
R 051
S 052
T 053
U 054
V 055
W 056
X 057
Y 058
Z 059
I 05A
J 05B
⇩ 05C
⇧ 05D
⇦ 05E
⇨ 05F
a 060
b 061
c 062
d 063
e 064
f 065
g 066
h 067
i 068
j 069
k 06A
l 06B
m 06C
n 06D
o 06E
p 06F
q 070
r 071
s 072
t 073
u 074
v 075
w 076
x 077
y 078
z 079
a 07A
c 07B
e 07C
f 07D
i 07E
j 07F


080
081
082
083
084
085
086
087
088
089
08A
08B
08C
08D
08E
08F
090
091
092
093
094
095
096
097
098
099
09A
09B
09C
09D
09E
09F
0A0
0A1
0A2
0A3
0A4
0A5
0A6
0A7
0A8
0A9
0AA
0AB
0AC
0AD
0AE
0AF
0B0
0B1
0B2
0B3
0B4
0B5
0B6
0B7
0B8
0B9
0BA
0BB
0BC
0BD
0BE
0BF


0C0
0C1
0C2
0C3
0C4
0C5
0C6
0C7
0C8
0C9
0CA
0CB
0CC
0CD
0CE
0CF
0D0
0D1
0D2
0D3
0D4
0D5
0D6
0D7
0D8
0D9
0DA
0DB
0DC
0DD
0DE
0DF
0E0
0E1
0E2
0E3
0E4
0E5
0E6
0E7
0E8
0E9
0EA
0EB
0EC
0ED
0EE
0EF
準
0F0
備
0F1
中
0F2
単
0F3
倍
0F4
補
0F5
拡
0F6
故
0F7
基
0F8
化
0F9
緑
0FA
例
0FB
頼
0FC
理
0FD
暗
0FE
異
0FF

あ	い	う	え	お	か	き	く
100	101	102	103	104	105	106	107
け	こ	さ	し	す	せ	そ	た
108	109	10A	10B	10C	10D	10E	10F
ち	つ	て	と	な	に	ぬ	ね
110	111	112	113	114	115	116	117
の	は	ひ	ふ	へ	ほ	ま	み
118	119	11A	11B	11C	11D	11E	11F
む	め	も	や	ゆ	よ	ら	り
120	121	122	123	124	125	126	127
る	れ	ろ	わ	を	ん	゛	゜
128	129	12A	12B	12C	12D	12E	12F
ぁ	ぃ	ぅ	ぇ	ぉ	っ	ゃ	ゅ
130	131	132	133	134	135	136	137
ょ	移	囲	右	可	押	横	解
138	139	13A	13B	13C	13D	13E	13F


ア 140
イ 141
ウ 142
エ 143
オ 144
カ 145
キ 146
ク 147
ケ 148
コ 149
サ 14A
シ 14B
ス 14C
セ 14D
ソ 14E
タ 14F
チ 150
ツ 151
テ 152
ト 153
ナ 154
ニ 155
ヌ 156
ネ 157
ノ 158
ハ 159
ヒ 15A
フ 15B
ヘ 15C
ホ 15D
マ 15E
ミ 15F
ム 160
メ 161
モ 162
ヤ 163
ユ 164
ヨ 165
ラ 166
リ 167
ル 168
レ 169
ロ 16A
ワ 16B
ヲ 16C
ン 16D
、 16E
。 16F
ァ 170
ィ 171
ゥ 172
ェ 173
ォ 174
ッ 175
ャ 176
ュ 177
ョ 178
開 179
外 17A
階 17B
確 17C
画 17D
機 17E
輝 17F

依	位	意	英	検	現	言	期
180	181	182	183	184	185	186	187
規	景	語	源	格	向	在	下
188	189	18A	18B	18C	18D	18E	18F
号	行	高	合	項	黒	供	給
190	191	192	193	194	195	196	197
左	止	再	最	作	始	仕	示
198	199	19A	19B	19C	19D	19E	19F
自	告	警	縞	修	手	周	終
1A0	1A1	1A2	1A3	1A4	1A5	1A6	1A7
障	縦	除	出	初	順	奨	小
1A8	1A9	1AA	1AB	1AC	1AD	1AE	1AF
上	常	状	場	色	信	垂	推
1B0	1B1	1B2	1B3	1B4	1B5	1B6	1B7
水	数	正	整	青	設	赤	素
1B8	1B9	1BA	1BB	1BC	1BD	1BE	1BF

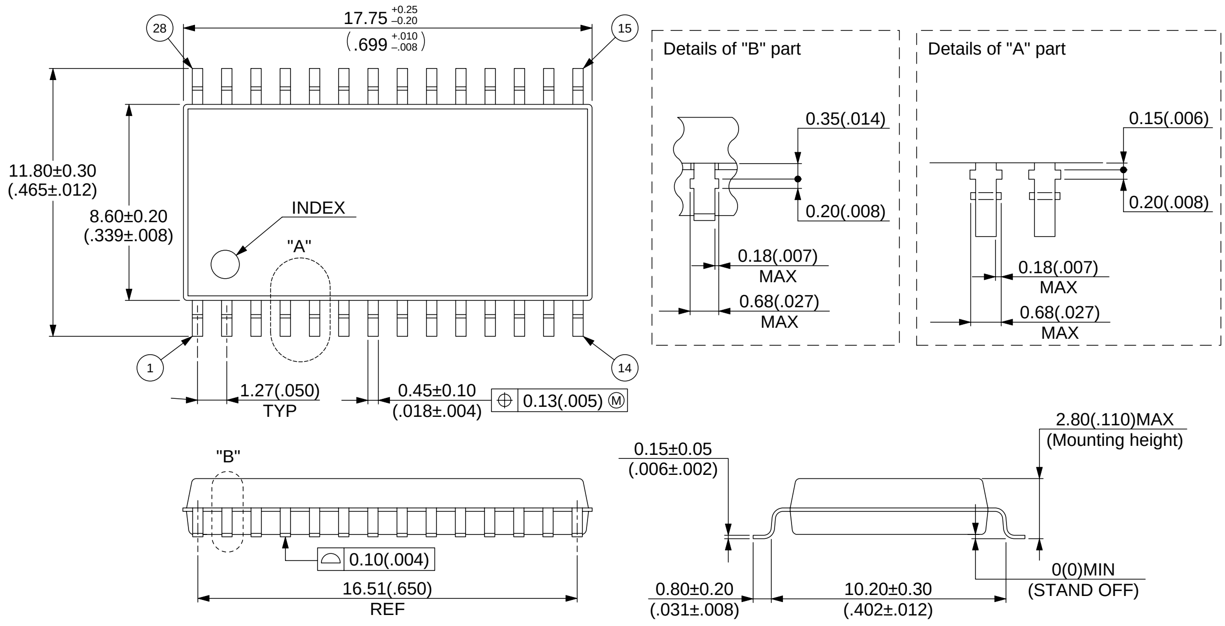
選 1C0	節 1C1	接 1C2	切 1C3	全 1C4	操 1C5	像 1C6	側 1C7
続 1C8	相 1C9	他 1CA	替 1CB	態 1CC	大 1CD	直 1CE	内 1CF
断 1D0	知 1D1	値 1D2	置 1D3	択 1D4	調 1D5	停 1D6	低 1D7
定 1D8	的 1D9	点 1DA	電 1DB	注 1DC	度 1DD	張 1DE	動 1DF
同 1E0	灯 1E1	日 1E2	入 1E3	認 1E4	能 1E5	波 1E6	白 1E7
背 1E8	範 1E9	微 1EA	必 1EB	表 1EC	部 1ED	平 1EE	不 1EF
方 1F0	法 1F1	変 1F2	本 1F3	万 1F4	明 1F5	面 1F6	模 1F7
滅 1F8	目 1F9	容 1FA	様 1FB	要 1FC	力 1FD	了 1FE	1FF

■ ORDERING INFORMATION

Part Number	Package	Remarks
MB90098APF	28-pin plastic SOP (FPT-28P-M17)	

■ PACKAGE DIMENSION

28-pin plastic SOP
(FPT-28P-M17)



17.75 +0.25 −0.20
(.699 +.010 −.008)
28
15
1
14
11.80±0.30
(.465±.012)
8.60±0.20
(.339±.008)
INDEX
"A"
1.27(.050)
TYP
0.45±0.10
(.018±.004)
0.13(.005) Ⓜ
Details of "B" part
0.35(.014)
0.20(.008)
0.18(.007)
MAX
0.68(.027)
MAX
Details of "A" part
0.15(.006)
0.20(.008)
0.18(.007)
MAX
0.68(.027)
MAX
"B"
0.10(.004)
16.51(.650)
REF
0.15±0.05
(.006±.002)
2.80(.110)MAX
(Mounting height)
0.80±0.20
(.031±.008)
10.20±0.30
(.402±.012)
0(0)MIN
(STAND OFF)

© 2000 FUJITSU LIMITED F28048S-1C-2

Dimensions in mm (inches)

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information and circuit diagrams in this document are presented as examples of semiconductor device applications, and are not intended to be incorporated in devices for actual use. Also, FUJITSU is unable to assume responsibility for infringement of any patent rights or other rights of third parties arising from the use of this information or circuit diagrams.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

F0106
© FUJITSU LIMITED Printed in Japan