

8-bit Proprietary Microcontrollers

CMOS

F²MC-8L MB89051 Series

MB89F051/MB89051

■ DESCRIPTION

The MB89051 series is a general-purpose, single-chip microcontroller that features a compact instruction set and contains a range of peripheral function set and timers, serial interface, a PWM timer, the USB hub function and the USB function. The USB hub function, in particular, supports five down ports (one of them is dedicated to an internal function) allowing them to interface with other USB devices. The microcontrollers also contain one USB function channel to support full speed.

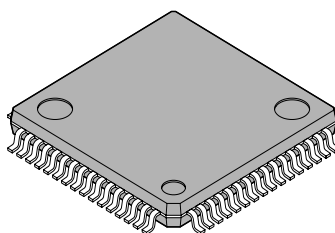
■ FEATURES

- Package type
64-pin LQFP Package (0.65 mm pitch)
- High-speed operations at low voltage
Minimum execution time : 0.33 μ s (Automatically generates a 12 MHz main clock and a 48 MHz USB interface synchronization clock with an externally supplied 6 MHz clock and the internal PLL circuit.)

(Continued)

■ Package

64-pin plastic LQFP



(FPT-64P-M09)

MB89051 Series

- F²MC-8L CPU core
Instruction set that is optimum to the controllers
 - Multiplication and division instructions
 - 16-bit arithmetic operations
 - branch instructions by bit testing
 - bit manipulation instructions, etc.
- PLL clock control
The internal PLL clock circuit allows the use of low-speed clocks which are advantageous to noise characteristics.
(6 MHz externally-supplied clock→12 MHz internal system clock)
- Various timers
8-bit PWM timer (can be used as either 8-bit PWM timer 2 channels or PPG timer 1 channel)
Internal 21-bit timebase timer
- Internal USB transceiver circuit (Compatible with full and low speeds)
- USB hub
USB function Compliant to USB Protocol Revision 1.0
Five downstream port channels (One of these channels is dedicated to a function.)
Automatically responds to all USB protocols by hardware.
Descriptor configuration is provided as ROM data for automatic responding by hardware (Vender ID and product ID) .
String data is not supported.
Allows switching between BUS power supply and own power supply mode.
Power supply to the USB down port is controlled port by port.
- USB function
USB function Compliant to USB Protocol Revision 1.0
Support for full speed when using hub
Support for both low and full speeds when using function
Allows four endpoints to be specified at maximum.
Types of transfer supported: control/interrupt/bulk/isochronous
Built-in DMAC (Maps the buffer for each endpoint on to the internal RAM to directly access the memory for function's send and receive data.)
- UART/SIO, SIO Serial Interface
Built-in UART/SIO function (selectable by switching) × 1 channel
Built-in SIO (3.3 V) × 2 channels
- I²C interface*¹
Supports Philips I²C bus standards
Uses a two-wire data transfer protocol
Master/slave send/receive
- External interrupt
External interrupt (level detection × 7 channels)
Seven inputs are independent of one another and can also be used for resetting from low-power consumption mode (the L-level detection feature available) .
- Clock output functions
Able for 12 MHz*² and 6 MHz*² clocks to output. (dedicated pins, 3 V)
- Low power consumption (standby mode supported)
Stop mode (There is almost no current consumption since oscillation stops.)
Sleep mode (This mode stops the running CPU.)

(Continued)

(Continued)

- A maximum of 41 general-purpose I/O ports
General-purpose I/O ports (CMOS) : 37 (7 of 3 V ports)
General-purpose I/O ports (Nch open drain) : 4
- Power supply
Supply voltage: 3.3 V \pm 0.3 V or 5.0 V \pm 0.5 V
- Operating temperature
 $T_A = -40^\circ$ to $+85^\circ\text{C}$ (When the USB function is not in use.)
 $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$ (When the USB function is in use.)

*1 : I²C license

The customer is licensed to use Philips I²C patent when using this product in an I²C system that complies with the Philips I²C standard specifications.

*2 : When an external supply clock is at 6 MHz.

MB89051 Series

■ PRODUCT LINEUP

| Part number | | MB89051 | MB89F051 |
|----------------------|----------------------------|---|--|
| Parameter | | | |
| ROM size | | 32 KB | 32 KB (FLASH) |
| RAM size | | 2 KB | |
| Package | | LQFP-64 (FPT-64P-M09) | |
| Others | | MASK product | FLASH product/EVA product |
| CPU functions | | Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum execution time : 0.33 μ s (6 MHz) Interrupt processing time : 3 μ s (6 MHz) | |
| Peripheral functions | General-purpose ports | | General purpose I/O ports (37 : CMOS (7 of 3 V ports) , 4 : Nch open drain) |
| | USB hub | | Upstream port : 1 channel Downstream port : 5 channels (One is dedicated to an internal function.) Port power supply control method : By individual port Allows selection between own power supply and bus power supply |
| | USB function | | Supports full speed : when using hub Supports full and low speeds : when using function End point max 4 Built-in DMAC (Can be set to DMA transfer to the internal RAM) |
| | PWM timer | | 8-bit PWM timer operation 2 channels (can also be used as a PPG 1 channel timer) |
| | UART | SIO | Allows switching between UART (clock-synchronous/asynchronous data transfer allowed) and SIO (simple serial transfer). |
| | SIO | | SIO (simple serial) \times 2 channels (3 V) |
| | I ² C interface | | One channel. Supports Phillips I ² C bus standards. Uses a 2-wire protocol for communications with other devices. |
| | Timebase timer | | 21-bit timebase timer |
| | Clock output | | Allows clock output of 12 MHz* and 6 MHz* (3 V) |
| Standby mode | | Sleep mode and Stop mode | |

* : When external supply clock is at 6 MHz.

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

- Before evaluating using the FLASH product, it is necessary to confirm its differences from the product that will actually be used.

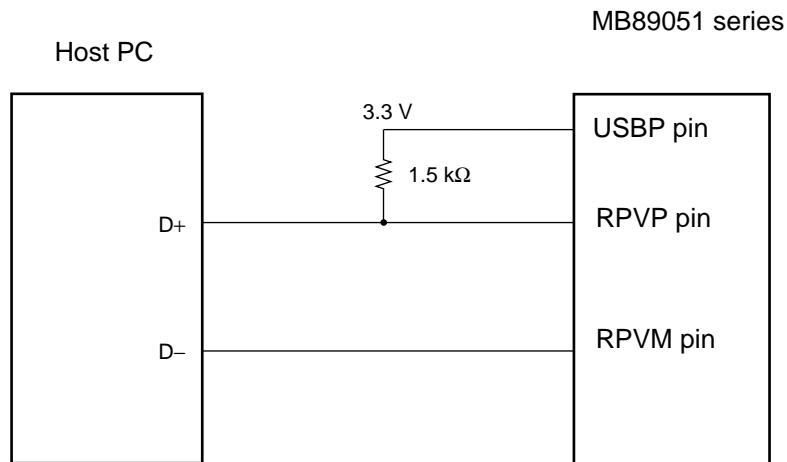
2. Current Consumption

- When operating at low speed, FLASH products will consume more current than mask ROM products. However, in sleep/stop mode the current consumption is the same.
- For detailed information on each package, see “■ PACKAGE DIMENSIONS”

3. USB Pull-up Resistor control

- Remains in high impedance state until USB connection take place. Before the USB connection, use USBP pin output to control pull-up resistance by software.

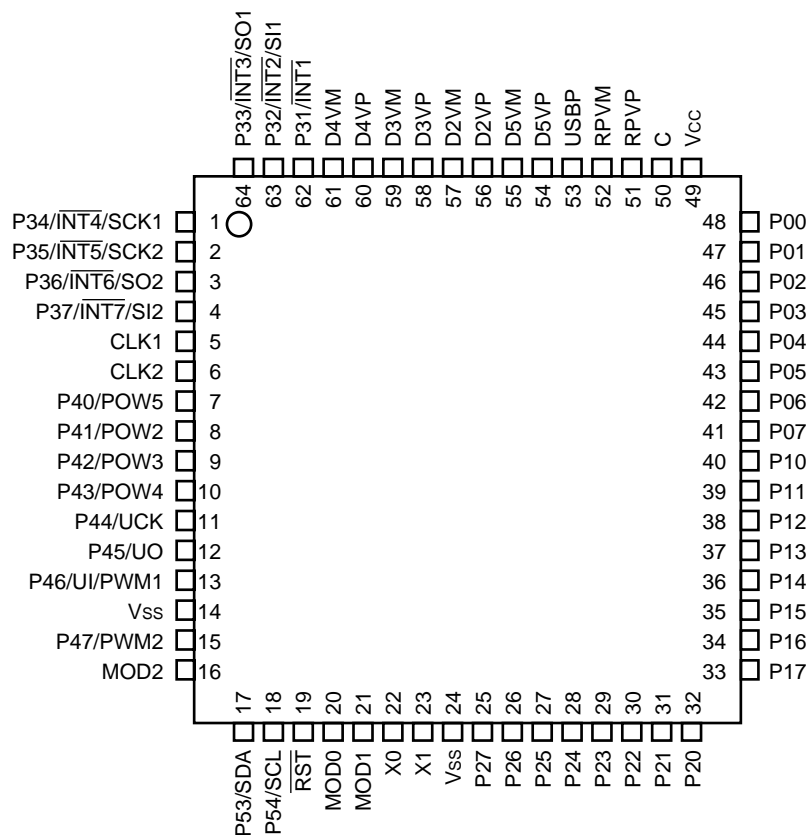
- The example of connection



MB89051 Series

PIN ASSIGNMENT

(TOP VIEW)



(FPT-64P-M09)

■ PIN DESCRIPTION

| Pin No. | Pin name | Circuit type | Function |
|---------|-------------------------------------|--------------|--|
| 1 | P34/ $\overline{\text{INT4}}$ /SCK1 | E | General-purpose CMOS I/O pin The external interrupt input is a hysteresis input. (Level detection) SIO1 clock I/O |
| 2 | P35/ $\overline{\text{INT5}}$ /SCK2 | E | General-purpose CMOS I/O pin The external interrupt input is a hysteresis input. (Level detection) SIO2 clock I/O |
| 3 | P36/ $\overline{\text{INT6}}$ /SO2 | B | General-purpose CMOS I/O pin The external interrupt input is a hysteresis input. (Level detection) SIO2 serial data output |
| 4 | P37/ $\overline{\text{INT7}}$ /SI2 | E | General-purpose CMOS I/O pin The external interrupt input is a hysteresis input. (Level detection) SIO2 serial data input |
| 5 | CLK1 | M | 6 MHz clock output pin (When external supply clock is at 6 MHz.) |
| 6 | CLK2 | M | 12 MHz clock output pin (When external supply clock is at 6 MHz.) |
| 7 | P40/POW5 | B | General-purpose CMOS I/O pin This pin also serves as USB Down Port power control signal. |
| 8 | P41/POW2 | B | General-purpose CMOS I/O pin This pin also serves as USB Down Port power control signal. |
| 9 | P42/POW3 | B | General-purpose CMOS I/O pin This pin also serves as USB Down Port power control signal. |
| 10 | P43/POW4 | B | General-purpose CMOS I/O pin This pin also serves as USB Down Port power control signal. |
| 11 | P44/UCK | E | General-purpose CMOS I/O pin UART/S10 clock I/O |
| 12 | P45/UO | B | General-purpose CMOS I/O pin UART/S10 serial data output |
| 13 | P46/UI/ PWM1 | N | Nch open drain general-purpose I/O pin UART/S10 serial data input PWM timer |
| 14 | V _{SS} | — | Power supply pin (GND) |
| 15 | P47/PWM2 | K | Nch open drain general-purpose I/O pin PWM timer |
| 16 | MOD2 | F | An operating mode designation pin. Connect directly to V _{SS} . |
| 17 | P53/SDA | K | Nch open drain general-purpose I/O pin Also serve as I ² C interface data input/output pin. |
| 18 | P54/SCL | K | Nch open drain general-purpose I/O pin Also serve as I ² C interface clock input/output pin. |
| 19 | $\overline{\text{RST}}$ | I | Reset pin (Reset on the negative logic low level.) |
| 20 | MOD0 | F | An operating mode designation pin. Connect directly to V _{SS} . |
| 21 | MOD1 | F | An operating mode designation pin. Connect directly to V _{SS} . |

(Continued)

MB89051 Series

| Pin No. | Pin name | Circuit type | Function |
|---------|-----------------|--------------|--|
| 22 | X0 | A | Pins for the connection of crystal oscillation circuit.(6 MHz) |
| 23 | X1 | | |
| 24 | V _{ss} | — | Power supply pin (GND) |
| 25 | P27 | B | General-purpose CMOS I/O pin* |
| 26 | P26 | B | General-purpose CMOS I/O pin* |
| 27 | P25 | B | General-purpose CMOS I/O pin* |
| 28 | P24 | B | General-purpose CMOS I/O pin* |
| 29 | P23 | B | General-purpose CMOS I/O pin* |
| 30 | P22 | B | General-purpose CMOS I/O pin* |
| 31 | P21 | B | General-purpose CMOS I/O pin* |
| 32 | P20 | B | General-purpose CMOS I/O pin* |
| 33 | P17 | B | General-purpose CMOS I/O pin |
| 34 | P16 | B | General-purpose CMOS I/O pin |
| 35 | P15 | B | General-purpose CMOS I/O pin |
| 36 | P14 | B | General-purpose CMOS I/O pin |
| 37 | P13 | B | General-purpose CMOS I/O pin |
| 38 | P12 | B | General-purpose CMOS I/O pin |
| 39 | P11 | B | General-purpose CMOS I/O pin |
| 40 | P10 | B | General-purpose CMOS I/O pin |
| 41 | P07 | B | General-purpose CMOS I/O pin |
| 42 | P06 | B | General-purpose CMOS I/O pin |
| 43 | P05 | B | General-purpose CMOS I/O pin |
| 44 | P04 | B | General-purpose CMOS I/O pin |
| 45 | P03 | B | General-purpose CMOS I/O pin |
| 46 | P02 | B | General-purpose CMOS I/O pin |
| 47 | P01 | B | General-purpose CMOS I/O pin |
| 48 | P00 | B | General-purpose CMOS I/O pin |
| 49 | V _{cc} | — | Power supply pin. |
| 50 | C | — | Connect an external capacitor of 0.1 μ F. When using with 3.3 V power supply, connect this pin with the V _{cc} pin to set to 3.3 V input. |
| 51 | RPVP | USBDRV | USB route port + pin |
| 52 | RPVM | USBDRV | USB router port – pin |
| 53 | USBP | L | USB pull-up resistance connection pin. |
| 54 | D5VP | USBDRV | USB down port 5 + pin |
| 55 | D5VM | USBDRV | USB down port 5 – pin |

* : For output only on the emulator.

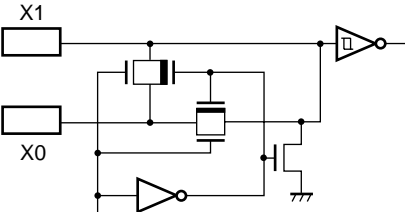
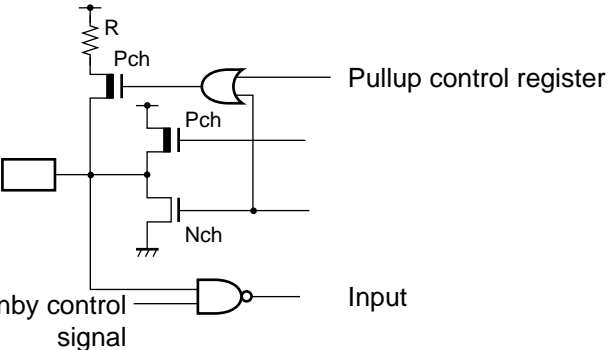
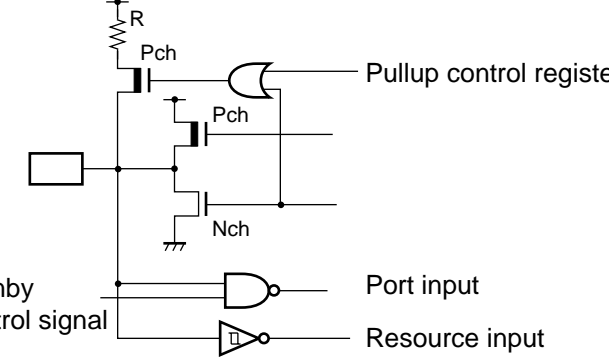

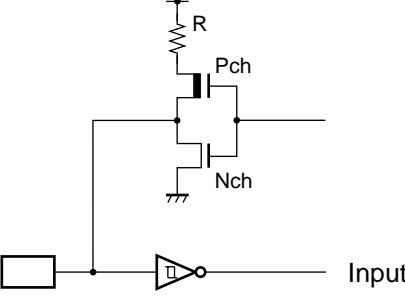
(Continued)

(Continued)

| Pin No. | Pin name | Circuit type | Function |
|---------|------------------------------------|--------------|---|
| 56 | D2VP | USBDRV | USB down port 2 + pin |
| 57 | D2VM | USBDRV | USB down port 2 – pin |
| 58 | D3VP | USBDRV | USB down port 3 + pin |
| 59 | D3VM | USBDRV | USB down port 3 – pin |
| 60 | D4VP | USBDRV | USB down port 4 + pin |
| 61 | D4VM | USBDRV | USB down port 4 – pin |
| 62 | P31/ $\overline{\text{INT1}}$ | B | General-purpose CMOS I/O pin External interrupt input (Hysteresis input (level detection)) |
| 63 | P32/ $\overline{\text{INT2}}$ /SI1 | E | General-purpose CMOS I/O pin External interrupt input (Hysteresis input (level detection)) SIO1 serial data input |
| 64 | P33/ $\overline{\text{INT3}}$ /SO1 | B | General-purpose CMOS I/O pin External interrupt input (Hysteresis input (level detection)) SIO1 serial data output |

MB89051 Series

■ I/O CIRCUIT TYPE

| Type | Circuit | Remarks |
|------|--|--|
| A |  <p>Standby control signal</p> | <ul style="list-style-type: none"> Oscillation feedback resistance : 1 MΩ approx. |
| B |  <p>Pullup control register</p> <p>Standby control signal</p> <p>Input</p> | <ul style="list-style-type: none"> CMOS I/O |
| E |  <p>Pullup control register</p> <p>Standby control signal</p> <p>Port input</p> <p>Resource input</p> | <ul style="list-style-type: none"> CMOS I/O Hysteresis input |
| F |  <p>Input</p> | <ul style="list-style-type: none"> CMOS input |
| I |  <p>Input</p> | <ul style="list-style-type: none"> Hysteresis I/O Pullup resistance |

(Continued)

(Continued)

| Type | Circuit | Remarks |
|--------|---|--|
| USBDVR | <p>The diagram shows a USBDRV circuit. It has two input pins labeled D+ and D-. These are connected to a network of logic gates. The D+ input is connected to a buffer (D+ input), an inverter (D- input), a differential input (Differential input), a full D+ output (Full D+ output), a full D- output (Full D- output), a low D+ output (Low D+ output), and a low D- output (Low D- output). The D- input is connected to a buffer (D- input), an inverter (D+ input), a differential input (Differential input), a full D+ output (Full D+ output), a full D- output (Full D- output), a low D+ output (Low D+ output), and a low D- output (Low D- output). The direction signal (Direction) is connected to an AND gate. The speed signal (Speed) is connected to an OR gate.</p> | <ul style="list-style-type: none"> • USB I/O |
| K | <p>The diagram shows a circuit for type K. It has a standby control signal input and an Nch transistor. The standby control signal is connected to the gate of the Nch transistor. The output of the Nch transistor is connected to an input pin.</p> | <ul style="list-style-type: none"> • Nch open drain I/O |
| L | <p>The diagram shows a circuit for type L. It has a Pch transistor and an Nch transistor. The Pch transistor is connected to a pull-up resistor. The Nch transistor is connected to the output of the Pch transistor.</p> | <ul style="list-style-type: none"> • USB pull-up resistance connection |
| M | <p>The diagram shows a circuit for type M. It has a Pch transistor and an Nch transistor. The Pch transistor is connected to a clock output signal. The Nch transistor is connected to the output of the Pch transistor.</p> | <ul style="list-style-type: none"> • Clock output |
| N | <p>The diagram shows a circuit for type N. It has a standby control signal input and an Nch transistor. The standby control signal is connected to the gate of the Nch transistor. The output of the Nch transistor is connected to a port input (Port input) and a resource input (Resource input).</p> | <ul style="list-style-type: none"> • Nch open drain I/O • Hysteresis input |

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{cc} or lower than V_{ss} is applied to input or output pins other than the medium- and high-voltage pins or if voltage higher than the rating is applied between V_{cc} and V_{ss} .

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also take care to prevent the analog input from exceeding the digital power supply (V_{cc}) when the power supply to the analog power system is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions and latchup leading to permanent damage to the pins. These unused pins should be connected to a pullup or pulldown resistance of at least $2\text{ k}\Omega$ between the pin and the power supply.

Unused I/O pins should be placed in output state to leave it open or pins that are in input state should be handled the same as unused input pins.

3. Note to noise in the External Reset Pin (\overline{RST})

If the reset pulse applied to the external reset pin (\overline{RST}) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin (\overline{RST}).

4. Power Supply Voltage Fluctuations

Although V_{cc} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{cc} ripple fluctuations (P-P value) will be less than 10% of the standard V_{cc} value at the commercial frequency (50 Hz to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Note on the clock during operation

This microcontroller uses a PLL for generating the main clock signal. If the oscillator is removed or the clock input stops during operation, therefore, the microcontroller may keep on operating at the free-running frequency of the self-oscillation circuit in the PLL. The operation is not however guaranteed.

6. About port 2 (P20 to P27)

Port 2 serves as an output-only terminal on the emulator.

■ PROGRAMMING AND ERASING FLSH MEMORY

1. Flash Memory

The flash memory is located between 8000_H and FFFF_H in the CPU memory map and incorporates a flash memory interface circuit that allows read access and program access from the CPU to be performed in the same way as mark ROM. Programming and erasing flash memory is also performed via the flash memory interface circuit by executing instructions in the CPU. This enables the flash memory to be updated in place under the control of the CPU, providing an efficient method of updating program and data.

2. Flash Memory Features

- 32 Kbyte × 8-bit configuration (16 K + 8 K + 8 K sectors)
- Automatic programming algorithm (Embedded Algorithm* : Equivalent to MBM29LV200)
- Includes an erase pause and restart function
- Data polling and toggle bit for detection of program/erase completion
- Detection of program/erase completion via CPU interrupt
- Compatible with JEDEC-standard command
- Sector Protection (sectors can be combined in any combination)
- No. of program/erase cycles : 10,000 (Min)

* : Embedded Algorithm is a trademark of Advanced Micro Devices.

3. Procedure for Programming and Erasing Flash Memory

Programming and reading flash memory cannot be performed at the same time. Accordingly, to program or erase flash memory, the program must first be copied from flash memory to RAM so that programming can be performed without program access from flash memory.

4. Flash Memory Register

- Control status register (FMCS)

| Address | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 | Initial value |
|---------|------|--------|------|------|-----------|-----------|------|-----------|---------------|
| 002EH | INTE | RDYINT | WE | RDY | Re-served | Re-served | — | Re-served | 000X00X0B |
| | R/W | R/W | R/W | R | R/W | R/W | — | R/W | |

5. Sector Configuration

The table below shows the sector configuration of flash memory and lists the addresses of each sector for both during CPU access and a flash memory programming.

- Sector configuration of flash memory

| Flash Memory | CPU Address | Programmer Address* |
|--------------|--|--|
| 16 Kbytes | FFFF _H to C000 _H | 1FFFF _H to 1C000 _H |
| 8 Kbytes | BFFF _H to A000 _H | 1BFFF _H to 1A000 _H |
| 8 Kbytes | 9FFF _H to 8000 _H | 19FFF _H to 18000 _H |

* : Programmer address

The programmer address is the address to be used instead of the CPU address when programming data from a parallel flash memory programmer. Use the programmer address on programming or erasing using a general-purpose parallel programmer.

MB89051 Series

6. ROM Programmer Adaptor and Recommended ROM Programmers

| Package | Compatible adapter | Compatible programmers and models |
|-------------|-----------------------|--|
| | Sunhayato Corp. | Ando Denki K.K. |
| FPT-64P-M09 | FLASH-64QF2-32DP-8LF3 | AF9708 (ver 1.60 or higher) AF9709 (ver 1.60 or higher) |

- Inquiry:

Sunhayato Corp.

: TEL : 81-3-3984-7791

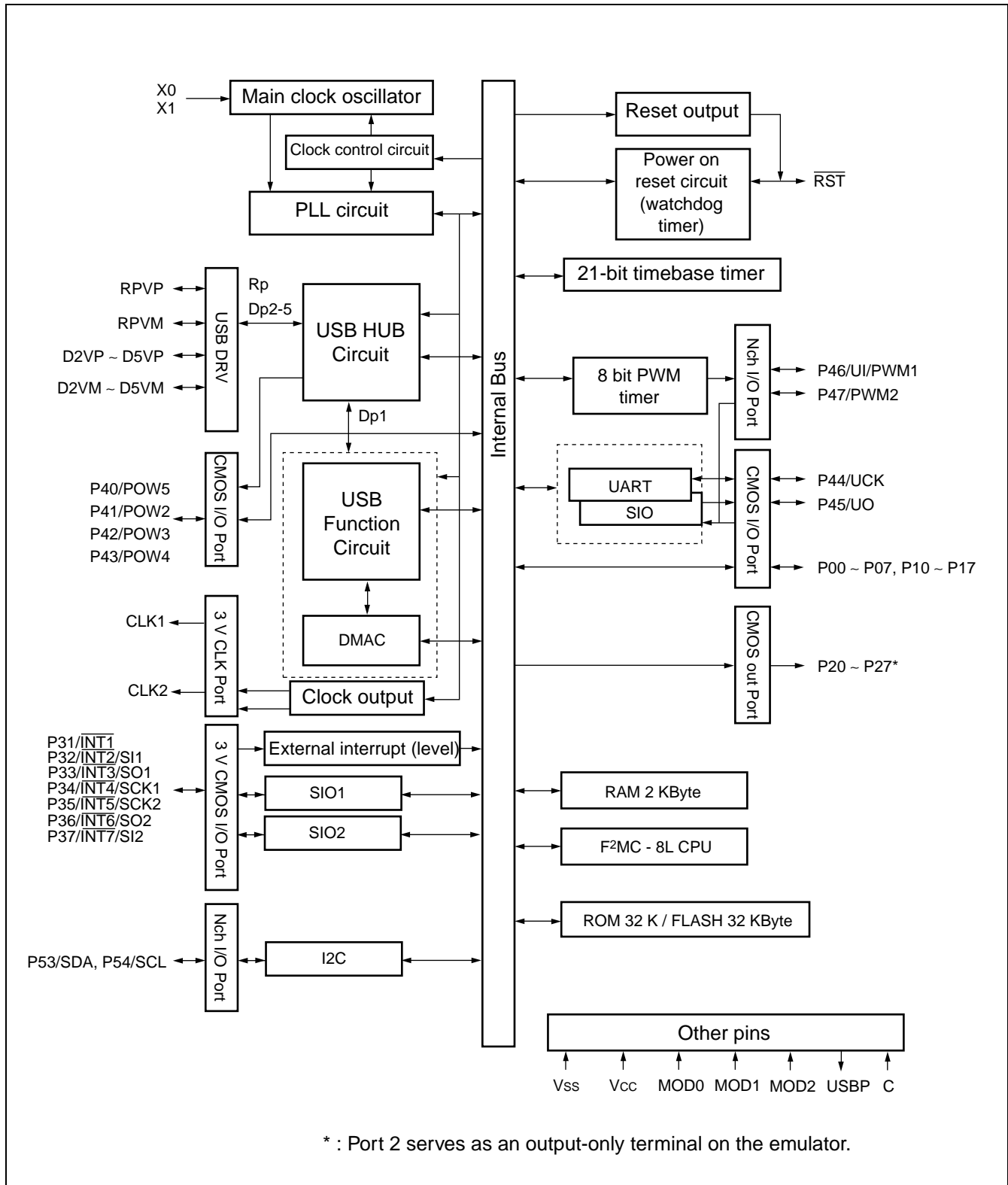
FAX : 81-3-3971-0535

E-mail : adapter@sunhayato.co.jp

Ando Denki K. K.

: TEL : 81-3-3733-1160

■ BLOCK DIAGRAM



MB89051 Series

■ CPU CORE

1. Memory Size

The MB89051 microcontroller offers a memory space of 64 Kbytes consisting of the I/O, RAM and ROM areas. The memory space contains areas that are used for specific purposes, such as a general-purpose register and a vector table.

- I/O area (addresses: 0000H through 007FH)

This area is assigned with the control and data registers, for example, of peripheral functions to be built in.

The I/O area is as accessible as the memory since the area is assigned to a part of the memory space. Direct addressing also allows the area to be accessed faster.

- RAM area

As an internal data area, a static RAM is built in.

The internal RAM capacity varies with the product type.

The area 80H to FFH can be accessed at high speed with direct addressing.

The area 100H to 1FFH can be used a general-purpose register area. (The usable area is limited depending on the product.)

When reset, RAM data becomes undefined.

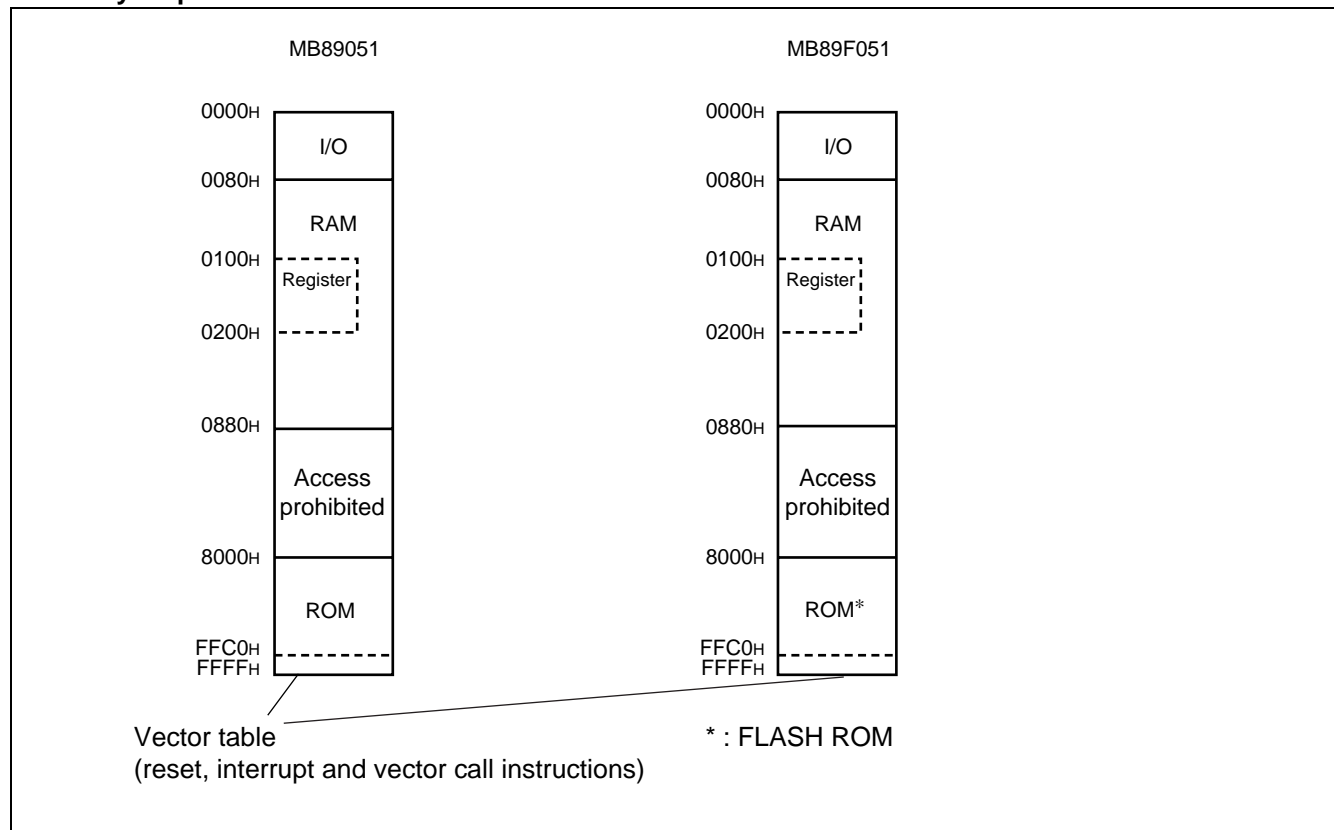
- ROM area

As an internal program area, a ROM is built in.

The internal RAM capacity varies with the product type.

The area FFC0H to FFFFH should be used for a vector table, for example.

• Memory map

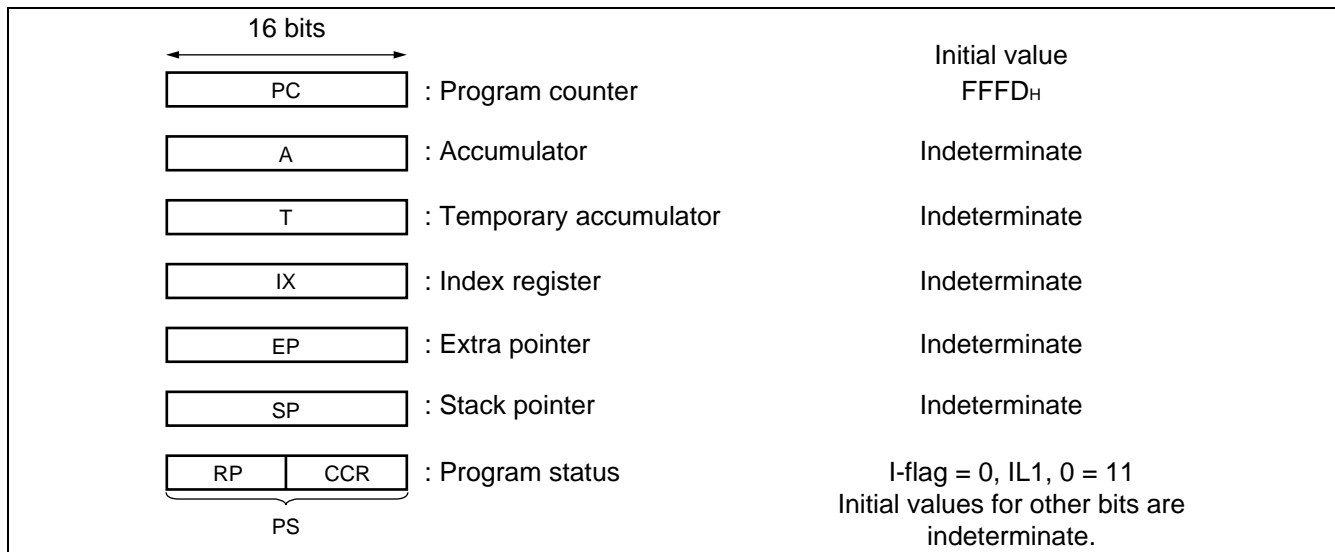


2. Registers

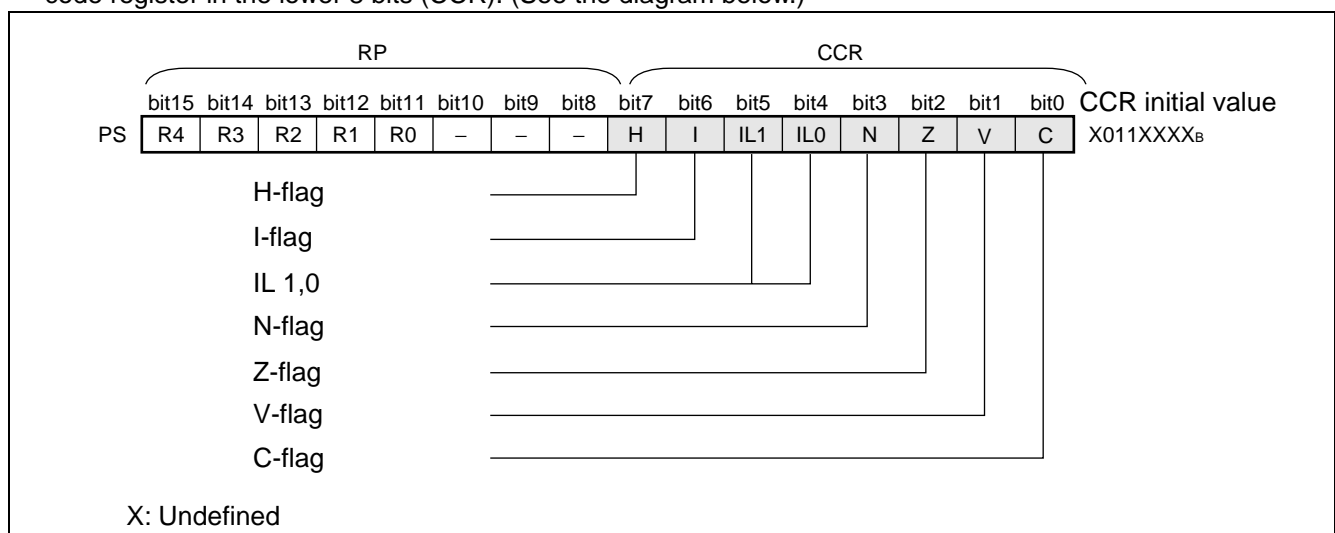
The MB89051 series has two types of registers; the registers dedicated to specific purposes in the CPU and the general-purpose registers.

The dedicated registers are as follows:

| | |
|---------------------------|--|
| Program counter (PC) | : A 16-bit register to indicate locations where instructions are stored. |
| Accumulator (A) | : A 16-bit register for temporary storage of operations. In the case of an 8-bit data processing instruction, the lower one byte is used. |
| Temporary accumulator (T) | : A 16-bit register which performs operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used. |
| Index register (IX) | : A 16-bit register for index modification. |
| Extra pointer (EP) | : A 16-bit register to point to a memory address. |
| Stack pointer (SP) | : A 16-bit register to indicate a stack area. |
| Program status (PS) | : A 16-bit register to store a register pointer or a condition code. |



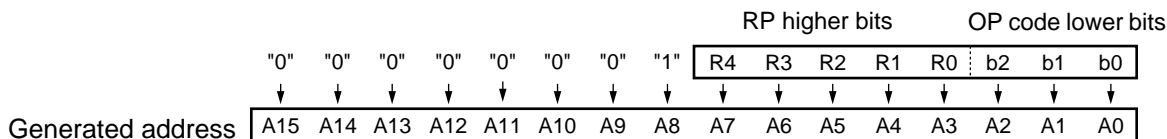
The PS register can further be divided into the register bank pointer in the higher 8 bits (RP) and the condition code register in the lower 8 bits (CCR). (See the diagram below.)



MB89051 Series

The RP points to the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule shown next.

Rule for Conversion of Actual Addresses in the General-purpose Register Area



The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at the time of an interrupt.

- H flag : The flag is set to "1" when an arithmetic operation results in a carry from bit 3 to bit 4 or in a borrow from bit 4 to bit 3. The bit is cleared to "0" in other instances. The flag is for decimal adjustment instructions; do not use for other than additions and subtractions.
- I flag : Interrupt is enabled when this flag is set to "1." Interrupt is disabled when this flag is set to "0." The flag is set to "0" when reset.
- IL1, 0 : Indicates the level of the interrupt currently enabled. An interrupt is processed only if its level is higher than the value this bit indicates.

| IL1 | IL0 | Interrupt level | High-low |
|-----|-----|-----------------|---|
| 0 | 0 | 1 | Higher ↑ ↓ Lower = no interruption |
| 0 | 1 | | |
| 1 | 0 | 2 | |
| 1 | 1 | 3 | |

- N flag : The flag is set to "1" when an arithmetic operation results in setting of the MSB to "1" or is cleared to "0" when the MSB is set to "1."
- Z flag : The flag is set to "1" when an arithmetic operation results in "0" or is set to "0" in other instances.
- V flag : The flag is set to "1" when an arithmetic operation results in two's complement overflow or is cleared to "0" if no overflow occurs.
- C flag : The flag is set to "1" when an arithmetic operation results in a carry from bit 7 or in a borrow to bit 7. The flag is cleared to "0" if neither of them occurs. In the case of a shift instruction, the flag is set to the shift-out value.

The following general-purpose registers are provided:

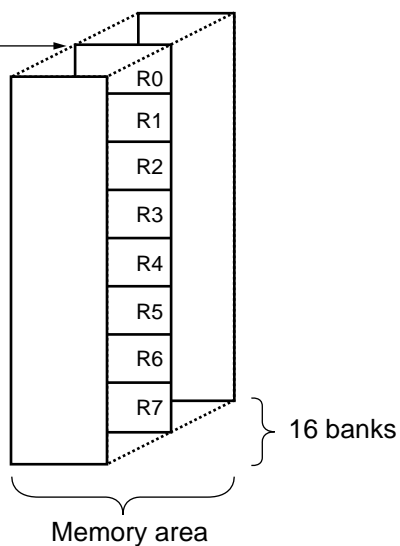
- General-purpose registers : 8-bit data storage registers

The general-purpose registers are 8 bits in length and located in the register banks in the memory. One bank contains eight registers and the MB89051 microcontrollers allow a total of 16 banks to be used at maximum.

The bank currently in use is indicated by the register bank pointer (RP).

Register Bank Configuration

This address = $0100_H + 8 \times (RP)$



MB89051 Series

■ I/O MAP

| Address | Register name | Register description | Read/write | Initial value |
|------------------------------------|---------------|---|------------|---------------|
| 00 _H | PDR0 | Port 0 data register | R/W | XXXXXXXX |
| 01 _H | DDR0 | Port 0 direction register | W | 00000000 |
| 02 _H | PDR1 | Port 1 data register | R/W | XXXXXXXX |
| 03 _H | DDR1 | Port 1 direction register | W | 00000000 |
| 04 _H | PDR2 | Port 2 data register | R/W | 00000000 |
| 05 _H | Reserved area | | | |
| 06 _H | DDR2 | Port 2 direction register | R/W | 00000000 |
| 07 _H | SYCC | System clock control register | R/W | XXX11X00 |
| 08 _H | STBC | Standby control register | R/W | 0001XXXX |
| 09 _H | WDTC | Watchdog timer control register | R/W | XXXXXXXX |
| 0A _H | TBTC | Timebase timer control register | R/W | 00XXX000 |
| 0B _H | Vacancy | | | |
| 0C _H | PDR3/USBP | Port 3 data register/Pull-up register for USB | R/W | XXXXXXXX |
| 0D _H | DDR3/USBPC | Port 3 data direction register/ Pull-up control register for USB | R/W | 00000000 |
| 0E _H | Reserved area | | | |
| 0F _H | Vacancy | | | |
| 10 _H | PDR4 | Port 4 data register | R/W | XXXXXXXX |
| 11 _H | DDR4 | Port 4 direction register | R/W | 00000000 |
| 12 _H | PDR5 | Port 5 data register | R/W | XXX11XXX |
| 13 _H to 15 _H | Reserved area | | | |
| 16 _H to 20 _H | Vacancy | | | |
| 21 _H | PURR0 | Port 0 pullup option setting register | R/W | 11111111 |
| 22 _H | PURR1 | Port 1 pullup option setting register | R/W | 11111111 |
| 23 _H | PURR2 | Port 2 pullup option setting register | R/W | 11111111 |
| 24 _H | PURR3 | Port 3 pullup option setting register | R/W | 1111111X |
| 25 _H | PURR4 | Port 4 pullup option setting register | R/W | 11111111 |
| 26 _H | Reserved area | | | |
| 27 _H | CTR1 | PWM control register 1 | R/W | 00000000 |
| 28 _H | CTR2 | PWM control register 2 | R/W | 000X0000 |
| 29 _H | CTR3 | PWM control register 3 | R/W | X000XXXX |
| 2A _H | CMR1 | PWM compare register 1 | W | XXXXXXXX |
| 2B _H | CMR2 | PWM compare register 2 | W | XXXXXXXX |
| 2C _H | CKR | Clock output control register | R/W | XXXXXXXX00 |
| 2D _H | SCS | Serial clock switching register | R/W | XXXXXXXX0 |

(Continued)

MB89051 Series

| Address | Register name | Register description | Read/write | Initial value |
|-----------------------------------|---------------|---|------------|-----------------|
| 2E _H | FMCS | Flash memory control status register (Only built-in Flash Memory products) | R, R/W | 0 0 0 X 0 0 X 0 |
| 2F _H | SMC1 | Serial mode control register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 30 _H | SMC2 | Serial mode control register 2 | R/W | 0 0 0 0 0 0 0 0 |
| 31 _H | SSD | Serial status and control register | R | 0 0 0 0 1 XXX |
| 32 _H | SIDR/SODR | Serial input/serial output data register | R/W | XXXXXXXX |
| 33 _H | SRC | Serial rate control register | R/W | XXXXXXXX |
| 34 _H | IBSR | I ² C bus status register | R | 0 0 0 0 0 0 0 0 |
| 35 _H | IBCR | I ² C bus control register | R/W | 0 0 0 1 1 0 0 0 |
| 36 _H | ICCR | I ² C clock regeister | R/W | 0 X 0 XXXXX |
| 37 _H | IADR | I ² C address register | R/W | XXXXXXXX |
| 38 _H | IDAR | I ² C data register | R/W | XXXXXXXX |
| 39 _H | Vacancy | | | |
| 3A _H | SMR1 | Serial mode register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 3B _H | SDR1 | Serial data register 1 | R/W | XXXXXXXX |
| 3C _H | EIE | External interrupt control register | R/W | 0 0 0 0 0 0 0 0 |
| 3D _H | EIF | External interrupt flag register | R/W | XXXXXXXX 0 |
| 3E _H , 3F _H | Vacancy | | | |
| 40 _H | HMDR | HUB mode register | R/W | 1 0 XXXXX 0 |
| 41 _H | HDSR1 | Hub descriptor register 1 | R/W | XXXXXXXX |
| 42 _H | HDSR2 | Hub descriptor register 2 | R/W | XXXXXXXX |
| 43 _H | HDSR3 | Hub descriptor register 3 | R/W | XXXXXXXX |
| 44 _H | HSTR | Hub status register | R/W | 0 0 0 0 0 0 0 0 |
| 45 _H | OCCR | Over current register | R/W | 0 XXX 0 0 0 0 |
| 46 _H | DADR | Descriptor ROM address register | R/W | XXXXXXXX |
| 47 _H | Reserved area | | | |
| 48 _H , 49 _H | Vacancy | | | |
| 4A _H | SMR2 | Serial mode register 2 | R/W | 0 0 0 0 0 0 0 0 |
| 4B _H | SDR2 | Serial data register 2 | R/W | XXXXXXXX |
| 4C _H , 4D _H | Vacancy | | | |
| 4E _H | HDSR4 | Hub descriptor register 4 | R/W | 0 0 0 0 0 1 0 1 |
| 4F _H | Vacancy | | | |
| 50 _H | UMDR | USB reset mode register | R/W | 1 0 0 0 XX 0 0 |
| 51 _H | DBAR | DMA base address register | R/W | XXXXXXXX |
| 52 _H | TDCR0 | Transfer data count register 0 | R/W | X 0 0 0 0 0 0 0 |
| 53 _H | TDCR1 | Transfer data count register 1 | R/W | X 0 0 0 0 0 0 0 |
| 54 _H | Reserved area | | | |
| 55 _H | TDCR21 | Transfer data count register 2 | R/W | X 0 0 0 0 0 0 0 |

(Continued)

MB89051 Series

(Continued)

| Address | Register name | Register description | Read/write | Initial value |
|------------------------------------|---------------|------------------------------------|------------|-----------------|
| 56 _H | Reserved area | | | |
| 57 _H | TDCR3 | Transfer data count register 3 | R/W | X 0 0 0 0 0 0 0 |
| 58 _H | UCTR | USB control register | R/W | 0 0 0 0 0 0 0 0 |
| 59 _H | USTR1 | USB status register 1 | R/W | 0 0 0 0 0 0 0 0 |
| 5A _H | USTR2 | USB status register 2 | R | XXXXXX 0 0 |
| 5B _H | UMSKR | USB interrupt mask register | R/W | 0 0 0 0 0 0 0 0 |
| 5C _H | UFRMR1 | USB frame status register 1 | R | XXXXXXXX |
| 5D _H | UFRMR2 | USB frame status register 2 | R | XXXXXXXX |
| 5E _H | EPER | USB endpoint enable register | R/W | XXXX 0 0 0 1 |
| 5F _H | EPBR0 | End point setup register 0 | R/W | X 0 0 0 0 0 0 0 |
| 60 _H | EPBR11 | Endpoint setup register 11 | R/W | XX 0 0 0 0 XX |
| 61 _H | EPBR12 | Endpoint setup register 12 | R/W | X 0 0 0 0 0 0 0 |
| 62 _H | EPBR21 | Endpoint setup register 21 | R/W | XX 0 0 0 0 XX |
| 63 _H | EPBR22 | Endpoint setup register 22 | R/W | X 0 0 0 0 0 0 0 |
| 64 _H | EPBR31 | Endpoint setup register 31 | R/W | XX 0 0 0 0 XX |
| 65 _H | EPBR32 | Endpoint setup register 32 | R/W | X 0 0 0 0 0 0 0 |
| 66 _H | Reserved area | | | |
| 67 _H to 78 _H | Vacancy | | | |
| 79 _H | Reserved area | | | |
| 7A _H | Vacancy | | | |
| 7B _H | ILR1 | Interrupt level setting register 1 | W | 1 1 1 1 1 1 1 1 |
| 7C _H | ILR2 | Interrupt level setting register 2 | W | 1 1 1 1 1 1 1 1 |
| 7D _H | ILR3 | level setting register 3 | W | 1 1 1 1 1 1 1 1 |
| 7E _H | ILR4 | Interrupt level setting register 4 | W | 1 1 1 1 1 1 1 1 |
| 7F _H | Reserved area | | | |

- Information about read/write
R/W: Read/write enabled, R: Read only, W: Write only
- Information about initial values
0: The initial value of this bit is "0".
1: The initial bit of this bit is "1".
X: The initial value of this bit is undefined.

Note : Vacancies and reserved spaces are not for use.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Rating | | Unit | Remarks |
|--|---------------------|--------------|--------------|------|--|
| | | Min | Max | | |
| Power supply voltage | V_{CC} | $V_{SS}-0.3$ | $V_{SS}+6.0$ | V | |
| Input voltage | V_I | $V_{SS}-0.3$ | $V_{CC}+0.3$ | V | Other than P31 to P37, P46, P47, P53, P54* ¹ |
| | | $V_{SS}-0.3$ | 3.3 | V | P31 to P37 |
| | | $V_{SS}-0.3$ | $V_{SS}+6.0$ | V | P46, P47, P53, P54* ¹ |
| Output voltage | V_O | $V_{SS}-0.3$ | $V_{CC}+0.3$ | V | Other than P31 to P37, P46, P47, P53, P54, CLK1, CLK2, USBP |
| | | $V_{SS}-0.3$ | 3.6 | V | P31 to P37, CLK1, CLK2, USBP |
| | | $V_{SS}-0.3$ | $V_{SS}+6.0$ | V | P46, P47, P53, 54 |
| Maximum clamp current | I_{CLAMP} | -2.0 | 2.0 | mA | *5 |
| Total maximum clamp current | $\Sigma I_{CLAMP} $ | — | 20 | mA | *5 |
| "L" level maximum output current | I_{OL} | — | 15 | mA | Normal output* ² |
| "L" level average output current | I_{OLAV} | — | 4 | mA | Normal output* ³ |
| "L" level total maximum output current | ΣI_{OL} | — | 100 | mA | Total normal output |
| "L" level total average output current | ΣI_{OLAV} | — | 40 | mA | Total normal output* ⁴ |
| "H" level maximum output current | I_{OH} | — | -15 | mA | Normal output* ² |
| "H" level average output current | I_{OHAV} | — | -4 | mA | Normal output* ³ |
| "H" level total maximum output current | ΣI_{OH} | — | -50 | mA | Total normal output |
| "H" level maximum output current | | — | -10 | mA | Total output of P31 to P37, CLK1, CLK2, USBP. |
| "H" level average total output current | ΣI_{OHAV} | — | -20 | mA | Total normal output* ⁴ |
| | | — | -10 | mA | Total output of P31 to P37, CLK1, CLK2 and USBP.* ⁴ |
| Power consumption | P_D | — | 300 | mW | |
| Operating temperature | T_A | -40 | +85 | °C | |
| Storage temperature | T_{stg} | -55 | +150 | °C | |

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

*1 : V_I should not exceed the specified ratings. However, if the maximum current to /from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

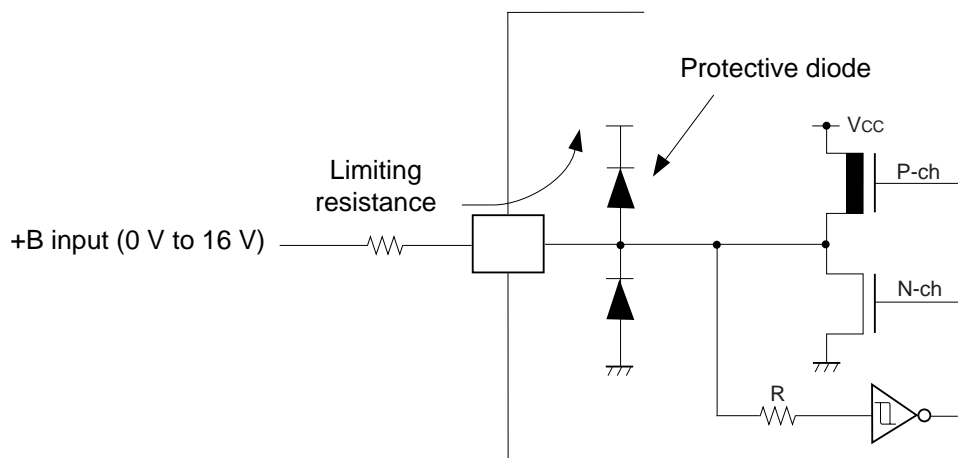
*2 : Maximum output current is defined as the peak value at one corresponding pin.

*3 : Average output current is defined as the average current flowing through one corresponding pin in an interval of 100 ms. (Average value : operating current \times operating duty)

MB89051 Series

- *4 : Average total output current is defined as the average current flowing through all corresponding pins in an interval of 100 ms.
- *5 :
- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P40 to P45
 - Use within recommended operating conditions.
 - Use at DC voltage (current)
 - The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.
 - The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
 - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
 - Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
 - Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
 - Care must be taken not to leave the +B input pin open.
 - Note that analog system input pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
 - Sample recommended circuits :

- Input/Output Equivalent circuits



WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

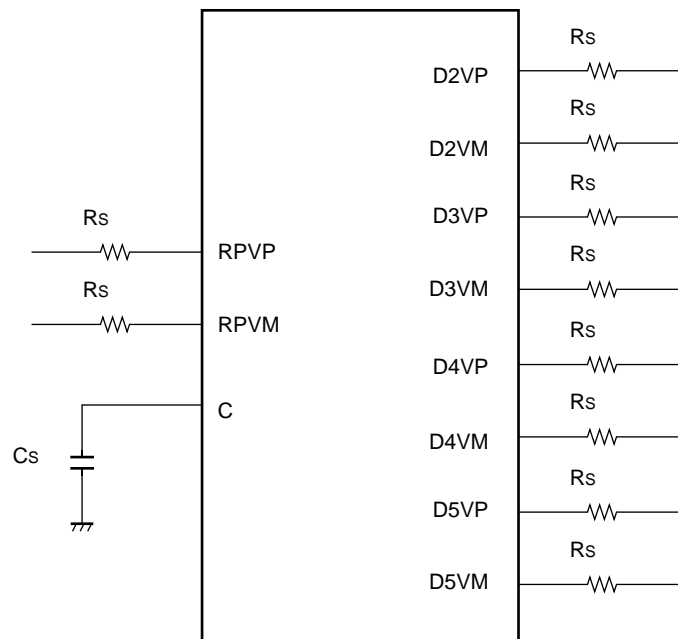
2. Recommended Operating Conditions

($V_{SS} = 0\text{ V}$)

| Parameter | Symbol | Value | | | Unit | Remarks |
|-----------------------|----------|-------|-----|-----|---------------|--------------------------------------|
| | | Min | Typ | Max | | |
| Power supply voltage | V_{CC} | 4.5 | — | 5.5 | V | At $V_{CC} = 5.0\text{ V}$ |
| | | 3.0 | — | 3.6 | V | At $V_{CC} = 3.3\text{ V}^*$ |
| Operating temperature | T_A | -40 | — | +85 | °C | When the USB function is not in use. |
| | | 0 | — | +70 | °C | When the USB function is in use |
| Smoothing capacitor | C_S | 0.1 | — | 1.0 | μF | At $V_{CC} = 5.0\text{ V}^*$ |
| Series resistance | R_S | — | 16 | — | Ω | When the USB function is in use |

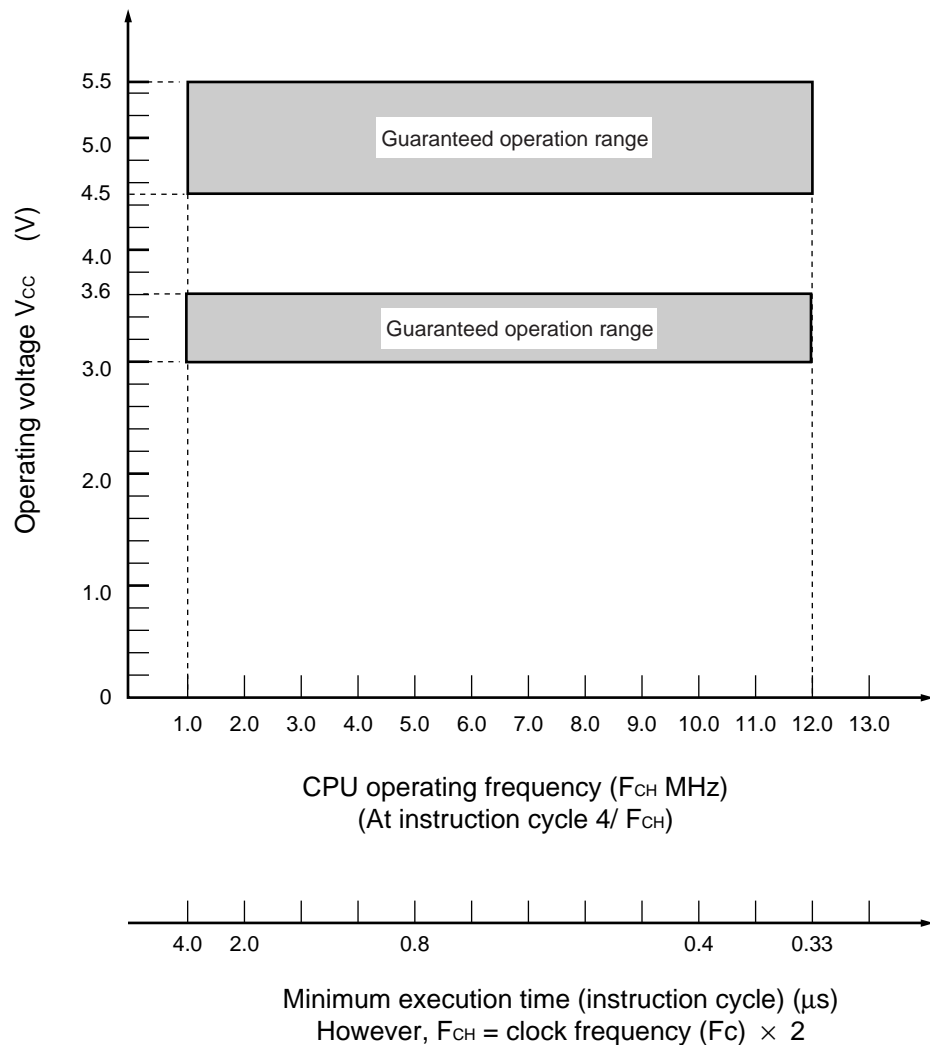
*: Use either a ceramic capacitor or a capacitor with similar frequency characteristics. The capacity of the smoothing capacitor for the V_{CC} pin should be greater than that of the C_S . When using with a supply voltage of 3.3 V, connect pin C with V_{CC} to input 3.3 V.

• C and USB Port Connection Diagram



MB89051 Series

- Operating voltage vs. Operating frequency



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics (Power supply voltage : 5.0 V)

($V_{CC} = 5.0 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|---------------------------------------|------------|---|----------------------------|--------------|-----|--------------|------|-------------|
| | | | | Min | Typ | Max | | |
| “H” level Input voltage | V_{IH} | P00 to P07, P10 to P17, P20 to P27, P40 to P47, P53, P54, MOD0, MOD1, MOD2 | — | $0.7 V_{CC}$ | — | $V_{CC}+0.3$ | V | |
| | | P31 to P37 | — | 2.5 | — | 3.3 | V | 3 V |
| | V_{IHS} | \overline{RST} , \overline{UCK} , UI | — | $0.8 V_{CC}$ | — | $V_{CC}+0.3$ | V | |
| | | $\overline{INT1}$ to $\overline{INT7}$, SCK1, SCK2, SI1, SI2 | — | 2.9 | — | 3.3 | V | 3 V |
| | V_{IH2C} | SCL, SDA | — | $0.8 V_{CC}$ | — | $V_{CC}+5.5$ | V | |
| “L” level Input voltage | V_{IL} | P00 to P07, P10 to P17, P20 to P27, P40 to P47, P53, P54, MOD0, MOD1, MOD2 | — | $V_{SS}-0.3$ | — | $0.3 V_{CC}$ | V | |
| | | P31 to P37 | — | $V_{SS}-0.3$ | — | 0.9 | | 3 V |
| | V_{ILS} | \overline{RST} , $\overline{INT1}$ to $\overline{INT7}$, \overline{UCK} , UI | — | $V_{SS}-0.3$ | — | $0.2 V_{CC}$ | V | |
| | | $\overline{INT1}$ to $\overline{INT7}$, SCK1, SCK2, SI1, SI2 | — | $V_{SS}-0.3$ | — | 0.6 | | 3 V |
| | V_{IL2C} | SCL, SDA | — | $V_{SS}-0.3$ | — | $0.3 V_{CC}$ | V | |
| Open-drain output application voltage | V_{D1} | P53, P54 | — | $V_{SS}-0.3$ | — | $V_{CC}+0.3$ | V | |
| “H” level Output voltage | V_{OH} | P00 to P07, P10 to P17, P20 to P24, P40 to P47 | $I_{OH} = -2.0 \text{ mA}$ | 4.0 | — | — | V | |
| | | P31 to P37, CLK1, CLK2 | $I_{OH} = -1.0 \text{ mA}$ | 2.6 | — | 3.6 V | V | 3 V |
| | | USBP | $I_{OH} = -2.4 \text{ mA}$ | 3.0 | — | 3.6 V | V | USB Pull up |

(Continued)

MB89051 Series

(Continued)

($V_{CC} = 5.0\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|--|------------|--|--|-------|-----|-----|---------------|---|
| | | | | Min | Typ | Max | | |
| “L” level Output voltage | V_{OL} | P00 to P07, P10 to P17, P20 to P24, P40 to P47, P53, P54, \overline{RST} | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| | | P31 to P37, CLK1, CLK2 | $I_{OL} = 1.0\text{ mA}$ | — | — | 0.4 | V | 3 V |
| Input leakage current (Hi-Z output leakage current) | I_{LI} | P00 to P07, P10 to P17, P20 to P27, P31 to P37, P40 to P47, CLK1, CLK2 | $0.0\text{ V} < V_I < V_{CC}$ | −5 | — | +5 | μA | When no pullup resistance is specified |
| | | USBP | | −5 | — | +5 | μA | |
| | | | | −5 | — | +5 | μA | |
| Open-drain out- put leakage cur- rent | I_{LID} | P53, P54 | $0.0\text{ V} < V_I < V_{SS} + 5.5\text{ V}$ | — | — | +5 | μA | |
| Pullup resistance | R_{PULL} | P00 to P07, P10 to P17, P20 to P27, P31 to P37, P40 to P47, P53, P54, \overline{RST} | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | k Ω | \overline{RST} is excluded when pullup resistance available is specified. |
| Power supply current | I_{CC} | V_{CC} | $F_{CH} = 12.0\text{ MHz}$, $V_{CC} = 5.0\text{ V}$, $t_{inst} = 0.333\text{ }\mu\text{s}$ | — | 29 | 42 | mA | MB89F051 |
| | | | | — | 28 | 41 | mA | MB89051 |
| | I_{CCS1} | | $F_{CH} = 12.0\text{ MHz}$, $V_{CC} = 5.0\text{ V}$, $t_{inst} = 0.333\text{ }\mu\text{s}$ | — | 20 | 30 | mA | Sleep mode |
| | I_{CCH} | | $T_A = +25\text{ }^{\circ}\text{C}$ | — | 40 | 70 | μA | Stop |
| Input capacitance | C_{IN} | Other than V_{CC} , V_{SS} and C | $f = 1\text{ MHz}$ | — | 5 | 15 | pF | |

4. DC Characteristics (Power supply votage : 3.3 V)

($V_{CC} = 3.3 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

| Parameter | Sym bol | Pin | Condition | Value | | | Unit | Remarks |
|---|------------|---|----------------------------|--------------|-----|--------------|------|--|
| | | | | Min | Typ | Max | | |
| “H” level Input voltage | V_{IH} | P00 to P07, P10 to P17, P20 to P27, P31 to P37, P40 to P47, P53, P54, MOD0, MOD1, MOD2 | — | $0.7 V_{CC}$ | — | $V_{CC}+0.3$ | V | |
| | V_{IHS} | \overline{RST} , UCK, UI, $\overline{INT1}$ to $\overline{INT7}$, SCK1, SCK2, SI1, SI2 | — | $0.8 V_{CC}$ | — | $V_{CC}+0.3$ | V | |
| | V_{IH2C} | SCL, SDA | — | $0.8 V_{CC}$ | — | $V_{CC}+5.5$ | V | |
| “L” level Input voltage | V_{IL} | P00 to P07, P10 to P17, P20 to P27, P31 to P37, P40 to P47, P53, P54, MOD0, MOD1, MOD2 | — | $V_{SS}-0.3$ | — | $0.3 V_{CC}$ | V | |
| | V_{ILS} | \overline{RST} , $\overline{INT1}$ to $\overline{INT7}$, UCK, UI, $\overline{INT1}$ to $\overline{INT7}$, SCK1, SCK2, SI1, SI2 | — | $V_{SS}-0.3$ | — | $0.2 V_{CC}$ | V | |
| | V_{IL2C} | SCL, SDA | — | $V_{SS}-0.3$ | — | $0.3 V_{CC}$ | V | |
| Open-drain output application voltage | V_{D1} | P53, P54 | — | $V_{SS}-0.3$ | — | $V_{CC}+0.3$ | V | |
| “H” level Output voltage | V_{OH} | P00 to P07, P10 to P17, P20 to P24, P40 to P47 | $I_{OH} = -2.0 \text{ mA}$ | 2.6 | — | — | V | |
| | | P31 to P37, CLK1, CLK2 | $I_{OH} = -1.0 \text{ mA}$ | 2.6 | — | — | V | |
| | | USBP | $I_{OH} = -2.4 \text{ mA}$ | 3.0 | — | — | V | USB Pull up, $V_{CC} = 3.1 \text{ V}$ to 3.6 V |

(Continued)

MB89051 Series

(Continued)

($V_{CC} = 3.3\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Pin | Condition | Value | | | Unit | Remarks |
|--|------------|--|--|-------|-----|-----|---------------|---|
| | | | | Min | Typ | Max | | |
| “L” level Output voltage | V_{OL} | P00 to P07, P10 to P17, P20 to P24, P40 to P47, P53, P54, \overline{RST} | $I_{OL} = 4.0\text{ mA}$ | — | — | 0.4 | V | |
| | | P31 to P37, CLK1, CLK2 | $I_{OL} = 1.0\text{ mA}$ | — | — | 0.4 | V | |
| Input leakage current (Hi-Z output leakage current) | I_{LI} | P00 to P07, P10 to P17, P20 to P27, P31 to P37, P40 to P47, CLK1, CLK2 | $0.0\text{ V} < V_I < V_{CC}$ | −5 | — | +5 | μA | When no pullup resistance is specified |
| | | USBP | | −5 | — | +5 | μA | |
| | | | | −5 | — | +5 | μA | |
| Open-drain output leakage current | I_{LID} | P53, P54 | $0.0\text{ V} < V_I < V_{SS}+5.5\text{ V}$ | — | — | +5 | μA | |
| Pullup resistance | R_{PULL} | P00 to P07, P10 to P17, P20 to P27, P31 to P37, P40 to P47, P53, P54, \overline{RST} | $V_I = 0.0\text{ V}$ | 25 | 50 | 100 | k Ω | \overline{RST} is excluded when pullup resistance available is specified. |
| Power supply current | I_{CC} | V_{CC} | $F_{CH} = 12.0\text{ MHz}$, $V_{CC} = 3.3\text{ V}$, $t_{inst} = 0.333\text{ }\mu\text{s}$ | — | 29 | 42 | mA | MB89F051 |
| | | | | — | 28 | 41 | mA | MB89051 |
| | I_{CCS1} | | $F_{CH} = 12.0\text{ MHz}$, $V_{CC} = 3.3\text{ V}$, $t_{inst} = 0.333\text{ }\mu\text{s}$ | — | 20 | 30 | mA | Sleep mode |
| | I_{CCH} | | $T_A = +25\text{ }^{\circ}\text{C}$ | — | 40 | 70 | μA | Stop |
| Input capacitance | C_{IN} | Other than V_{CC} and V_{SS} | $f = 1\text{ MHz}$ | — | 10 | — | pF | |

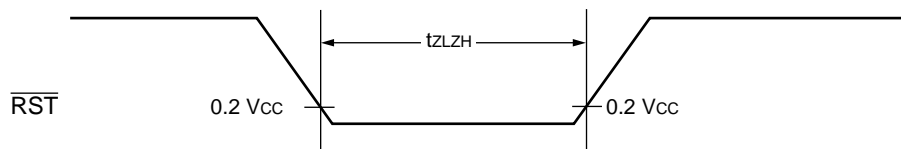
5. AC Characteristics

(1) Reset Timing

($V_{CC} = 5.0 \text{ V}$, $V_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|---|-------------------|-----------|----------------------|-----|------|---------|
| | | | Min | Max | | |
| $\overline{\text{RST}}$ "L" pulse width | t_{ZLZH} | — | 48 t_{HCYL} | — | ns | |

- Notes :
- t_{HCYL} is the oscillation cycle for the internal main clock.
 - If the reset pulse applied to the external reset pin ($\overline{\text{RST}}$) does not meet the specifications, it may cause malfunctions. Use caution so that the reset pulse less than the specifications will not be fed to the external reset pin ($\overline{\text{RST}}$).

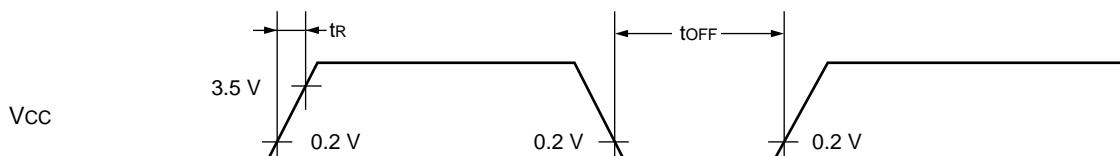


(2) Power-on reset

($V_{SS} = 0 \text{ V}$, $T_A = -40 \text{ }^{\circ}\text{C}$ to $+85 \text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Condition | Value | | Unit | Remarks |
|--------------------------|------------------|-----------|-------|-----|------|----------------------------|
| | | | Min | Max | | |
| Power supply rising time | t_R | — | 0.066 | 50 | ms | |
| Power supply cutoff time | t_{OFF} | — | 4 | — | ns | Due to repeated operations |

- Note : The power supply must be up within the selected oscillation stabilization time.
When the supply voltage needs to be varied while operating, it is recommended to smoothly start up the voltage.



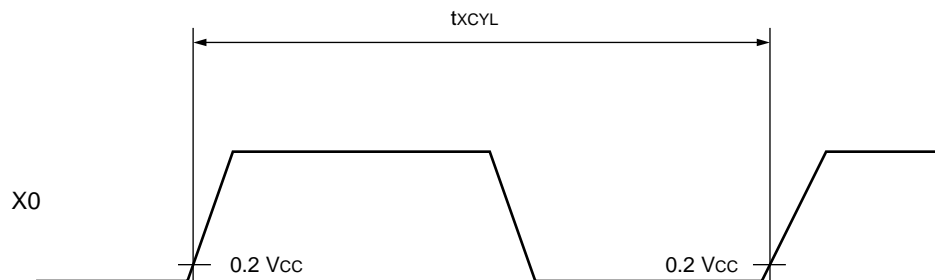
MB89051 Series

(3) Clock Timing

($V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

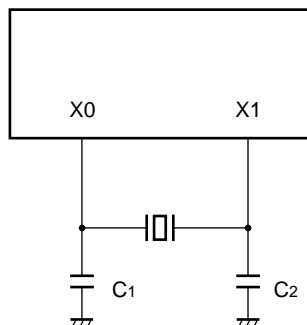
| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|-------------------------------|------------|----------|-----------|-------|-------|-----|------|-----------------|
| | | | | Min | Typ | Max | | |
| Clock frequency | F_C | X0, X1 | — | — | 6 | — | MHz | |
| Clock cycle time | t_{XCYL} | X0, X1 | | — | 166.6 | — | ns | |
| Internal main clock frequency | F_{CH} | — | | — | 12 | — | MHz | Twice the F_C |
| Internal clock cycle | t_{HCYL} | — | | — | 83.3 | — | ns | $t_{XCYL}/2$ |

• X0 and X1 Timing and Conditions



• Clock Conditions

When a crystal resonator is used



(4) Instruction Cycle

($V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

| Parameter | Symbol | Value | Unit | Remarks |
|---|------------|--|---------------|---|
| Instruction cycle (Min execution time) | t_{inst} | $4 / F_{CH}$, $8 / F_{CH}$, $16 / F_{CH}$, $64 / F_{CH}$ | μs | When operating at $F_{CH} = 12\text{ MHz}$ $t_{inst} = 0.33\text{ }\mu\text{s}$ ($4 / F_{CH}$) |

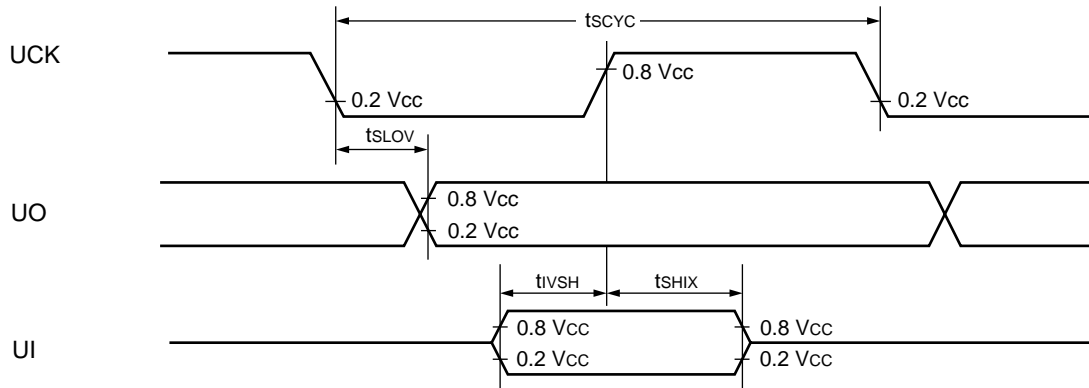
(5) UART Serial I/O Timing

($V_{CC} = 5.0\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

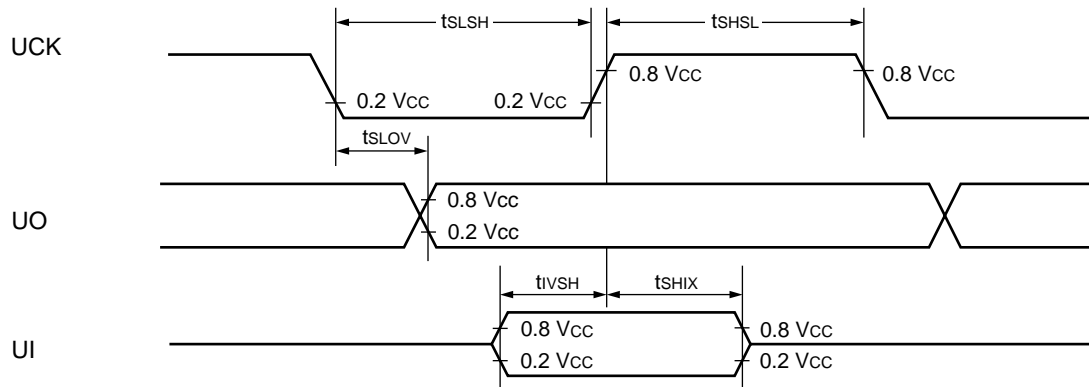
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|------------|----------|---------------------------|-----------------|------|---------------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | UCK | Internal shift clock mode | $2\ t_{inst}^*$ | — | μs | |
| UCK $\downarrow \rightarrow$ UO | t_{SLOV} | UCK, UO | | -200 | +200 | ns | |
| Valid UI \rightarrow UCK \uparrow | t_{IVSH} | UI, UCK | | 200 | — | ns | |
| UCK $\uparrow \rightarrow$ valid UI hold time | t_{SHIX} | UCK, UI | | 200 | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | UCK | External shift clock mode | $1\ t_{inst}^*$ | — | μs | |
| Serial clock "L" pulse width | t_{SLSH} | | | $1\ t_{inst}^*$ | — | μs | |
| UCK $\downarrow \rightarrow$ UO time | t_{SLOV} | UCK, UO | | 0 | 200 | ns | |
| Valid UI \rightarrow UCK \uparrow | t_{IVSH} | UI, UCK | | 200 | — | ns | |
| UCK $\uparrow \rightarrow$ valid UI hold time | t_{SHIX} | UCK, UI | | 200 | — | ns | |

* : For information on t_{inst} , see "(4) Instruction Cycle".

• Internal shift clock mode



• External shift clock mode



MB89051 Series

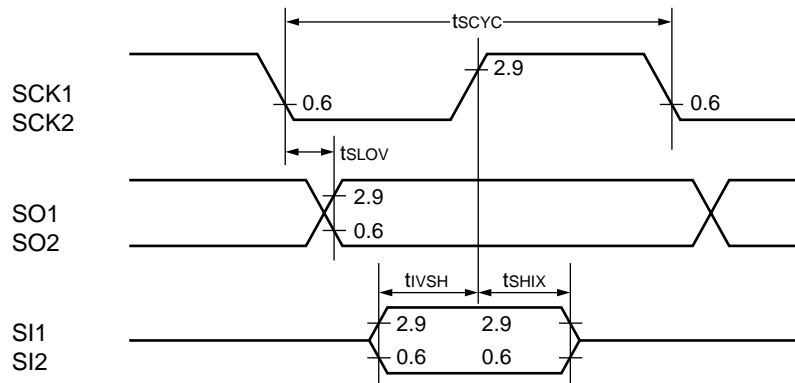
(6) Serial I/O Timing

($V_{CC} = 5.0\text{ V}$, $V_{SS} = 0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

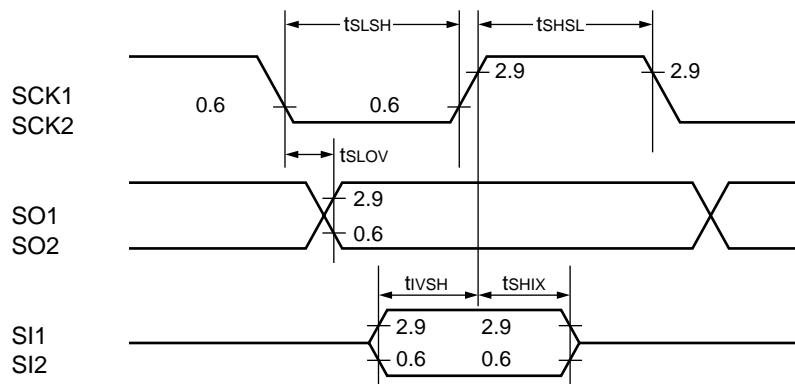
| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|------------|----------------------|---------------------------|----------------|------|---------------|---------|
| | | | | Min | Max | | |
| Serial clock cycle time | t_{SCYC} | SCK1, SCK2 | Internal shift clock mode | $2 t_{inst}^*$ | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK1, SO1, SCK2, SO2 | | -200 | +200 | ns | |
| Valid SI \rightarrow SCK \uparrow | t_{IVSH} | SCK1, SI1, SCK2, SI2 | | 200 | — | ns | |
| SCK $\uparrow \rightarrow$ Valid SI hold time | t_{SHIX} | SCK1, SI1, SCK2, SI2 | | 200 | — | ns | |
| Serial clock "H" pulse width | t_{SHSL} | SCK1, SCK2 | External shift clock mode | t_{inst}^* | — | μs | |
| Serial clock "L" pulse width | t_{SLSH} | SCK1, SCK2 | | t_{inst}^* | — | μs | |
| SCK $\downarrow \rightarrow$ SO time | t_{SLOV} | SCK1, SO1, SCK2, SO2 | | 0 | 200 | ns | |
| Valid SI \rightarrow SCK | t_{IVSH} | SCK1, SI1, SCK2, SI2 | | 200 | — | μs | |
| SCK $\uparrow \rightarrow$ Valid SI hold time | t_{SHIX} | SCK1, SI1, SCK2, SI2 | | 200 | — | μs | |

* : For information on t_{inst} , see “(4) Instruction Cycle”.

• Internal shift clock mode



• External shift clock mode

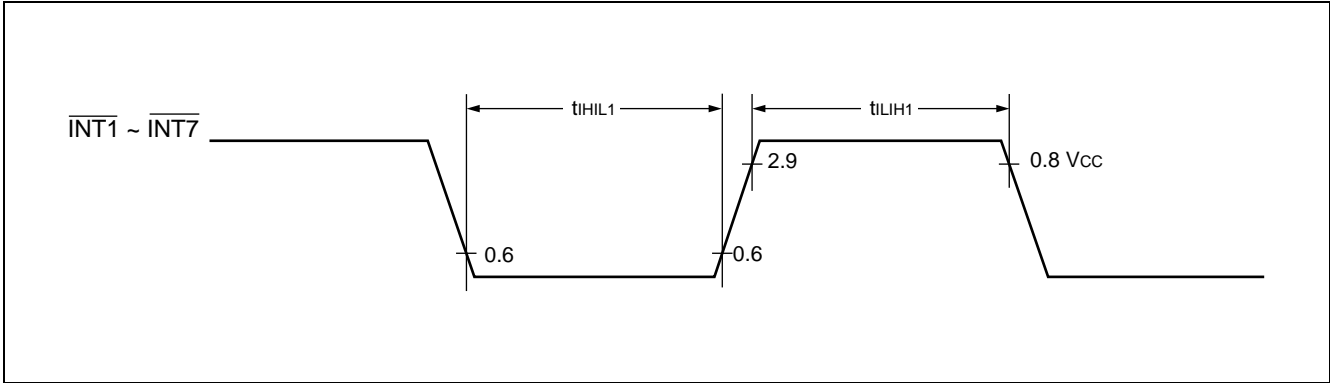


(7) Peripheral Input Timing

(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|------------------------------------|-------------------|--|-----------|-----------------------|-----|------|---------|
| | | | | Min | Max | | |
| Peripheral input “H” pulse width 1 | t _{LIH1} | $\overline{\text{INT1}}$ to $\overline{\text{INT7}}$ | — | 2 t _{inst} * | — | μs | |
| Peripheral input “L” pulse width 1 | t _{IHL1} | | — | 2 t _{inst} * | — | μs | |

* : For information on t_{inst}, see “ (4) Instruction Cycle”.



MB89051 Series

(8) I²C Timing

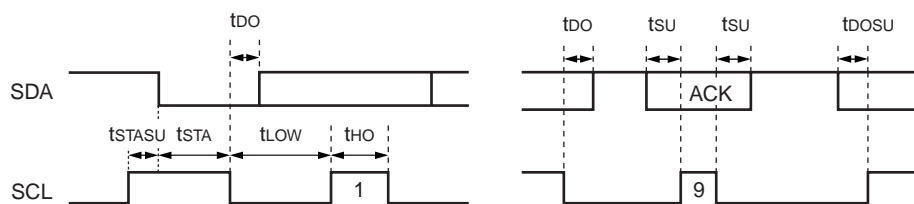
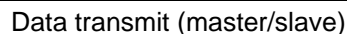
(V_{CC} = 5.0 V, V_{SS} = 0 V, T_A = -40 °C to +85 °C)

| Parameter | Symbol | Pin | Value | | Unit | Remarks |
|---------------------------------------|--------------------|-------------|---|---|------|-------------|
| | | | Min | Max | | |
| Start condition output | t _{STA} | SCL, SDA | $1 / 4 \times t_{inst}^{*1} \times m_t^{*2} \times n_t^{*3} - 20$ | $1 / 4 \times t_{inst}^{*1} \times m_t^{*2} \times n_t^{*3} + 20$ | ns | Master mode |
| Stop condition output | t _{STO} | SCL, SDA | $1 / 4 \times t_{inst}^{*1} \times (m_t^{*2} \times n_t^{*3} + 8) - 20$ | $1 / 4 \times t_{inst}^{*1} \times (m_t^{*2} \times n_t^{*3} + 8) + 20$ | ns | Master mode |
| Start condition detect | t _{STA} | SCL, SDA | $1 / 4 \times t_{inst}^{*1} \times 6 + 40$ | — | ns | |
| Stop condition detect | t _{STO} | SCL, SDA | $1 / 4 \times t_{inst}^{*1} \times 6 + 40$ | — | ns | |
| Restart condition output | t _{STASU} | SCL, SDA | $1 / 4 \times t_{inst}^{*1} \times (m_t^{*2} \times n_t^{*3} + 8) - 20$ | $1 / 4 \times t_{inst}^{*1} \times (m_t^{*2} \times n_t^{*3} + 8) + 20$ | ns | Master mode |
| Restart condition detect | t _{STASU} | SCL, SDA | $1 / 4 \times t_{inst}^{*1} \times 4 + 40$ | — | ns | |
| SCL output Low width | t _{LOW} | SCL | $1 / 4 \times t_{inst}^{*1} \times m_t^{*2} \times n_t^{*3} - 20$ | $1 / 4 \times t_{inst}^{*1} \times m_t^{*2} \times n_t^{*3} + 20$ | ns | Master mode |
| SCL output High width | t _{HIGH} | SCL | $1 / 4 \times t_{inst}^{*1} \times (m_t^{*2} \times n_t^{*3} + 8) - 20$ | $1 / 4 \times t_{inst}^{*1} \times (m_t^{*2} \times n_t^{*3} + 8) + 20$ | ns | Master mode |
| SDA output delay | t _{DO} | SDA | $1 / 4 \times t_{inst}^{*1} \times 4 - 20$ | $1 / 4 \times t_{inst}^{*1} \times 4 + 20$ | ns | |
| SDA output setup time after interrupt | t _{DOSU} | SDA | $1 / 4 \times t_{inst}^{*1} \times 4 - 20$ | — | ns | |
| SCL input Low pulse width | t _{LOW} | SCL | $1 / 4 \times t_{inst}^{*1} \times 6 + 40$ | — | ns | |
| SCL input High pulse width | t _{HIGH} | SCL | $1 / 4 \times t_{inst}^{*1} \times 2 + 40$ | — | ns | |
| SDA input setup time | t _{SU} | SDA | 40 | — | ns | |
| SDA hold time | t _{HO} | SDA | 0 | — | ns | |

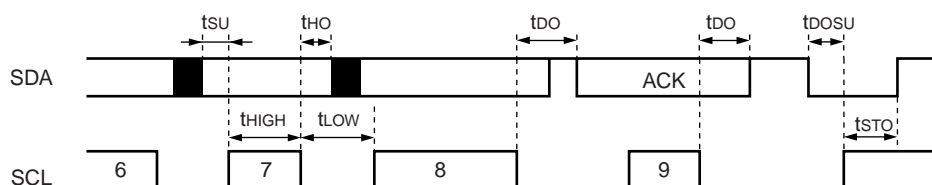
*1 : For information on t_{inst} , see “(4) Instruction Cycle”.

*2 : m is defined in the ICCR CS 4 to CS 3 (bit 4 to bit 3) .

*3 : n is defined in the ICCR CS 2 to CS 0 (bit 2 to bit 0) .



Data receive (master/slave)



6. FLASH Program/Erase characteristics

• Program/Erase characteristics

| Parameter | Condition | Value | | | Unit | Remarks |
|--------------------|--|--------|-----|-------|-------|---|
| | | Min | Typ | Max | | |
| Sector erase time | T _A = +25 °C V _{CC} = 5.0 V | — | 1 | 15 | s | Except for the write time before internal erase operation |
| Chip erase time | | — | 5 | 75 | s | Except for the write time before internal erase operation |
| Byte program time | | — | 8 | 3,600 | μs | Except for the over head time of the system. |
| Prgram/erase cycle | | 10,000 | — | — | cycle | |

MB89051 Series

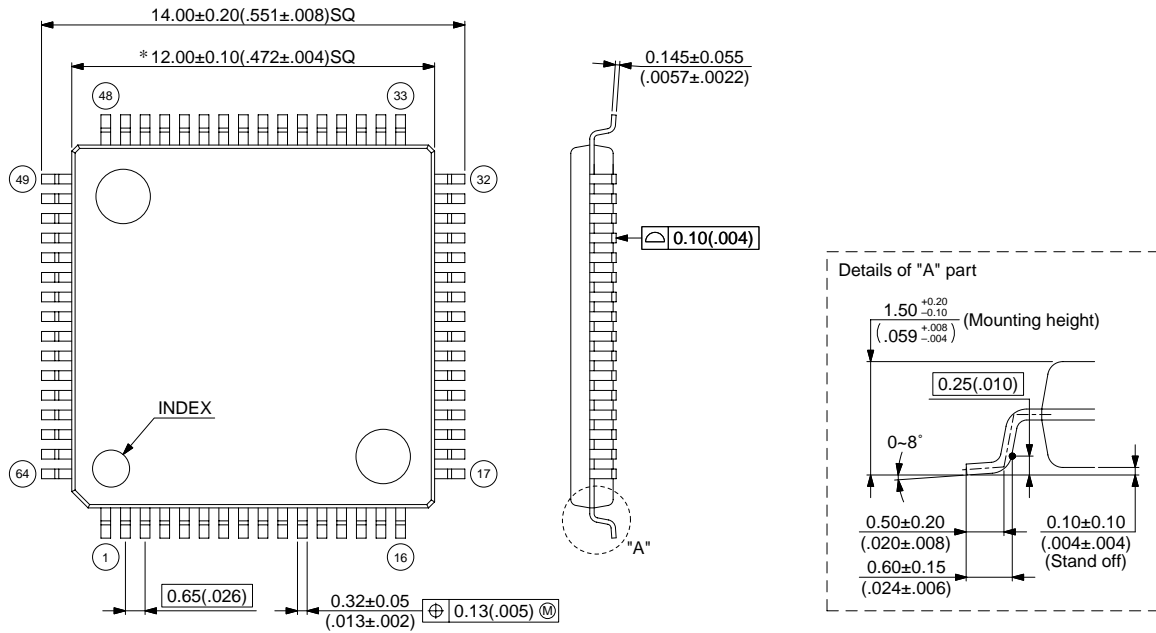
■ ORDERING INFORMATION

| Part Number | Package | Remarks |
|---------------------------|--------------------------------------|---------|
| MB89051PFM MB89F051PFM | 64-pin plastic LQFP (FPT-64P-M09) | |

■ PACKAGE DIMENSIONS

64-pin plastic LQFP
(FPT-64P-M09)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



© 2003 FUJITSU LIMITED F64018S-c-3-5

Dimensions in mm (inches)

Note : The values in parentheses are reference values.

FUJITSU LIMITED

All Rights Reserved.

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.