FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12541-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89930A Series

MB89935A/935B/P935A/PV930A

■ DESCRIPTION

The MB89930A series is a line of single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such, timers, a serial interface, an A/D converter and an external interrupt.

■ FEATURES

- MB89600 Series CPU core
- Maximum memory space : 64 Kbytes
- Minimum execution time : 0.4 µs/10 MHz
- Interrupt processing time : 3.6 µs/10 MHz
- I/O ports : max. 21channels
- 21-bit timebase timer
- 8-bit PWM timer
- 8/16-bit capture timer/counter
- 10-bit A/D converter : 8 channels
- UART
- 8-bit serial I/O
- External interrupt 1 : 3 channels
- External interrupt 2 : 8 channels
- Wild Register : 2 bytes

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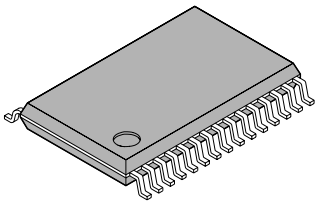
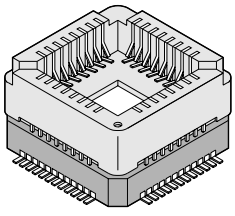
■ PACKAGE

30-pin plastic SSOP



(FPT-30P-M02)

48-pin ceramic MQFP



(MQP-48C-P01)

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- Low-power consumption modes (sleep mode, and stop mode)
- SSOP-30 and MQFP-48 package
- CMOS Technology

■ PRODUCT LINEUP

Parameter \ Part number	MB89935A	MB89935B	MB89P935A	MB89PV930A
Classification	Mass production product (mask ROM product)		One-time PROM product (for small-scale production)	Piggyback/evaluation product (for development)
ROM size	16 K × 8 bits (internal mask ROM)		16 K × 8 bits (internal PROM)	32 K × 8 bits (external EPROM)
RAM size	512 × 8 bits			
CPU functions	Number of instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, 16 bits Minimum execution time : 0.4 µs to 6.4 µs (10 MHz) Interrupt processing time : 3.6 µs to 57.6 µs (10 MHz)			
Ports	General-purpose I/O ports (CMOS) : 21 (also serve as peripherals) (4 ports are also an N-ch open-drain type.)			
21-bit time base timer	21-bit Interrupt cycle : 0.82 ms, 3.3 ms, 26.2 ms, or 419.4 ms with 10-MHz main clock			
Watching timer	Reset generation cycle : 419.4 ms minimum with 10-MHz main clock			
8-bit PWM timer	8-bit interval timer operation (square output capable, operating clock cycle : 0.4 µs , 3.2 µs, 6.4 µs, 25.6 µs) 8-bit resolution PWM operation (conversion cycle : 102.4 µs to 26.84 ms) Count clock selectable between 8-bit and 16-bit timer/counter outputs			
8/16-bit capture, timer/counter	8-bit capture timer/counter × 1 channel + 8-bit timer or 16-bit capture timer/counter × 1 channel Capable of event count operation and square wave output using external clock input with 8-bit timer 0 or 16-bit counter			
UART	Transfer data length : 6/7/8 bits			
8-bit Serial I/O	8 bits LSB first/MSB first selectable One clock selectable from four operation clocks (one external shift clock, three internal shift clocks : 0.8 µs, 6.4 µs, 25.6 µs)			
12-bit PPG timer	Output frequency : Pulse width and cycle selectable			
External interrupt 1 (wake-up function)	3 channels (Interrupt vector, request flag, request output enabled) Edge selectable (Rising edge, falling edge, or both edges) Also available for resetting stop/sleep mode (Edge detectable even in stop mode)			
External interrupt 2 (wake-up function)	1 channel with 8 inputs (Independent L-level interrupt and input enable) Also available for resetting stop/sleep mode (Level detectable even in stop mode)			

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Part number / Parameter	MB89935A	MB89935B	MB89P935A	MB89PV930A
10-bit A/D converter	10-bit precision × 8 channels A/D conversion function (Conversion time : 15.2 µs/10 MHz) Continuous activation by 8/16-bit timer/counter output or time-base timer counter			
Wild Register	8-bit × 2			
Standby mode	Sleep mode, and Stop mode			
*Power supply Voltage	2.2 V to 5.5 V		3.0 V to 5.5 V	2.7 V to 5.5 V

* : The minimum operating voltage varies with the operating frequency, the function, and the connected ICE.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89935A	MB89935B	MB89P935A	MB89PV930A
FPT-30P-M02	○	○	○	×*
MQP-48C-P01	×	×	×	○

○ : Available × : Not available

* : Adapter for 48-pin to 30-pin conversion (manufactured by Sun Hayato Co., Ltd.)
Part number : 48QF-30SOP-8L
Inquiry : Sun Hayato Co., Ltd. : TEL (81) -3-3986-0403

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used.

2. Current Consumption

In the case of the MB89PV930A, add the current consumed by the EPROM which is connected to the top socket.

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product. Before using options check section “■ MASK OPTIONS” Take particular care on the following points :

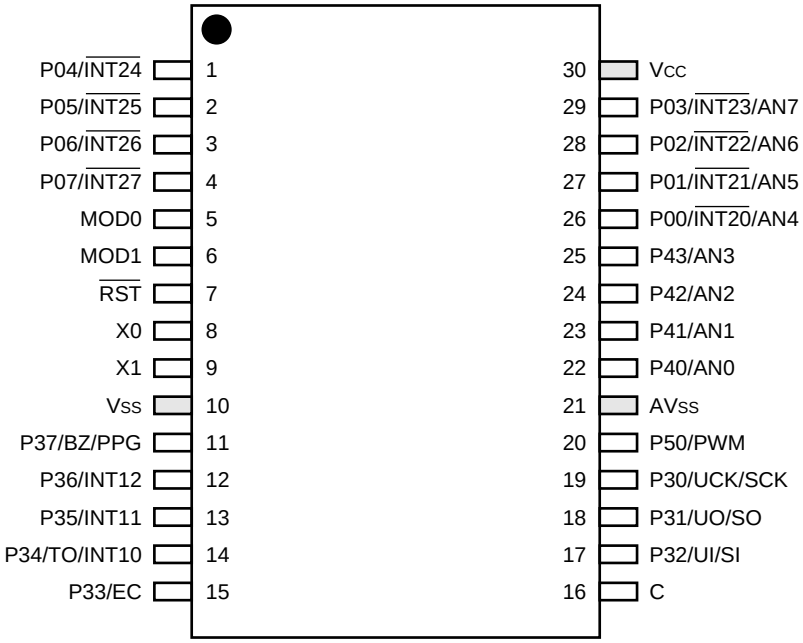
Options are fixed on the MB89PV930A and MB89P935A.

4. Difference between MB89935A and MB89935B

MB89935B is different from MB89935A in that the internal circuit and oscillator have been changed and the radiated noise and current consumption while oscillation is active is reduced. For details of the characteristics of current consumption, see “■ EXAMPLE CHARACTERISTICS”.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-30P-M02)

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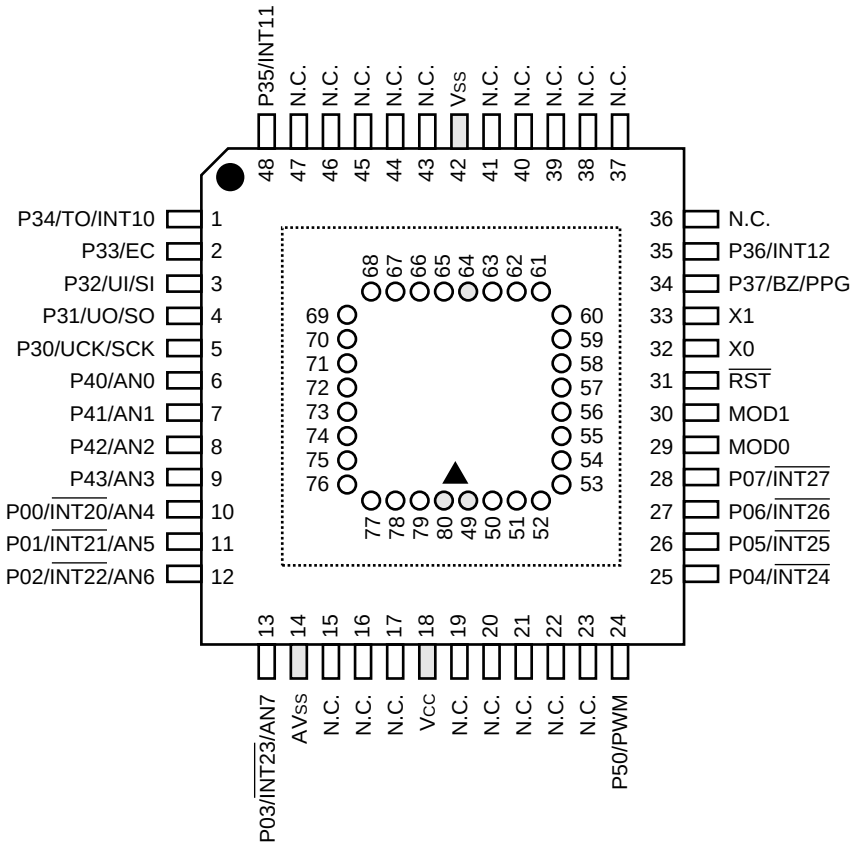
(TOP VIEW)



(MQP-48C-P01)

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
49	V_{PP}	57	N.C.	65	O4	73	OE
50	A12	58	A2	66	O5	74	N.C.
51	A7	59	A1	67	O6	75	A11
52	A6	60	A0	68	O7	76	A9
53	A5	61	O1	69	O8	77	A8
54	A4	62	O2	70	CE	78	A13
55	A3	63	O3	71	A10	79	A14
56	N.C.	64	V_{SS}	72	N.C.	80	V_{CC}

N.C. : Internally connected. Do not use.

■ PIN DESCRIPTION

Pin No.		Pin name	Circuit type	Function
SSOP*1	MQFP*2			
8	32	X0	A	Pins for connecting the crystal resonator for the main clock. To use an eternal clock, input the signal to X0 and leave X1 open.
9	33	X1		
5	29	MOD0	B	Memory access mode setting input pins. Connect the pin directly to Vss.
6	30	MOD1		
7	31	$\overline{RST}$	C	Reset I/O pin. This pin serves as an N-channel open-drain output with pull-up resistor and a hysteresis input as well. The pin outputs the "L" signal (optionally) in response to an internal reset request. Also, it initializes the internal circuit upon input of the "L" signal.
26 to 29	10 to 13	P00/$\overline{INT20}$/AN4 to P03/$\overline{INT23}$/AN7	G	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2 or as an A/D converter analog input. The input of external interrupt 2 is a hysteresis input.
1 to 4	25 to 28	P04/$\overline{INT24}$ to P07/$\overline{INT27}$	D	General-purpose CMOS I/O ports. These pins also serve as an input (wake-up input) of external interrupt 2. The input of external interrupt 2 is a hysteresis input.
19	5	P30/UCK/SCK	D	General-purpose CMOS I/O ports. This pin also serves as the clock I/O pin for the UART or 8-bit serial I/O. The resource is a hysteresis input.
18	4	P31/UO/SO	E	General-purpose CMOS I/O ports. This pin also serves as the data output pin for the UART or 8-bit serial I/O.
17	3	P32/UI/SI	D	General-purpose CMOS I/O ports. This pin also serves as the data input pin for the UART or 8-bit serial I/O. The resource is a hysteresis input.
15	2	P33/EC	D	General-purpose CMOS I/O ports. This pin also serves as the external clock input pin for the 8/16-bit capture timer/counter. The resource is a hysteresis input.
14	1	P34/TO/INT10	D	General-purpose CMOS I/O ports. This pin also serves as the output pin for the 8/16-bit capture timer/counter or as the input pin for external interrupt 1. The resource is a hysteresis input.
13, 12	48, 35	P35/INT11, P36/INT12	D	General-purpose CMOS I/O ports. These pins also serve as the input pin for external interrupt 1. The resource is a hysteresis input.

(Continued)

*1 : FPT-30P-M02

*2 : MQP-48C-P01

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Pin No.		Pin name	Circuit type	Function
SSOP*1	MQFP*2			
11	34	P37/BZ/PPG	E	General-purpose CMOS I/O ports. This pin also serves as the buzzer output pin or the 12-bit programmable pulse generator output.
20	24	P50/PWM	E	General-purpose CMOS I/O ports. This pin also serves as the 8-bit PWM output pin. The pin is a hysteresis input.
22 to 25	6 to 9	P40/AN0 to P43/AN3	F	General-purpose CMOS I/O ports. These pins can also be used as N-channel open-drain ports. The pins also serve as A/D converter analog input pins.
30	18	V_{CC}	—	Power supply pin
10	42	V_{SS}	—	Power (GND) pin
21	14	AV_{SS}	—	Power supply pin for the A-D converter. Apply equal potential to this pin and the V_{SS} pin.
16	—	C	—	Capacitance pin for regulating the power supply. Connect an external ceramic capacitor of about 0.1 μF.
—	15,16,17 19,20,21 22,23,36 37,38,39 40,41,43 44,45,46 47	N.C.	—	Internally connected pins Be sure to leave them open.

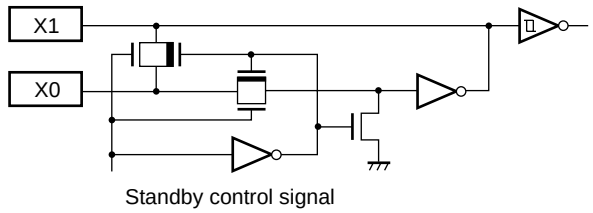
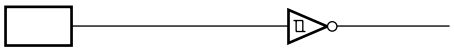
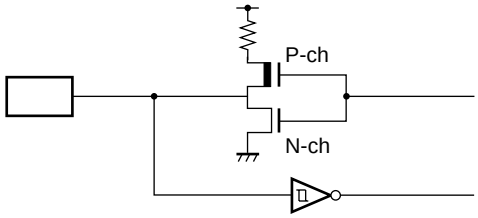
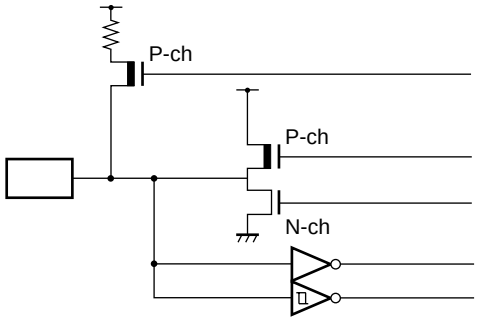
*1 : FPT-30P-M02

*2 : MQP-48C-P01

■ EXTERNAL EPROM PIN DESCRIPTION (MB89PV930A only)

Pin No.	Pin name	I/O	Function
49	V_{PP}	O	“H” level output pin
50 51 52 53 54 55 58 59 60	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
61 62 63	O1 O2 O3	I	Data input pins
64	V_{SS}	O	Power supply (GND) pin
65 66 67 68 69	O4 O5 O6 O7 O8	I	Data input pins
70	CE	O	ROM chip enable pin Outputs “H” during standby.
71	A10	O	Address output pin
73	OE	O	ROM output enable pin Outputs “L” at all times.
75 76 77 78 79	A11 A9 A8 A13 A14	O	Address output pins
80	V_{CC}	O	EPROM power supply pin
56 57 72 74	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal oscillation type
B		• Hysteresis input
C		• At an output pull-up resister (P-ch) of approximately 50 kΩ/5.0 V • Hysteresis input
D		• CMOS output • CMOS input • Hysteresis input (Resource input) • Pull-up resistor optional

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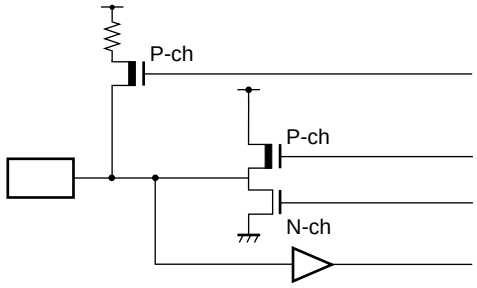
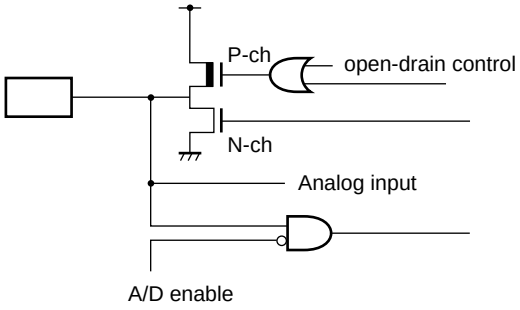
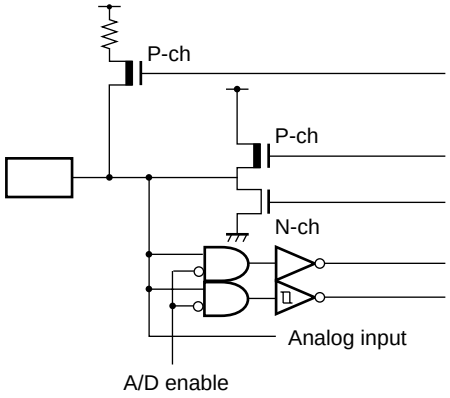
Type	Circuit	Remarks
E		• CMOS output • CMOS input • Pull-up resistor optional
F		• CMOS output • CMOS input • Analog input • N-ch open-drain output available
G		• CMOS output • CMOS input • Hysteresis input (Resouce input) • Analog input

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ ELECTRICAL CHARACTERISTICS” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input terminals open may lead to permanent damage due to malfunction and latchup; pull up or pull down the terminals through the resistors of 2 kΩ or more.
Make the unused I/O terminal in a state of output and leave it open and if it is in an input state, handle it with the same procedure as the input terminals.

3. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

4. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

5. Treatment of Power Supply Pins on Microcontrollers with A/D Converters

Connect to be $AV_{SS} = V_{SS}$ even if the A/D converters are not in use.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

7. About the Wild Register Function

No wild register can be debugged on the MB89PV930A. For the operation check, test the MB89P935A installed on a target system.

8. Program Execution in RAM

When the MB89PV930A is used, no program can be executed in RAM.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TVM

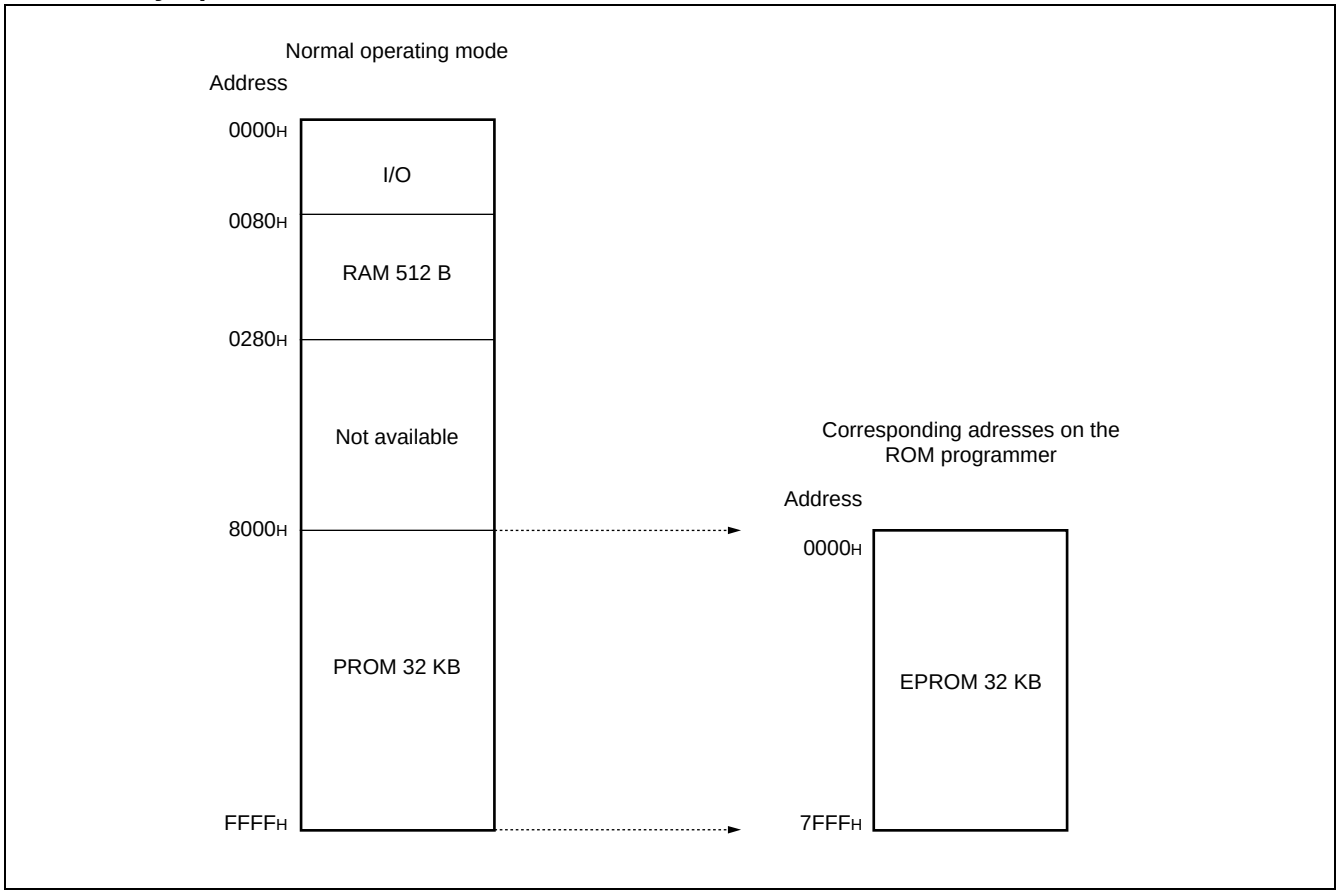
2. Programming Socket Adapter

To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer : Sun Hayato Co., Ltd.) listed below.

Package	Compatible socket part number
LCC-32	ROM-32LC-28DP-S

Inquiry : Sun Hayato Co., Ltd. : TEL (81) -3-3986-0403
FAX (81) -3-5396-9106

3. Memory Space.



4. Programming to the EPROM

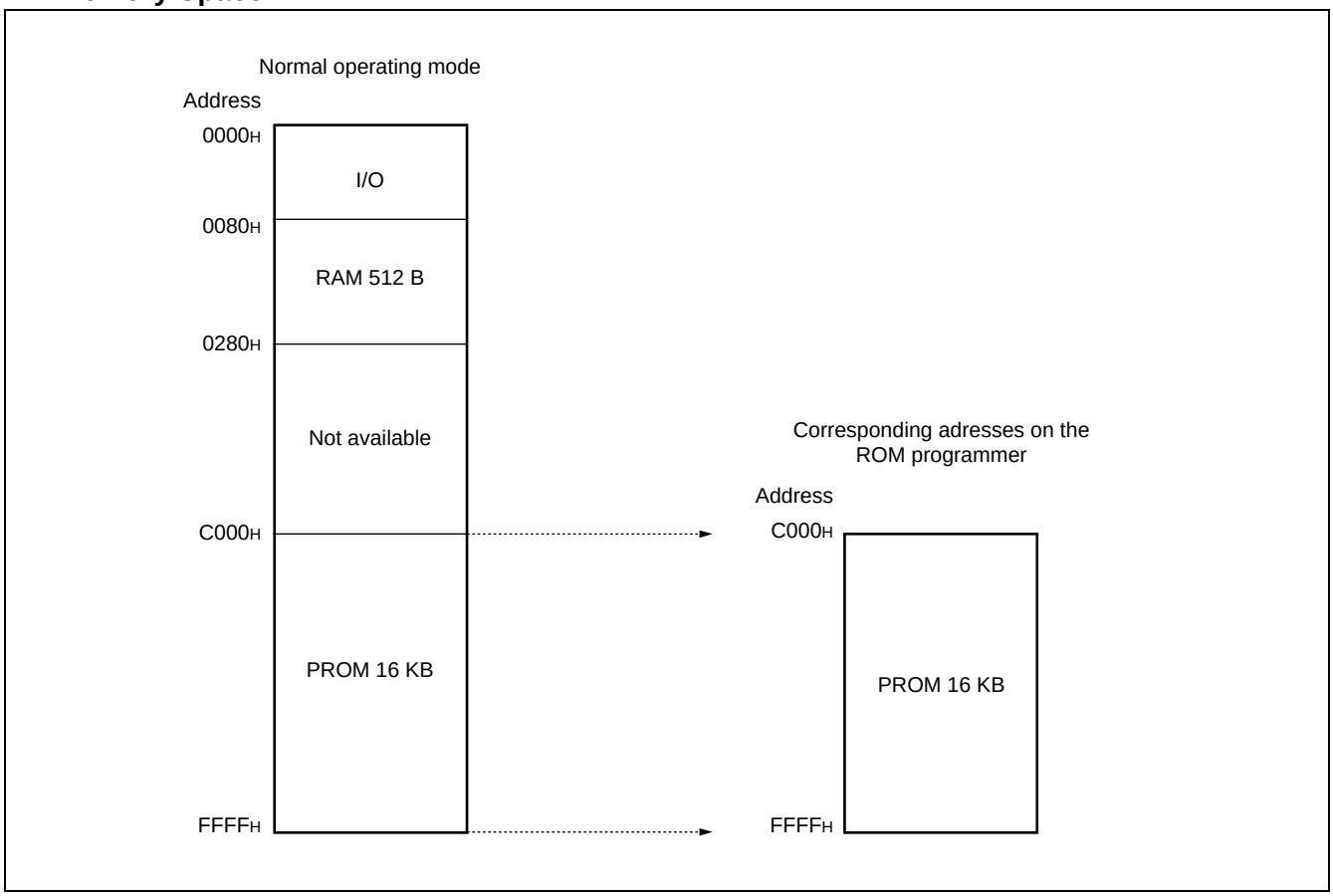
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$.

(3) Program to 0000_H to $7FFF_H$ with the EPROM programmer.

■ PROGRAMMING TO THE OTPROM WITH MB89P935A

1. Memory Space



2. Programming to the OTPROM

To program to the OTPROM using an EPROM programmer AF200 (manufacturer : Yokogawa Digital Computer Corp.) .

Inquiry : Yokogawa Digital Computer Corp. : TEL (81) -42-333-6224

Note : Programming to the OTPROM with MB89P935A is serial programming mode only.

3. Programming Adaptor for OTPROM

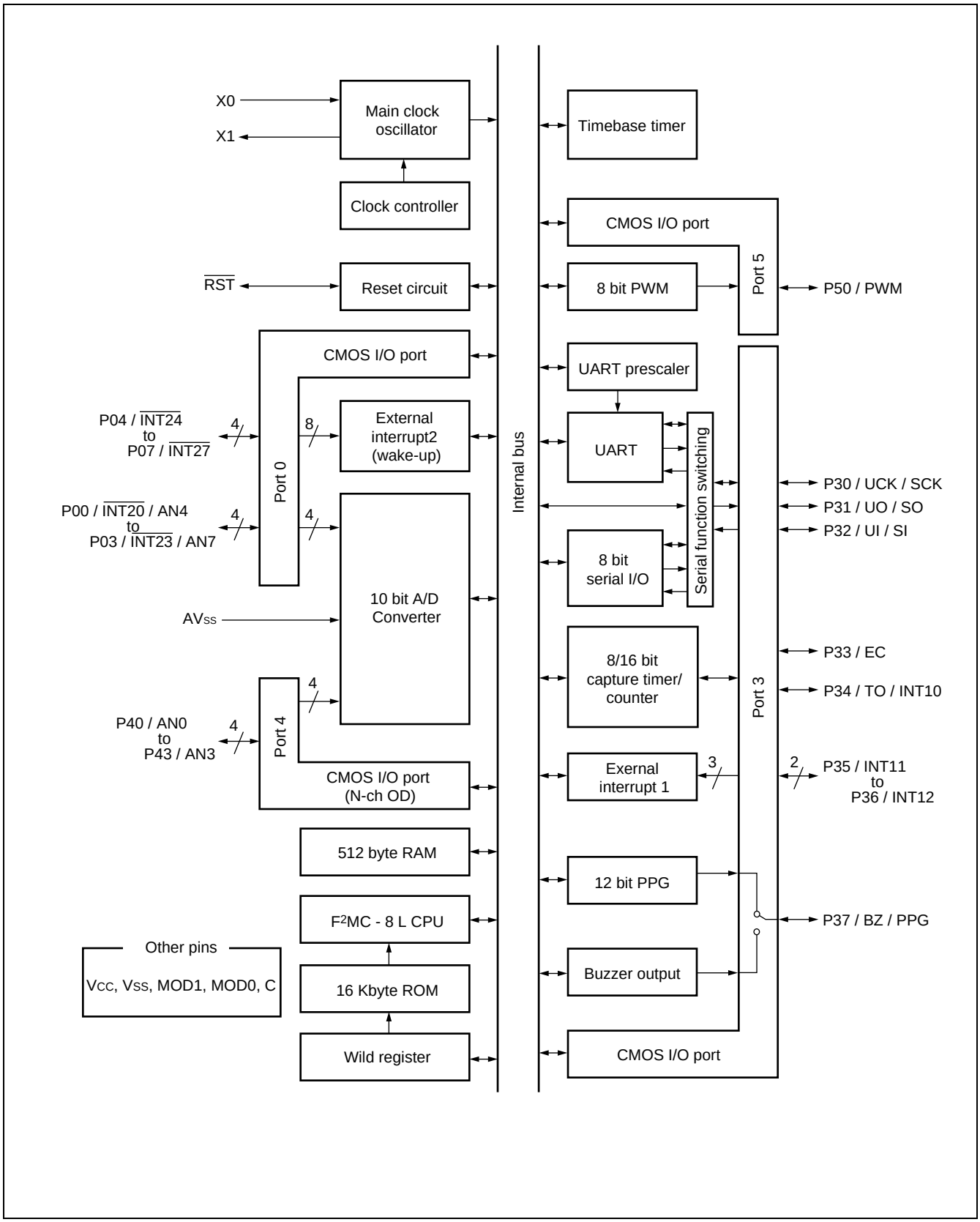
To program to the OTPROM using an EPROM programmer AF200, use the programming adapter (manufacturer : Sun Hayato Co., Ltd.) listed below.

Adaptor socket : ROM3-FPT30M02-8L

Inquiry : Sun Hayato Co., Ltd. : TEL (81) -3-3986-0403

FAX (81) -3-5396-9106

■ BLOCK DIAGRAM

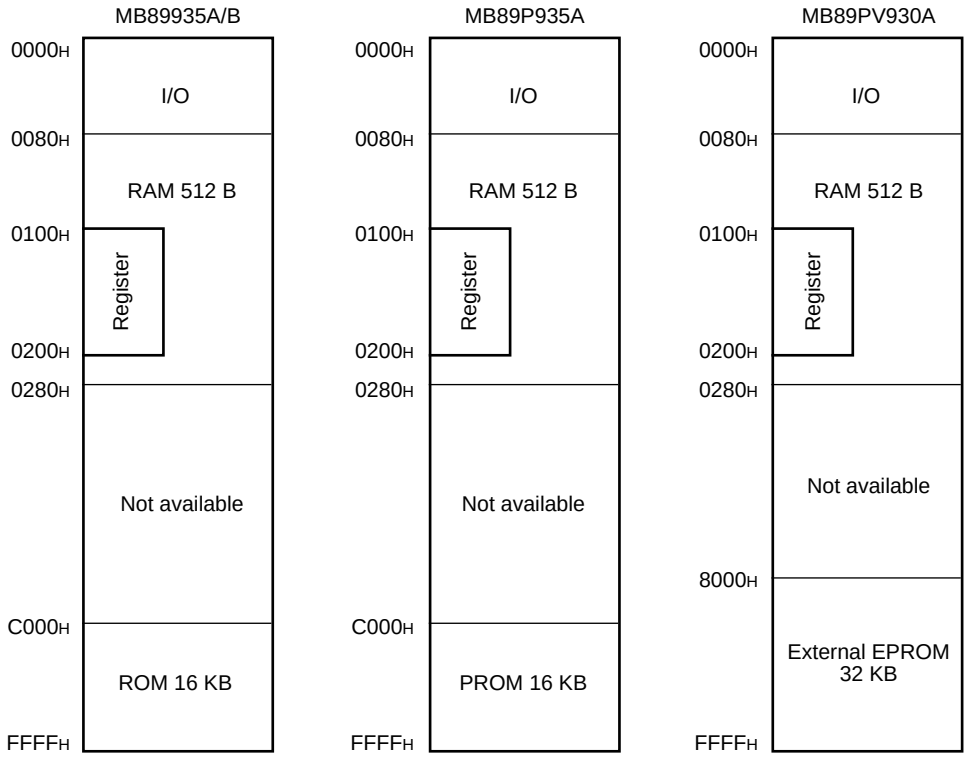


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89930A series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89930A series is structured as illustrated below.

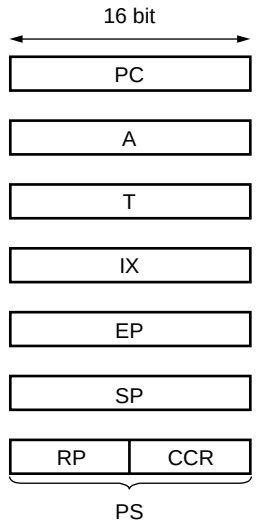
- **Memory Space**



2. Registers

The MB89930A series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided :

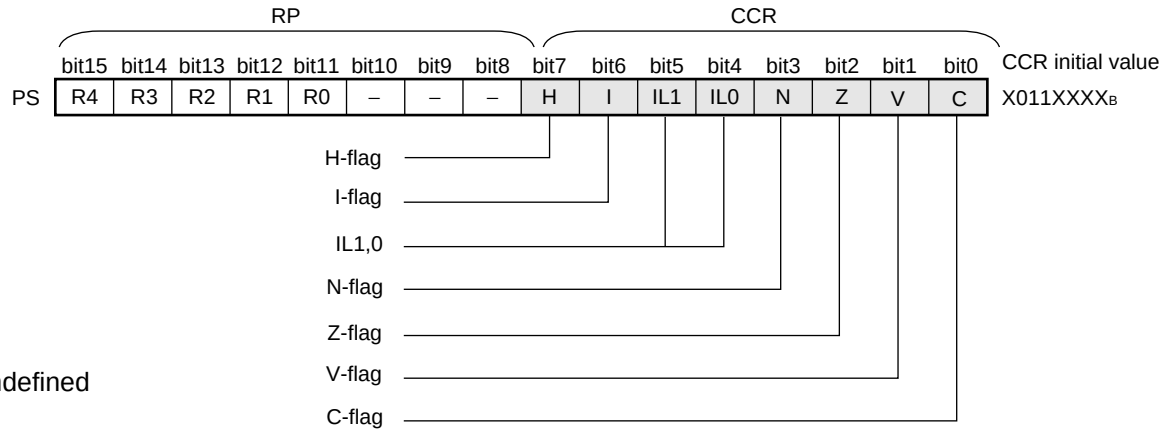
Program counter (PC) :	A 16-bit register for indicating instruction storage positions
Accumulator (A) :	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T) :	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX) :	A 16-bit register for index modification
Extra pointer (EP) :	A 16-bit pointer for indicating a memory address
Stack pointer (SP) :	A 16-bit register for indicating a stack area
Program status (PS) :	A 16-bit register for storing a register pointer, a condition code



	Initial value
: Program counter	$FFFD_H$
: Accumulator	Indeterminate
: Temporary accumulator	Indeterminate
: Index register	Indeterminate
: Extra pointer	Indeterminate
: Stack pointer	Indeterminate
: Program status	I-flag = 0, IL1, 0 = 11 The other bit values are indeterminate.

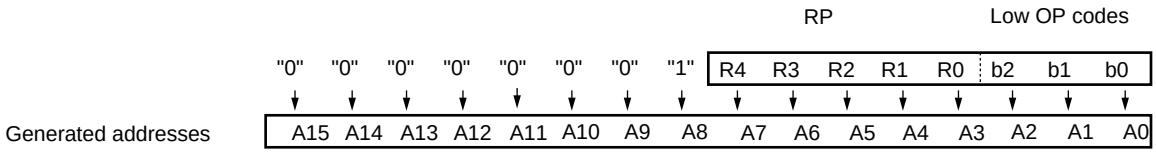
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR) . (See the diagram below.)

- **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag : Set to “1” when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. This flag is for decimal adjustment instructions.

I-flag : Interrupt is enabled when this flag is set to “1”. Interrupt is disabled when the flag is cleared to “0”. Cleared to “0” at the reset.

IL1, 0 : Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High ↕ Low = no interrupt
0	1		
1	0	2	
1	1	3	

N-flag : Set to “1” if the MSB becomes to “1” as the result of an arithmetic operation. Cleared to “0” when the bit is cleared to “0”.

Z-flag : Set to “1” when an arithmetic operation results in 0. Cleared otherwise.

V-flag : Set to “1” if the complement on 2 overflows as a result of an arithmetic operation. Cleared to “0” if the overflow does not occur.

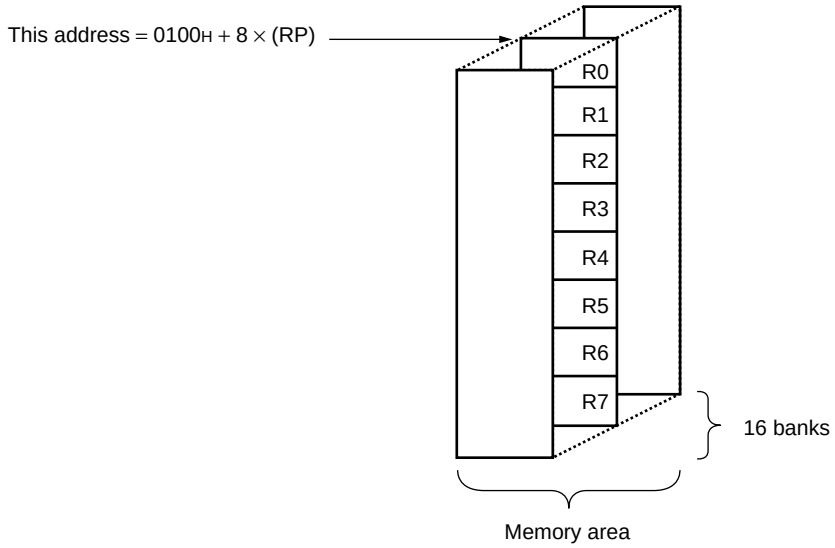
C-flag : Set to “1” when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to “0” otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided :

General-purpose registers : An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89930A series. The bank currently in use is indicated by the register bank pointer (RP) ..

- **Register Bank Configuraiton**



■ I/O MAP

Address	Register name	Register description	Read/write	Initial value
0000H	PDR0	Port 0 data register	R/W	X X X X X X X X
0001H	DDR0	Port 0 data direction register	W	0 0 0 0 0 0 0 0
0002H to 00006H	Vacancy			
0007H	SYCC	System clock control register	R/W	1 - - MM1 0 0
0008H	STBC	Standby control register	R/W	0 0 0 1 0 - - -
0009H	WDTC	Watchdog timer control register	W	0 - - - X X X X
000AH	TBTC	Timebase timer control register	R/W	0 0 - - - 0 0 0
000BH	Vacancy			
000CH	PDR3	Port 3 data register	R/W	X X X X X X X X
000DH	DDR3	Port 3 data direction register	W	0 0 0 0 0 0 0 0
000EH	RSFR	Reset flag register	R	X X X X - - - -
000FH	PDR4	Port 4 data register	R/W	- - - - X X X X
0010H	DDR4	Port 4 data direction register	R/W	- - - - 0 0 0 0
0011H	OUT4	Port 4 output format register	R/W	- - - - 0 0 0 0
0012H	PDR5	Port 5 data register	R/W	- - - - - - - X
0013H	DDR5	Port 5 data direction register	R/W	- - - - - - - 0
0014H	RCR21	12-bit PPG control register 1	R/W	0 0 0 0 0 0 0 0
0015H	RCR22	12-bit PPG control register 2	R/W	- - 0 0 0 0 0 0
0016H	RCR23	12-bit PPG control register 3	R/W	0 - 0 0 0 0 0 0
0017H	RCR24	12-bit PPG control register 4	R/W	- - 0 0 0 0 0 0
0018H	BZCR	Buzzer register	R/W	- - - - - 0 0 0
0019H	TCCR	Capture control register	R/W	0 0 0 0 0 0 0 0
001AH	TCR1	Timer 1 control register	R/W	0 0 0 0 0 0 0 0
001BH	TCR0	Timer 0 control register	R/W	0 0 0 - 0 0 0 0
001CH	TDR1	Timer 1 data register	R/W	X X X X X X X X
001DH	TDR0	Timer 0 data register	R/W	X X X X X X X X
001EH	TCPH	Capture data register H	R	X X X X X X X X
001FH	TCPL	Capture data register L	R	X X X X X X X X
0020H	TCR2	Timer output control register	R/W	- - - - - - 0 0
0021H	Vacancy			
0022H	CNTR	PWM control register	R/W	0 - 0 0 0 0 0 0
0023H	COMR	PWM compare register	W	X X X X X X X X
00024H	EIC1	External interrupt 1 Control register 1	R/W	0 0 0 0 0 0 0 0

(Continued)

Address	Register name	Register description	Read/write	Initial value
0025H	EIC2	External interrupt 1 Control register 2	R/W	- - - - 0 0 0 0
0026H	Vacancy			
0027H				
0028H	SMC	Serial mode control register	R/W	0 0 0 0 0 - 0 0
0029H	SRC	Serial rate control register	R/W	- - 0 1 1 0 0 0
002AH	SSD	Serial status and data register	R/W	0 0 1 0 0 - 1 X
002BH	SIDR	Serial input data register	R	X X X X X X X X
	SODR	Serial output data register	W	X X X X X X X X
002CH	UPC	Clock division selection register	R/W	- - - - 0 0 1 0
002DH to 0002FH	Vacancy			
0030H	ADC1	A/D converter control register 1	R/W	- 0 0 0 0 0 0 0
0031H	ADC2	A/D converter control register 2	R/W	- 0 0 0 0 0 0 1
0032H	ADDH	A/D converter data register H	R/W	- - - - - - X X
0033H	ADDL	A/D converter data register L	R/W	X X X X X X X X
0034H	ADEN	A/D enable register	R/W	0 0 0 0 0 0 0 0
0035H	Vacancy			
0036H	EIE2	External interrupt 2 control register1	R/W	0 0 0 0 0 0 0 0
0037H	EIF2	External interrupt 2 control register2	R/W	- - - - - - - 0
0038H	Vacancy			
0039H	SMR	Serial mode register	R/W	0 0 0 0 0 0 0 0
003AH	SDR	Serial data register	R/W	X X X X X X X X
003BH	SSEL	Serial function switching register	R/W	- - - - - - - 0
003CH to 003FH	Vacancy			
0040H	WRARH0	Upper-address setting register	R/W	X X X X X X X X
0041H	WRARL0	Lower-address setting register	R/W	X X X X X X X X
0042H	WRDR0	Data setting register 0	R/W	X X X X X X X X
0043H	WRARH1	Upper-address setting register	R/W	X X X X X X X X
0044H	WRARL1	Lower-address setting register	R/W	X X X X X X X X
0045H	WRDR1	Data setting register 1	R/W	X X X X X X X X
0046H	WREN	Address comparison EN registor	R/W	X X X X X 0 0
0047H	WROR	Wild-register data test register	R/W	- - - - - - 0 0
0048H to 006FH	Vacancy			
0070H	PUL0	Port-0 pull-up setting register	R/W	0 0 0 0 0 0 0 0

(Continued)

(Continued)

Address	Register name	Register description	Read/write	Initial value
0071H	PUL3	Port-3 pull-up setting register	R/W	0 0 0 0 0 0 0 0
0072H	PUL5	Port-5 pull-up setting register	R/W	- - - - - - - 0
0073H to 007AH	Vacancy			
007BH	ILR1	Interrupt level setting register1	W	1 1 1 1 1 1 1 1
007CH	ILR2	Interrupt level setting register2	W	1 1 1 1 1 1 1 1
007DH	ILR3	Interrupt level setting register3	W	1 1 1 1 1 1 1 1
007EH	ILR4	Interrupt level setting register4	W	1 1 1 1 1 1 1 1
007FH	ITR	Interrupt test register	Not available	- - - - - - 0 0

- : Unused, X : Undefined, M : Set using the mask option

Note : Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

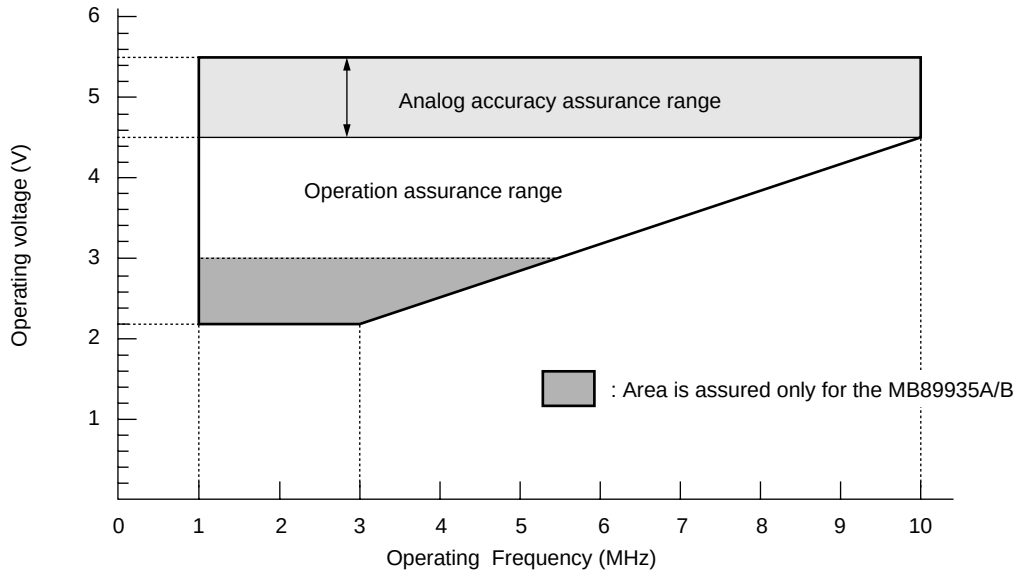
1. Absolute Maximum Ratings

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
Input voltage	V_I	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_O	V_{SS} – 0.3	V_{CC} + 6.0	V	
“L” level maximum output current	I_{OL1}	—	20	mA	Pins P40 to P43
	I_{OL2}	—	10	mA	Pins excluding P40 to P43
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating rate)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“H” level maximum output current	I_{OH}	—	–10	mA	
“H” level average output current	I_{OHAV}	—	–2	mA	Average value (operating current × operating rate)
“H” level total maximum output current	ΣI_{OH}	—	–50	mA	
Power consumption	Pd	—	200	mW	
Operating temperature	Ta	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2	5.5	V	Normal operation assurance range MB89935A/B
		1.5	6.0	V	Retains the RAMstate in stop mode
"H" level input voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	P00 to P07, P30 to P37, P40 to P43, P50, UI/SI
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	MOD0/1, $\overline{RST}$, EC, $\overline{INT20}$ to $\overline{INT27}$, UCK/SCK, INT10 to INT12
"L" level input voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	P00 to P07, P30 to P37, P40 to P43, P50, UI/SI
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	MOD0/1, $\overline{RST}$, EC, $\overline{INT20}$ to $\overline{INT27}$, UCK/SCK, INT10 to INT12
Open-drain output pin application voltage	V_D	V_{SS} – 0.3	V_{CC} + 0.3	V	P40 to P43
Operating temperature	Ta	–40	+85	°C	



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, F_{CH} = 10 MHz (External clock) , Ta = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P30 to P37, P40 to P43, P50 , UI/SI	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MOD0/1, UCK/SCK, EC, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{IL}	P00 to P07, P30 to P37, P40 to P43, P50 , UI/SI	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MOD0/1, UCK/SCK, EC, $\overline{INT20}$ to $\overline{INT27}$, INT10 to INT12	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_D	P40 to P43	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
"H" level output voltage	V_{OH}	P00 to P07, P30 to P37, P40 to P43, P50	I_{OH} = –4.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P30 to P37, P50, $\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P40 to P43	I_{OL} = 12.0 mA	—	—	0.4	V	
Input leakage current	I_{LI}	P00 to P07, P30 to P37, P40 to P43, P50 , MOD0/1	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P30 to P37, P40 to P43, P50	V_I = 0.0 V	25	50	100	kΩ	
Power supply current	I_{CC}	V_{CC} Normal operation mode (External clock, highest gear speed)	When A/D converter stops	—	8	12	mA	MB89935A/B
				—	6	9	mA	MB89P935A
			When A/D converter starts	—	10	15	mA	MB89935A/B
				—	8	12	mA	MB89P935A
	I_{CCS}	Sleep mode (External clock, highest gear speed)	When A/D converter stops	—	4	6	mA	MB89935A/B
				—	3	5	mA	MB89P935A

(Continued)

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(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, F_{CH} = 10 MHz (External clock) , Ta = –40 °C to +85 °C)

Parameter	Sym-bol	Pin name		Condition	Value			Unit	Remarks
					Min.	Typ.	Max.		
Power supply current	I_{CCH}	V_{CC}	Stop mode Ta = +25 °C (External clock)	When A/D converter stops	—	—	1	µA	MB89935A/B
					—	—	10	µA	MB89P935A
Input capacitance	C_{IN}	Other than AV_{SS}, V_{CC}, V_{SS}		—	—	10	—	pF	MB89P935A

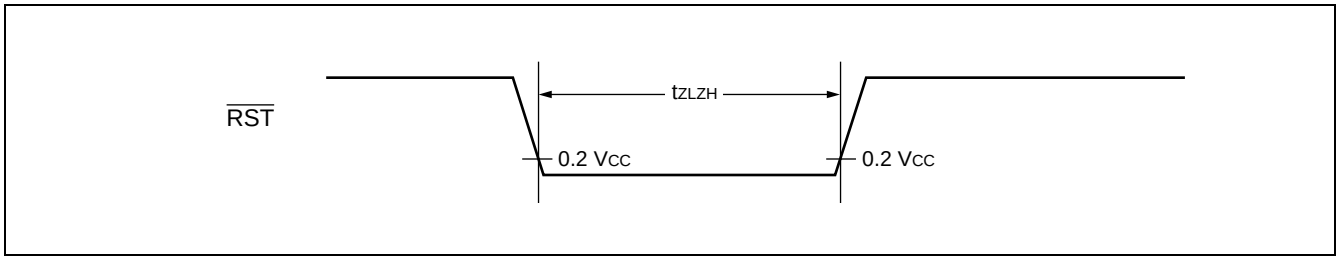
4. AC Characteristics

(1) Reset Timing

(AV_{SS} = V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	16 t_{HCYL}	—	ns	

t_{HCYL} : 1 oscillating clock cycle time

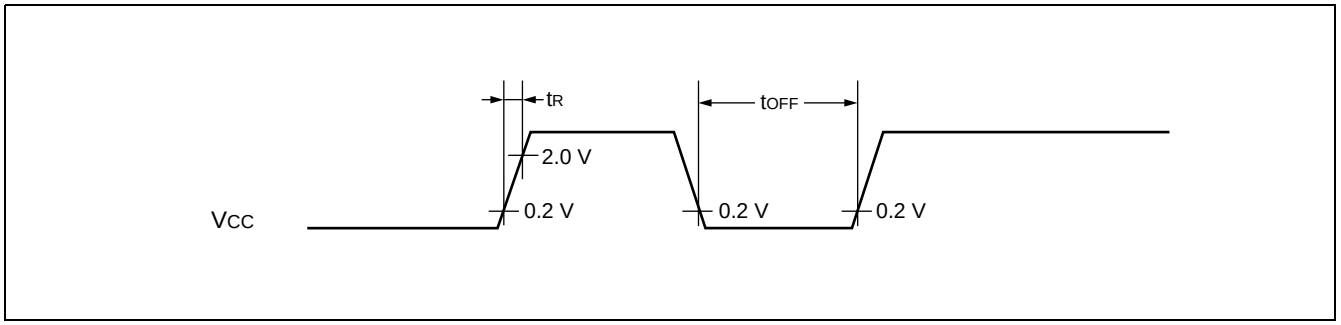


Note : When the power-on reset option is not on, leave the external reset on until oscillation becomes stable.

(2) Power-on Reset

(AV_{SS} = V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	
Power supply cutoff time	t_{OFF}		1	—	ms	Due to repeated operations



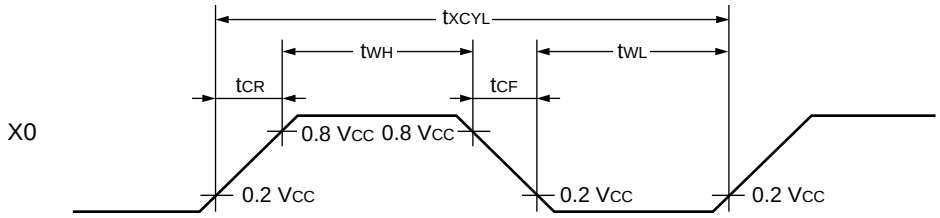
Note : The supply voltage must be set to the minimum value required for operation within the prescribed default oscillation settling time.

(3) Clock Timing

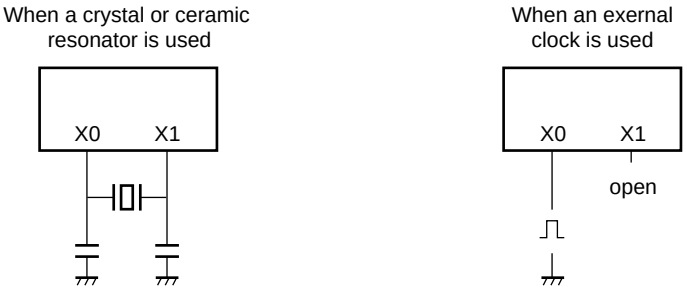
(AV_{SS} = V_{SS} = 0.0 V, Ta = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Clock frequency	F_{CH}	—	1	10	MHz	
Clock cycle time	t_{XCYL}		100	1000	ns	
Input clock pulse width	t_{WH} t_{WL}		20	—	ns	
Input clock rising/falling time	t_{CR} t_{CF}		—	10	ns	

- **X0 and X1 Timing and Conditions**



- **Main Clock Conditions**

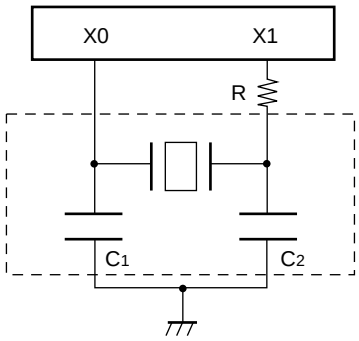


(4) Instruction Cycle.

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{INST}	4/F_{CH}, 8/F_{CH}, 16/F_{CH}, 64/F_{CH}	µs	t_{INST} = 0.4 µs when operating at F_{CH} = 10 MHz (4/F_{CH})

(5) Recommended Resonator Manufactures

- **Sample application of ceramic resonator**



Resonator manufacturer	Resonator	Frequency (MHz)	C_1	C_2	R
Murata Mfg. Co., Ltd.	CSTS0400MG06	4.00	Built-in	Built-in	330 Ω
	CSTCC4.00MG0H6	4.00	Built-in	Built-in	330 Ω
	CSTS0800MG06	8.00	Built-in	Built-in	Not required
	CSTCC8.00MG0H6	8.00	Built-in	Built-in	Not required
	CST10.0MTW	10.00	Built-in	Built-in	Not required
	CSTCC10.0MG0H6	10.00	Built-in	Built-in	Not required

Inquiry : Murata Mfg. Co., Ltd.

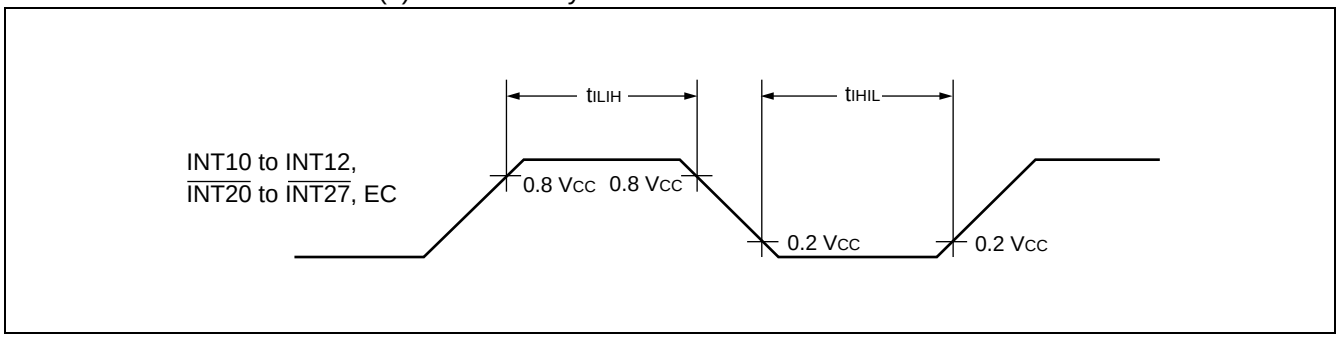
- Murata Electronics North America, Inc. : TEL1-404-436-1300
- Murata Europe Management GmbH : TEL 49-911-66870
- Murata Electronics Singapore (Pte.) : TEL 65-758-4233

(6) Peripheral Input Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

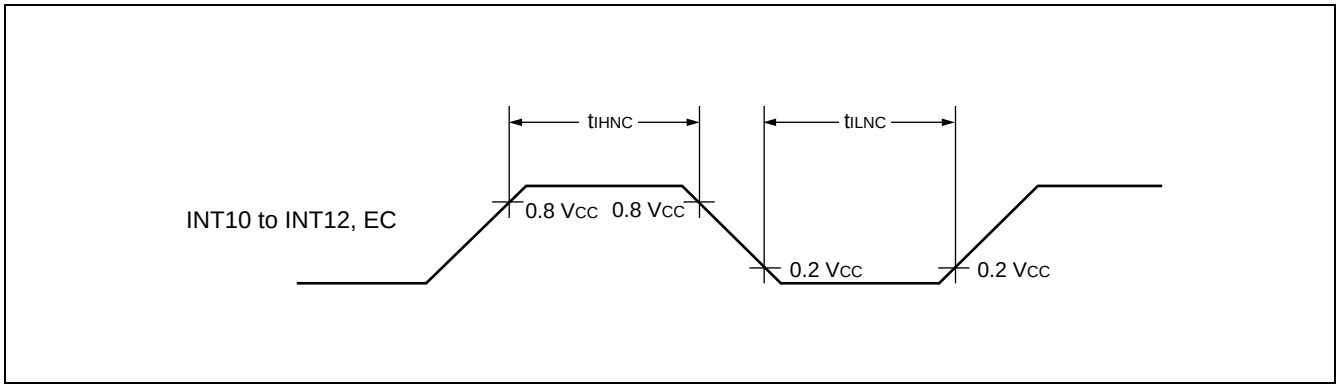
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width	t_{ILIH}	INT10 to INT12, INT20 to INT27, EC	2 t_{INST}*	—	µs	
Peripheral input “L” pulse width	t_{IHIL}		2 t_{INST}*	—	µs	

* : For information on t_{INST} see “ (4) Instruction Cycle”.



(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input “H” noise limit	t_{IHNC}	INT10 to INT12, EC	7	15	23	ns	
Peripheral input “L” noise limit	t_{ILNC}		7	15	23	ns	



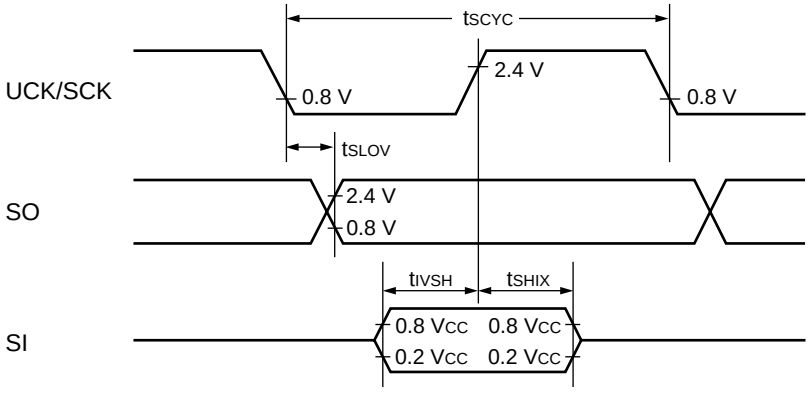
(7) UART, Serial I/O Timing

(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

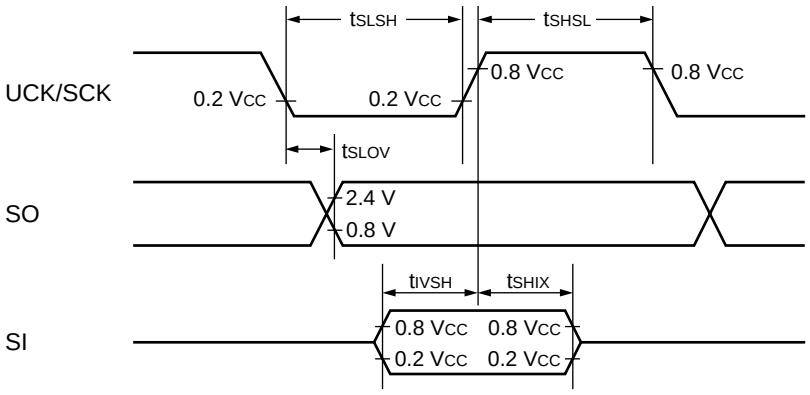
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	UCK/SCK	Internal shift clock mode	2 t_{INST}*	—	µs	
UCK/SCK ↓ → SO time	t_{SLOV}	UCK/SCK, SO		–200	200	ns	
Valid SI → UCK/SCK↑	t_{IVSH}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	
UCK/SCK ↑ → Valid SI hold time	t_{SHIX}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	UCK/SCK	External shift clock mode	t_{INST}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	UCK/SCK		t_{INST}*	—	µs	
UCK/SCK ↓ → SO time	t_{SLOV}	UCK/SCK, SO		0	200	ns	
Valid SI → UCK/SCK	t_{IVSH}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	
UCK/SCK ↑ → Valid SI hold time	t_{SHIX}	UCK/SCK, SI		1/2 t_{INST}*	—	µs	

* : For information on t_{inst}, see “ (4) Instruction Cycle”.

- **Internal Shift Clock Mode**



- **External Shift Clock Mode**



5. A/D Converter

(1) A/D Converter Electrical Characteristics

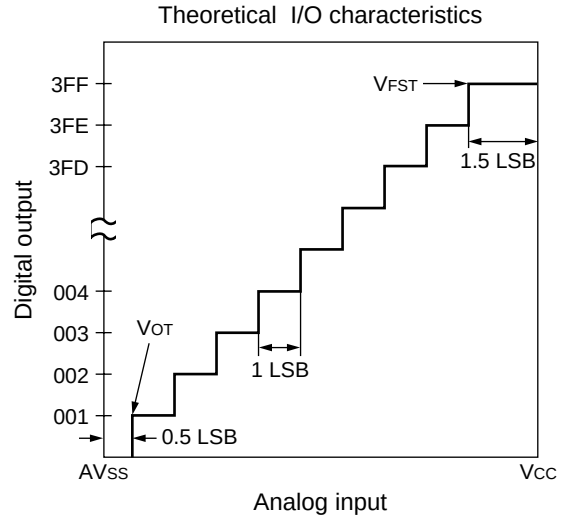
(V_{CC} = 5.0 V ± 10%, AV_{SS} = V_{SS} = 0.0 V, Ta = –40 °C to +85 °C)

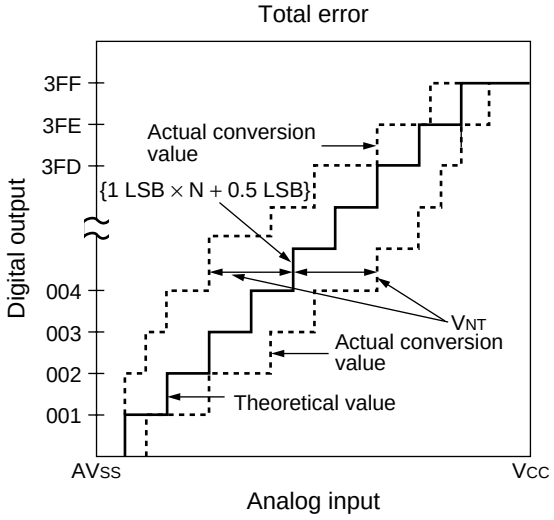
Parameter	Symbol	Value			Unit	Remarks
		Min.	Typ.	Max.		
Resolution	—	—	—	10	bit	
Total error		–5.0	—	+5.0	LSB	
Linearity error		–3.0	—	+3.0	LSB	
Differential linearity error		–2.5	—	+2.5	LSB	
Zero transition voltage	V_{OT}	AV_{SS} – 3.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 4.5 LSB	V	
Full-scale transition voltage	V_{FST}	V_{CC} – 6.5 LSB	V_{CC} – 1.5 LSB	V_{CC} + 2.0 LSB	V	
A/D mode conversion time		—	—	38 t_{INST}*	µs	
Analog port input current	I_{AIN}	—	—	10	µA	
Analog input voltage range	—	0	—	V_{CC}	V	

* : For information on t_{inst}, see “ (4) Instruction Cycle” in “4. AC Characteristics.”

(2) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 10, analog voltage can be divided into 2^{10} = 1024.
- Linearity error (unit : LSB)
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error (unit : LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit : LSB)
  The difference between theoretical and actual conversion values

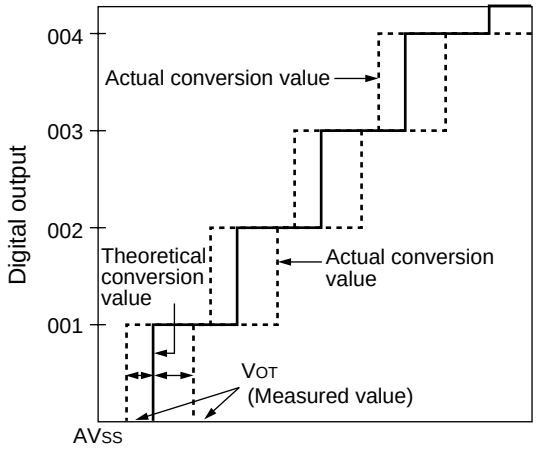




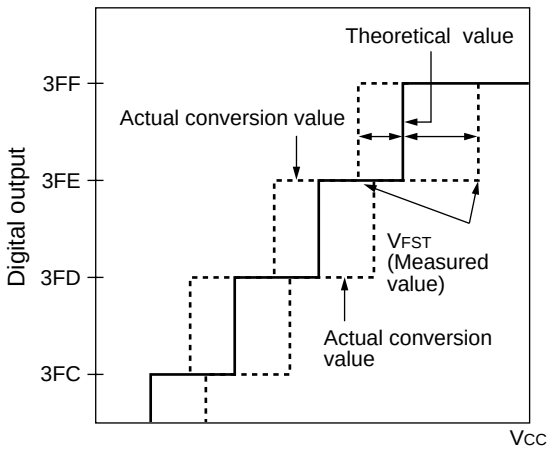
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ \text{(V)}$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times \text{N} + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

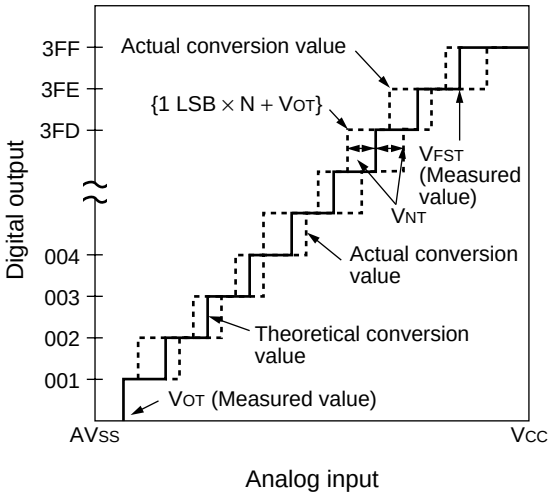
Zero transition error



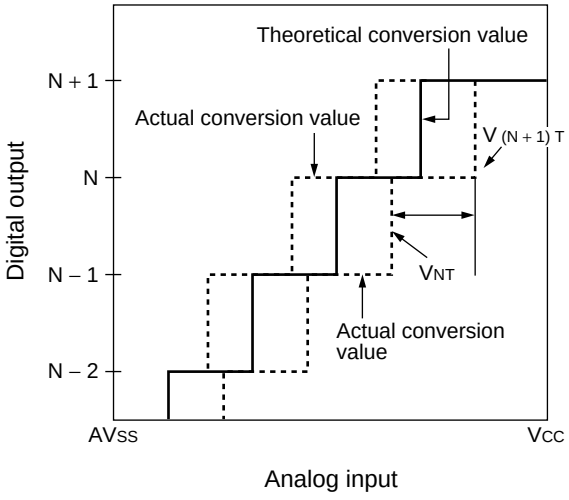
Full-scale transition error



Linearity error



Differential linearity error



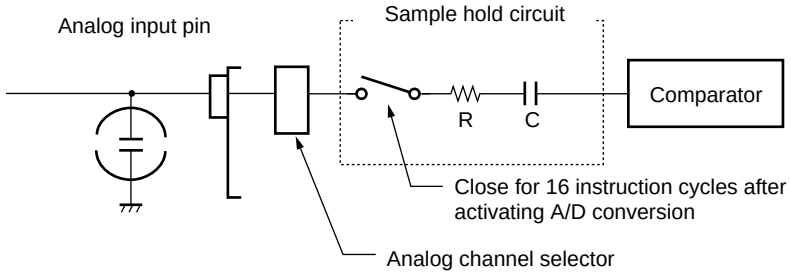
$$\text{Linearity error of digital output } N = \frac{V_{NT} - \{1\ \text{LSB} \times N + V_{OT}\}}{1\ \text{LSB}}$$

$$\text{Differential linearity of error digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1$$

(3) Notes on Using A/D Converter

- Input impedance of the analog input pins
  The A/D converter used for the MB89930A series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for 16 instruction cycles after activating A/D conversion. For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low (below 4 kΩ) .
  Note that if the impedance cannot be kept low, it is recommended to connect an external capacitor of about 0.1 μF for the analog input pin.

- **Analog Input Equivalent Circuit**



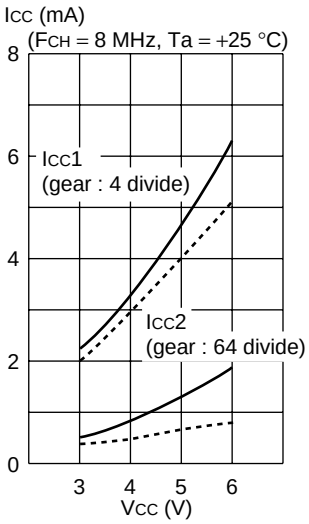
If the analog input impedance is higher than 4 kΩ, it is recommended to connect an external capacitor of approx. 0.1 μF.

- Error
  The smaller the | V_{CC} – AV_{SS} |, the greater the error would become relatively.

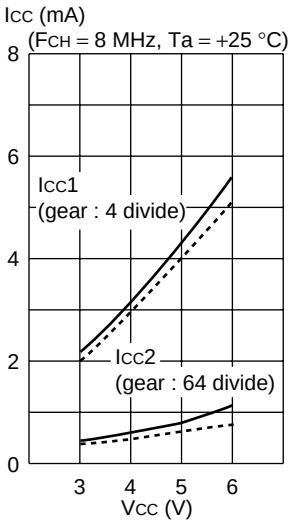
■ EXAMPLE CHARACTERISTICS

- Power supply current (MB89935A/MB89935B/MB89P935A : 8 MHz (when FAR resonator [NM8000] is used)

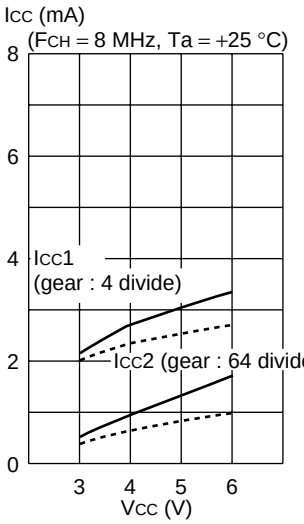
MB89935A
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})



MB89935B
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})

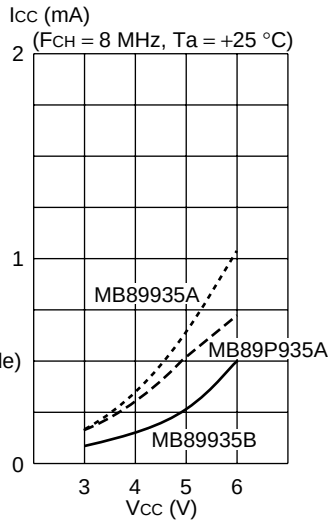


MB89P935A
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})



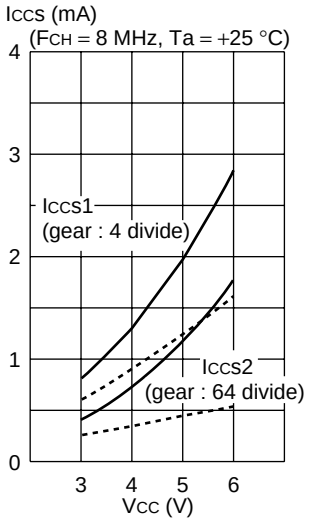
MB89935A/MB89935B/
MB89P935A/

FAR : [NM8000]

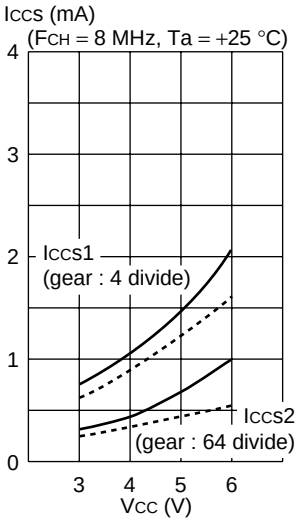


FAR : [NM8000]
External clock

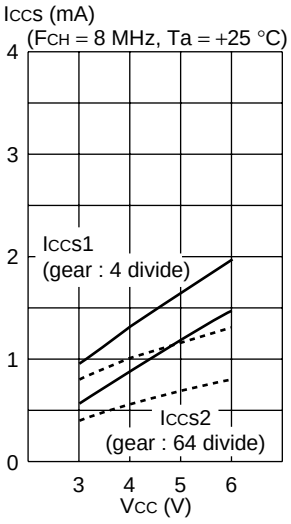
MB89935A
Sleep mode
($I_{CC}S1$ – V_{CC}, $I_{CC}S2$ – V_{CC})



MB89935B
Sleep mode
($I_{CC}S1$ – V_{CC}, $I_{CC}S2$ – V_{CC})

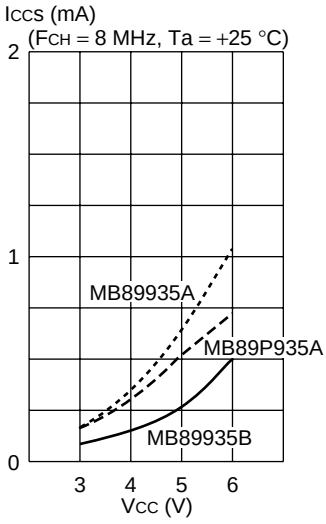


MB89P935A
Sleep mode
($I_{CC}S1$ – V_{CC}, $I_{CC}S2$ – V_{CC})



MB89935A/MB89935B/
MB89P935A/

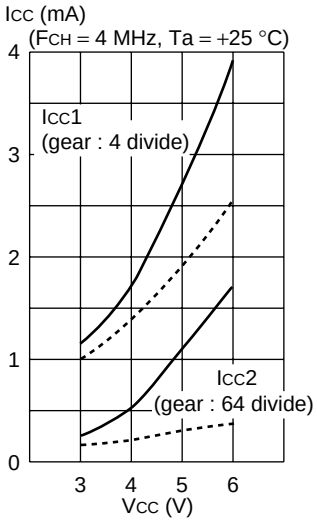
FAR : [NM8000]



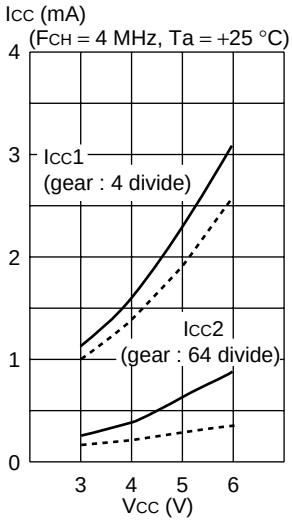
FAR : [NM8000]
External clock

• MB89935A/MB89935B/MB89P935A : 4 MHz (when FAR resonator [NM4000] used)

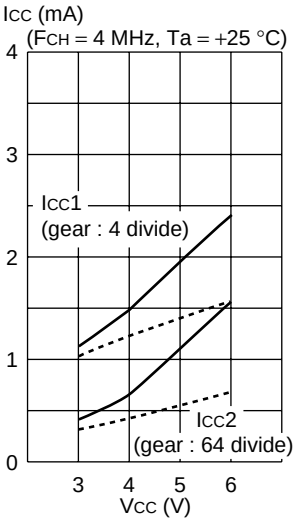
MB89935A
Normal operation mode
($I_{CC}1 – V_{CC}$, $I_{CC}2 – V_{CC}$)



MB89935B
Normal operation mode
($I_{CC}1 – V_{CC}$, $I_{CC}2 – V_{CC}$)

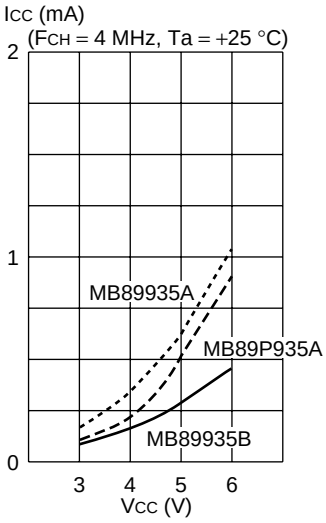


MB89P935A
Normal operation mode
($I_{CC}1 – V_{CC}$, $I_{CC}2 – V_{CC}$)



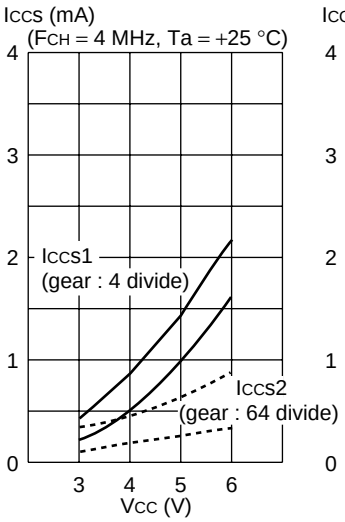
MB89935A/MB89935B/
MB89P935A/

FAR : [NM4000]

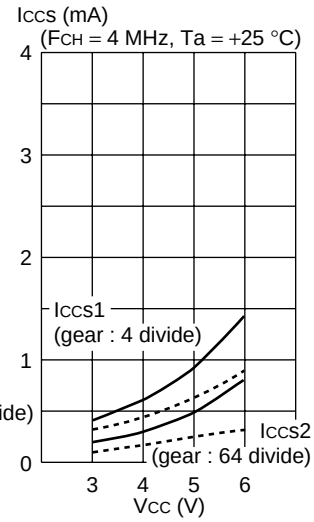


FAR : [NM4000]
External clock

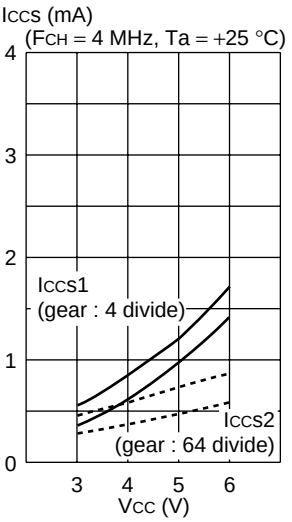
MB89935A
Seep mode
($I_{CC}S1 – V_{CC}$, $I_{CC}S2 – V_{CC}$)



MB89935B
Seep mode
($I_{CC}S1 – V_{CC}$, $I_{CC}S2 – V_{CC}$)

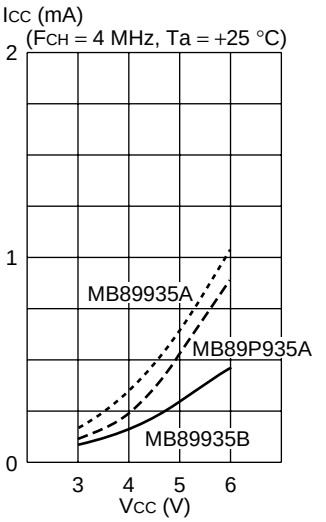


MB89P935A
Seep mode
($I_{CC}S1 – V_{CC}$, $I_{CC}S2 – V_{CC}$)



MB89935A/MB89935B/
MB89P935A/

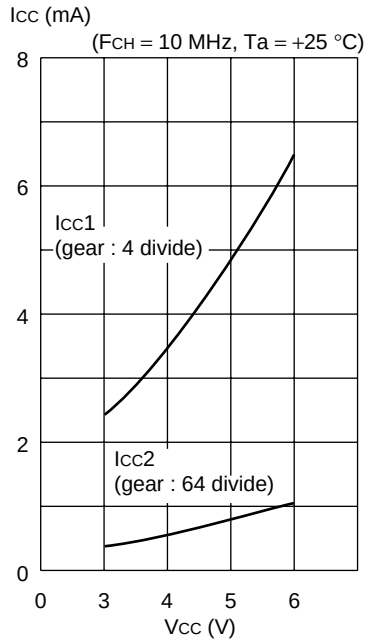
FAR : [NM4000]



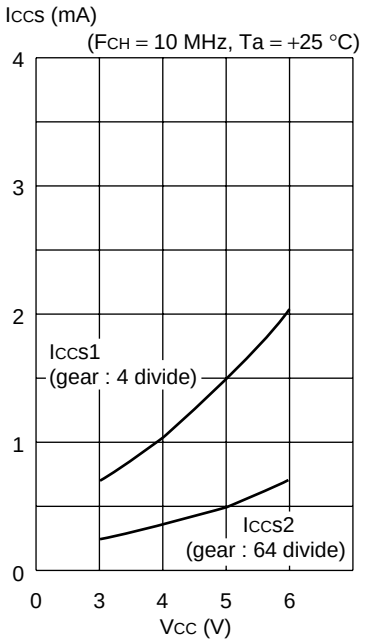
FAR : [NM4000]
External clock

- MB89935A/MB89935B : 10 MHz (when external clock is used)

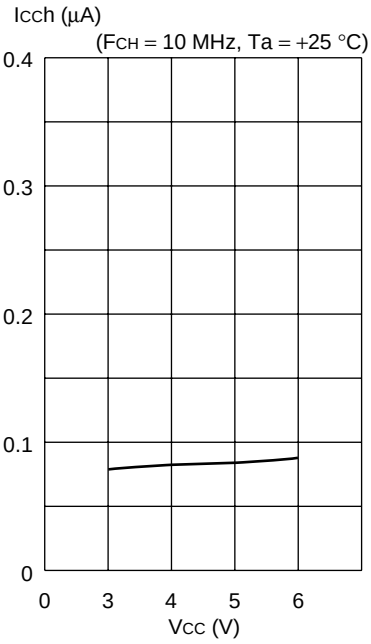
MB89935A/B
Normal operation mode
($I_{CC}1$ – V_{CC}, $I_{CC}2$ – V_{CC})



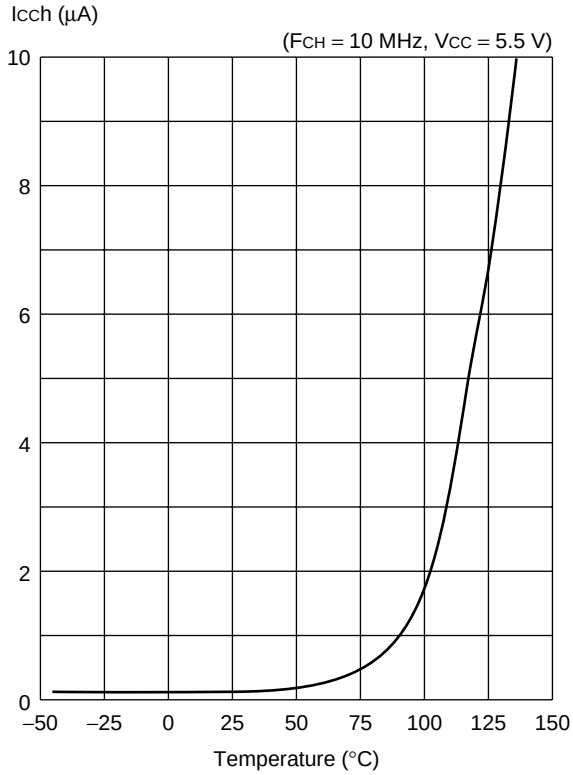
MB89935A/B
Normal operation mode
($I_{CCS}1$ – V_{CC}, $I_{CCS}2$ – V_{CC})



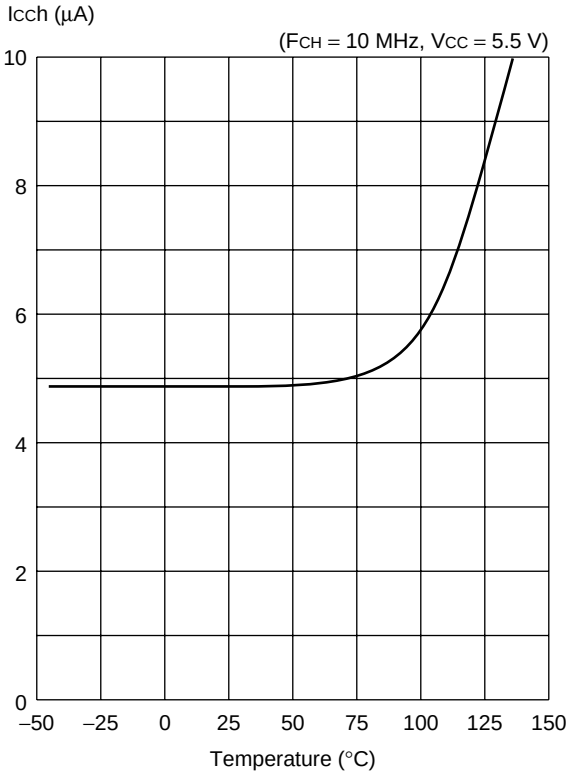
MB89935A/B
Normal operation mode
($I_{CC}h$ – V_{CC})



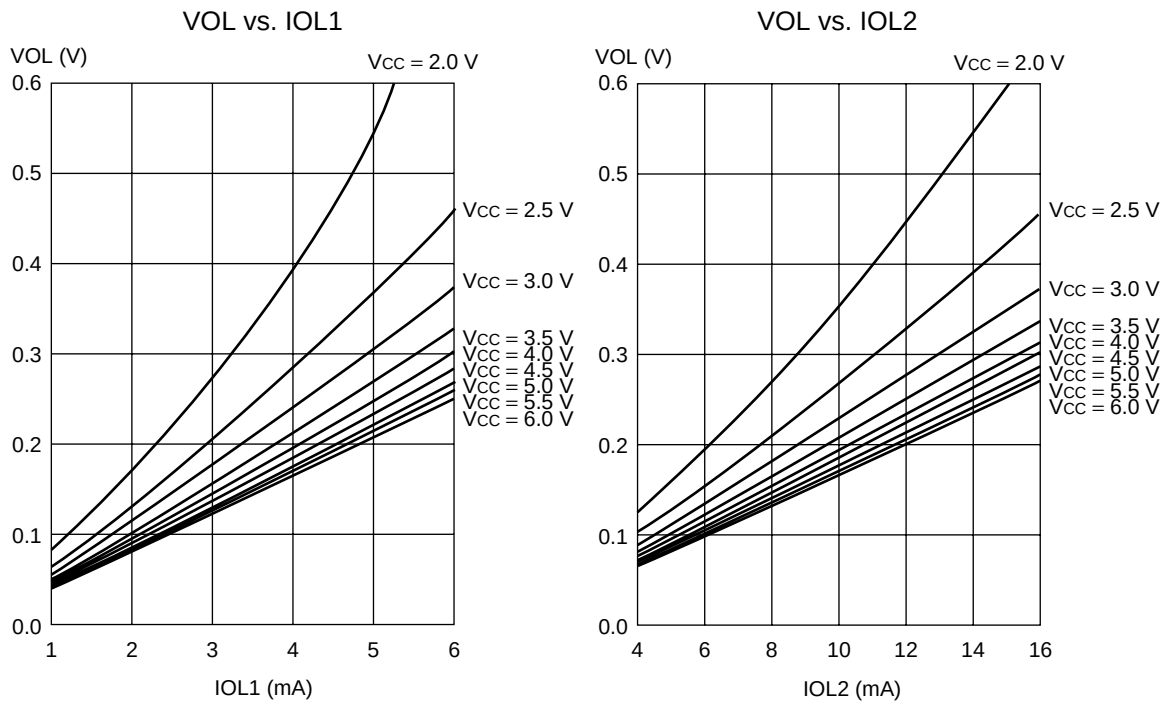
MB89935A/MB89935B
Stop mode ($I_{CC}h$ – V_{CC})



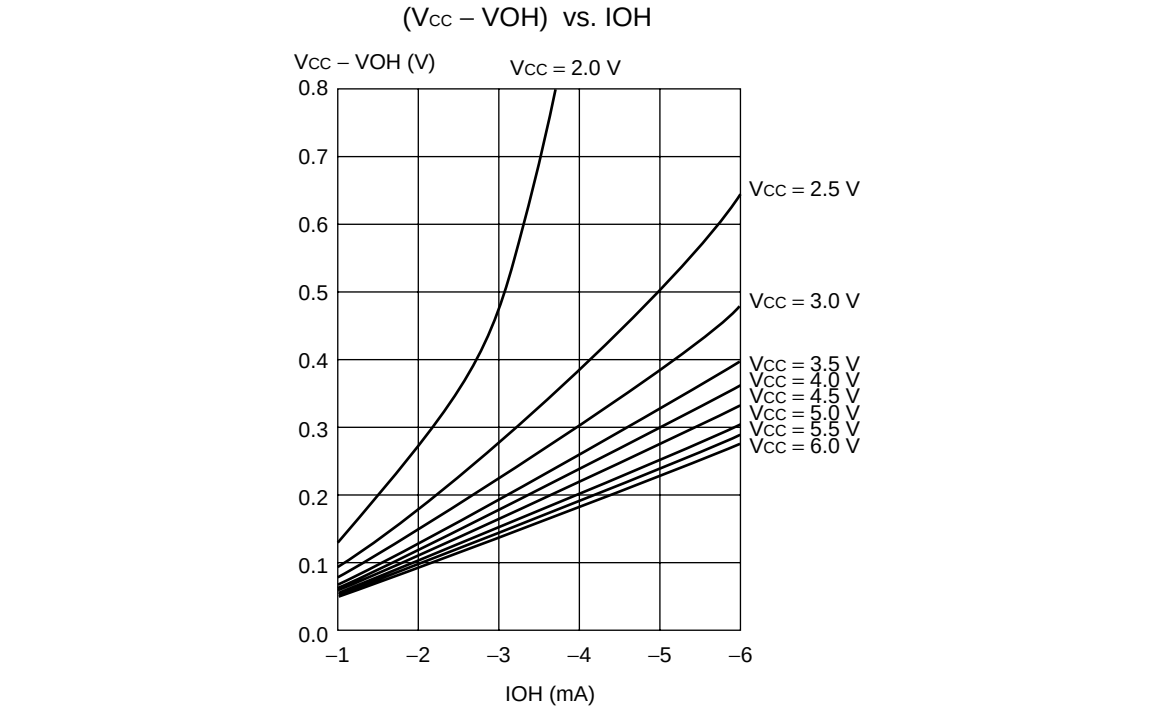
MB89P935A
Stop mode ($I_{CC}h$ – V_{CC})



(2) “L” level output voltage



(3) “H” level output voltage



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:
- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:
- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Note During byte transfer to A, T ← A is restricted to low bytes.
Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

No	Part number	MB89935A/B	MB89P935A	MB89PV930A
	Specifying procedure	Specify when ordering masking	Setting not possible	
1	Selection of initial value of main clock oscillation settling time* (with F_{CH} = 10 MHz) 01 : $2^{14}/F_{CH}$ (Approx.1.63 ms) 10 : $2^{17}/F_{CH}$ (Approx.13.1 ms) 11 : $2^{18}/F_{CH}$ (Approx.26.2 ms)	Selectable	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)	Fixed to $2^{18}/F_{CH}$ (Approx. 26.2 ms)
2	Power-on reset selection With power-on reset Without power-on reset	Selectable	Available	Available
3	Reset pin output With reset output Without reset output	Selectable	With reset output	With reset output

F_{CH} : Main clock oscillation frequency

* : Initial value to which the oscillation settling time bit (SYCC : WT1, WT0) in the system clock control register is set

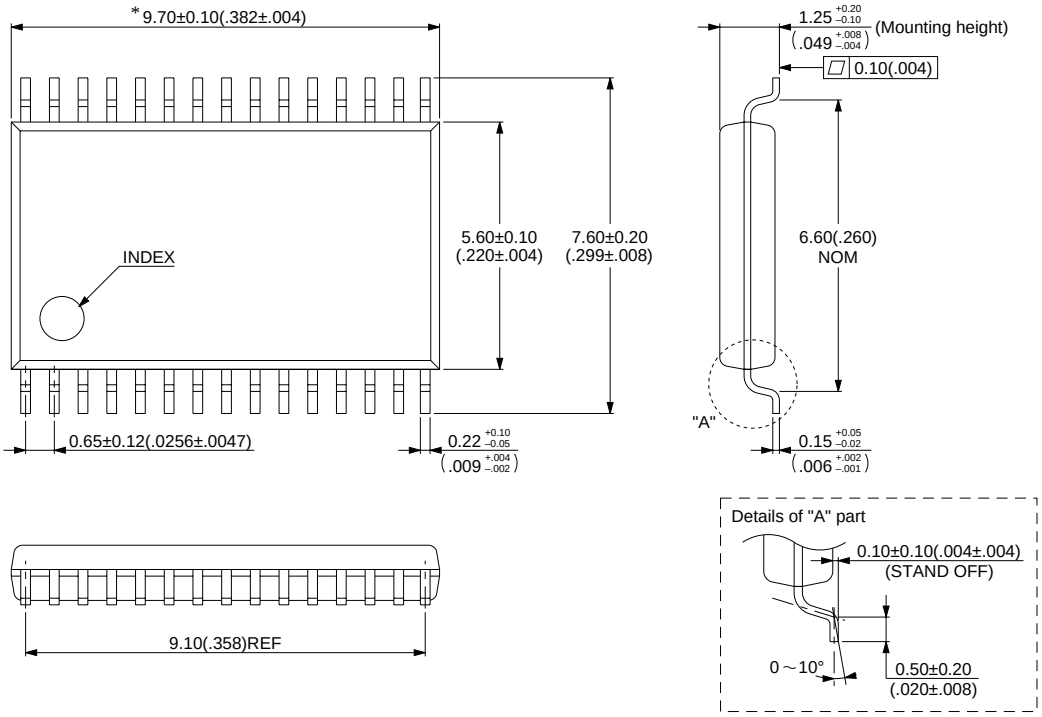
■ ORDERING INFORMATION

Part number	Package	Remarks
MB89935APFV MB89935BPFV MB89P935APFV	30-pin Plastic SSOP (FPT-30P-M02)	
MB89PV930ACFV	48-pin Ceramic MQFP (MQP-48C-P01)	

■ PACKAGE DIMENSIONS

30-pin plastic LQFP
(FPT-30P-M02)

* : This dimension does not include resin protrusion.



Dimensions in mm (inches)

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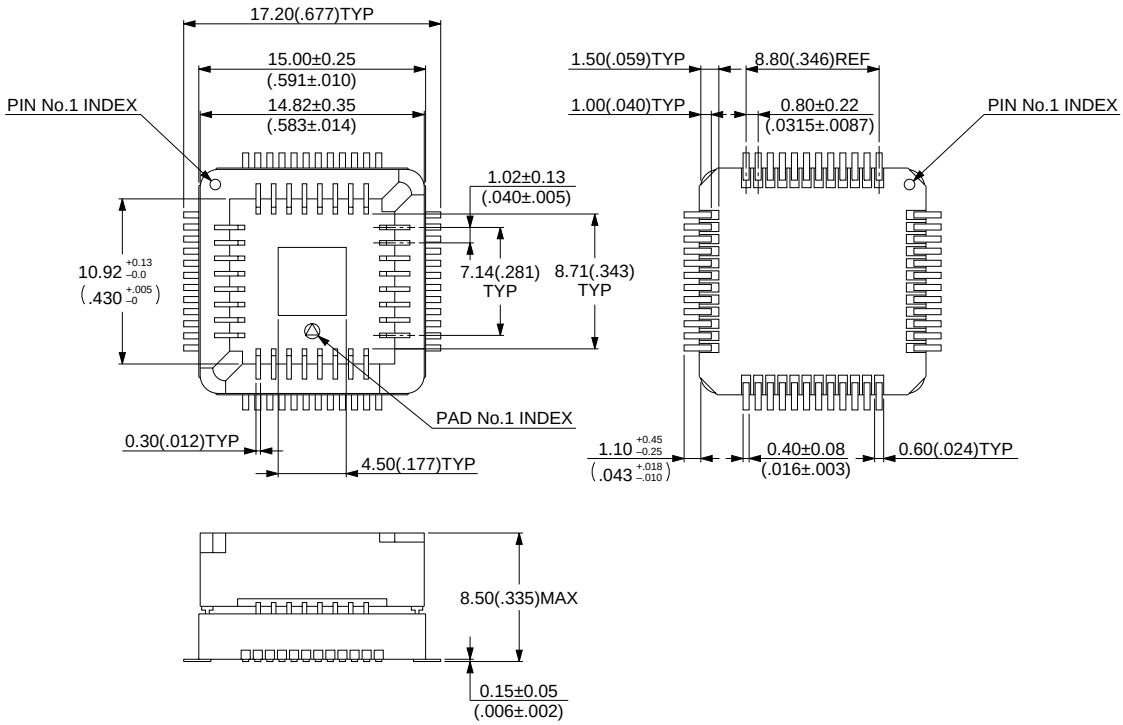
48-pin ceramic MQFP
(MQP-48C-P01)



Dimensions in mm (inches)

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