FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12526-1E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89920 Series

MB89923/925/P928/PV920

PRELIMINARY

■ DESCRIPTION

The MB89920 series is a line of single-chip microcontrollers using the F²MC*-8L CPU core which can operate at low voltage but at high speed.

The microcontrollers in this series contain peripheral functions such as a PWM timer, an input capture/output compare control counter, an LCD controller/driver, an A/D converter, and a UART.

The MB89920 series can suit a wide range of applications such as analog input conversion, pulse input measurement/pulse output control, serial communications control, and display control.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- High speed processing at low voltage
  Minimum execution time: 0.5 µs/8.0 MHz
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.
- 8-bit PWM timer: 2 channels (also usable as a reload timer)
- 16-bit input capture: 2 channels / 16-bit output compare: 2 channels

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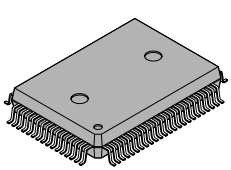
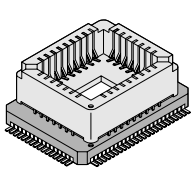
■ PACKAGE

80-pin Plastic QFP



(FPT-80P-M06)

80-pin Ceramic MQFP



(MQP-80C-P01)

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- 20-bit time-base counter
- UART: 1 channel (with asynchronous transfer mode and 8-bit synchronous serial mode)
- 8-bit serial interface: 1 channel (LSB first/MSB first selectability)
- 10-bit A/D converter: 8 channels
- LCD controller/driver: 28 segments × 4 commons (max. 112 pixels)
- Low-voltage detection reset
- Watchdog timer reset
- External interrupt: 4 channels
  Four channels are independent and capable of wake-up from the low-power consumption mode (with edge detection function)
- Buzzer output/clock output
- Low-power consumption modes:
  Stop mode (The software stops oscillation to minimize the current consumption.)
  Sleep mode (The CPU stops to reduce current consumption to approx. 1/3 of normal.)
  Hardware standby mode (The pin input stops oscillation.)

■ PRODUCT LINEUP

Parameter \ Part number	MB89923	MB89925	MB89P928	MB89PV920
Classification	Mass production products (mask ROM products)		One-time PROM product (for development)	Piggyback/evaluation product (for development)
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	48 K × 8 bits (internal PROM)	48 K × 8 bits (external ROM)
RAM size	256 × 8 bits	512 × 8 bits	1024 × 8 bits	
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.5 µs/8 MHz Interrupt processing time: 4.5 µs/8 MHz			
Ports	I/O ports (CMOS): 35 (25 ports also serve as peripherals.) I/O ports (N-ch open-drain): 34 (All also serve as peripherals.) Total: 69			
Options	Specify with mask options		Set with EPROM programmer	None
20-bit time-base timer	20 bits (interval time selection: 4.10 ms, 16.38 ms, 65.54 ms, 262 ms/8 MHz)			
Real-time I/O	16-bit timer: operating clock cycle (0.5 µs, 1.0 µs, 2.0 µs, 4.0 µs), overflow interrupt Input capture: 16 bits × 2 channels, external trigger edge selectability Output compare: 16 bits × 2 channels			
LCD controller/ driver	Common output: 4 (selectable from 2 to 4 by software) Segment output: 28 (can be switched to ports in 4-pin unit by software) Bias power supply pins: 3 LCD display RAM size: 14 × 8 bits Dividing resistor for LCD driving: bult-in (external resistor selectability)			
8-bit PWM timer	8 bits × 2-channel reload timer operation 8 bits × 2-channel PWM operation (4 cycles selectable) 8 bits × 1-channel PPG operation (4 oscillation clocks selectable)			
UART	Variable data length (7 or 8 bits), internal baud rate generator, error detection function, full-duplex with internal double buffer, NRZ transmission formation, Clock synchronous/asynchronous transfer capable			
8-bit serial I/O	8 bits, LSB first/MSB first selectability, One clock selectable from four transfer clocks (one external shift clock, three internal shift clocks: 1.0 µs, 4.0 µs, 16.0 µs)			
10-bit A/D converter	10-bit resolution × 8 channels A/D conversion mode (conversion time: 16.5 µs (33 instruction cycles)) Sense mode (conversion time: 9.0 µs (18 instruction cycles)) Continuous activation by an internal clock capable			
Watchdog timer	Interval time: approx. 130 to 260 ms			
Low-voltage detection reset	Reset activation voltage: 3.0 to 4.3 V Reset release voltage: 3.1 to 4.5 V			
Hardware standby	Stop the clock oscillation by pin input			
Buzzer/clock output	1 channel (output a frequency from 1 KHz, 2 KHz, 4 KHz, and divided clock frequency)			
External interrupt	4 channels (rising edge/falling edge selectability)			
Package	QFP-80			MQFP-80
Operating voltage	2.2 to 6.0 V*		2.7 to 6.0 V*	2.7 to 6.0 V*
EPROM for use	—			MBM27C512-20TV (LCC package)

* : The minimum operating voltage varies with conditions such as the operating frequencies, functions, and development tool.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89923 MB89925 MB89P928	MB89PV920
FPT-80P-M06	○	×
MQP-80C-P01	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.
- The external area is used.

2. Current Consumption

- In the case of the MB89PV920, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics.")

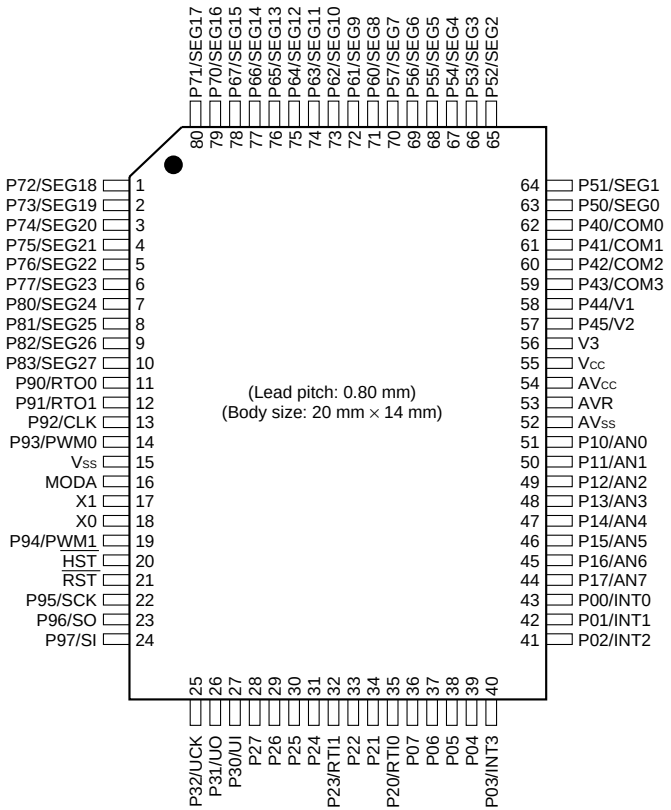
3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

Before using options check section "■ Mask Options."

■ PIN ASSIGNMENT

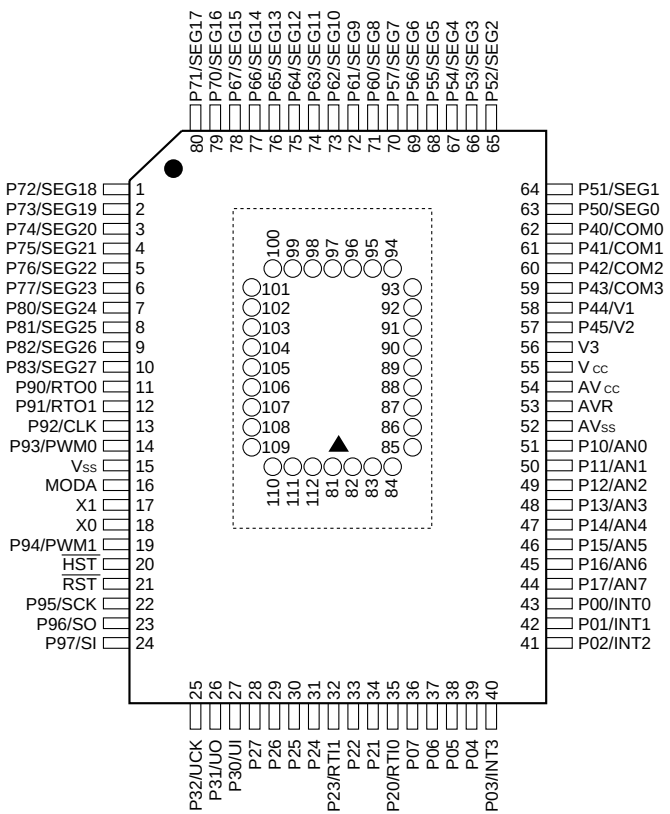
(Top view)



(FPT-80P-M06)

(Only for mass production or one-time PROM products)

(Top view)



(MQP-80C-P01)

- **Pin assignment on package top (only for piggyback/evaluation product)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
81	N.C.	89	AD2	97	N.C.	105	$\overline{OE}/V_{PP}$
82	A15	90	AD1	98	O4	106	N.C.
83	A12	91	AD0	99	O5	107	A11
84	AD7	92	N.C.	100	O6	108	A9
85	AD6	93	O1	101	O7	109	A8
86	AD5	94	O2	102	O8	110	A13
87	AD4	95	O3	103	$\overline{CE}$	111	A14
88	AD3	96	V_{SS}	104	A10	112	V_{CC}

N.C.: Internally connected. Do not use.

(Only for piggyback/evaluation product)

■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Function
17	X1	A	Clock oscillator pins
18	X0		
16	MODA	B	Operation mode selection input pin Connect this pin to V_{SS} (GND).
20	$\overline{HST}$	B	Hardware standby input pin
21	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with a pull-up resistor, and a hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
11, 12	P90/RTO0, P91/RTO1	D	General-purpose I/O ports A pull-up resistor option is provided. Also serve as an output compare data output.
13	P92/BUZ/CLK	D	General-purpose I/O port Also serves as a buzzer/clock output.
14	P93/PWM0	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit PWM output.
19	P94/PWM1	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as an 8-bit PWM output.
22	P95/SCK	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the clock I/O (SCK) for the serial I/O. The SCK input is a hysteresis input. The output type can be switched between N-ch open-drain and CMOS.
23	P96/SO	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data output (SO) for the serial I/O. The output type can be switched between N-ch open-drain and CMOS.
24	P97/SI	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as the data input (SI) for the serial I/O.
25	P32/UCK	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a UART clock I/O (UCK). The UCK input is hysteresis input. The output type can be switched between N-ch open-drain and CMOS.
26	P31/UO	D	General-purpose I/O port A pull-up resistor option is provided. Also serves as a UART data output (UO). The output type can be switched between N-ch open-drain and CMOS.

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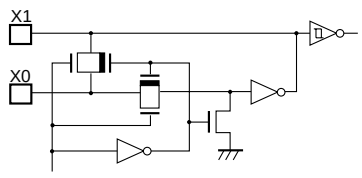
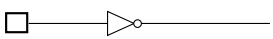
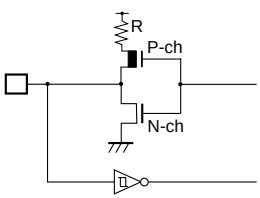
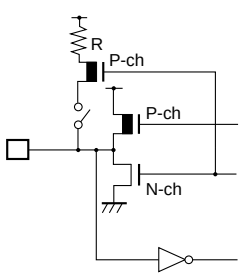
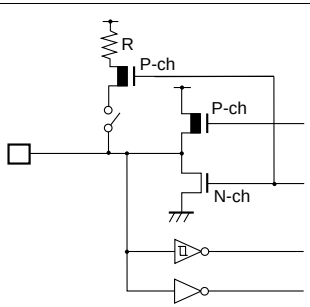
Pin no.	Pin name	Circuit type	Function
27	P30/UI	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as a UART data input (UI).
28 to 31	P27 to P24	D	General-purpose I/O ports A pull-up resistor option is provided.
32	P23/RTI1	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an input capture data input.
33, 34	P22, P21	D	General-purpose I/O ports A pull-up resistor option is provided.
35	P20/RTI0	E	General-purpose I/O port A pull-up resistor option is provided. Also serves as an input capture data input.
36 to 39	P07 to P04	D	General-purpose I/O ports A pull-up resistor options is provided.
40 to 43	P03/INT3 to P00/INT0	E	General-purpose I/O ports A pull-up resistor options is provided. Also serve as an external interrupt input (INT0 to INT3).
44 to 51	P17/AN7 to P10/AN0	G	CMOS I/O ports Also serve as an A/D converter analog input.
57, 58	P45/V2, P44/V1	F	LCD driving power supply pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD driving power supply.
59 to 62	P43/COM3 to P40/COM0	F	LCD common output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD common output.
63 to 70	P50/SEG0 to P57/SEG7	F	LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output.
71 to 78	P60/SEG8 to P67/SEG15	F	LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output.
79, 80	P70/SEG16, P71/SEG17	F	LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output.
1 to 6	P72/SEG18 to P77/SEG23	F	LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output.
7 to 11	P80/SEG24 to P83/SEG27	F	LCD segment output pins These pins can be used as an N-ch open-drain general-purpose I/O when not used as an LCD segment output.
52	AV_{SS}	—	A/D converter power supply (GND) pin
53	AVR	—	A/D converter reference power supply pin
54	AV_{CC}	—	A/D converter power supply pin
55	V_{CC}	—	Power supply pin
56	V3	—	LCD driving power supply pin
15	V_{SS}	—	Power supply (GND) pin

- **External EPROM pins (the MB89PV920 only)**

Pin no.	Pin name	I/O	Function
82 83 84 85 86 87 88 89 90 91	A15 A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
93 94 95	O1 O2 O3	I	Data input pins
96	V_{SS}	O	Power supply (GND) pin
98 99 100 101 102	O4 O5 O6 O7 O8	I	Data input pins
103	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
104	A10	O	Address output pin
105	$\overline{OE}/V_{PP}$	O	ROM output enable pin Outputs “L” at all times.
107 108 109	A11 A9 A8	O	Address output pins
110	A13	O	Address output pin
111	A14	O	Address output pin
112	V_{CC}	O	EPROM power supply pin
81 92 97 106	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• At an oscillation feedback resistor of approximately 1 MΩ (1 to 8 MHz)
B		
C		• At an output pull-up resistor of approximately 50 KΩ (5.0 V) • Hysteresis input
D		• CMOS output • CMOS input • Pull-up resistor optional
E		• CMOS output • CMOS input • Hysteresis input (peripheral input) • Pull-up resistor optional

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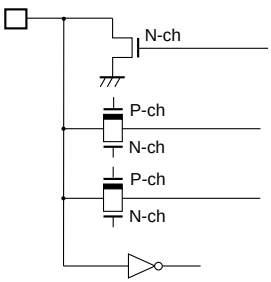
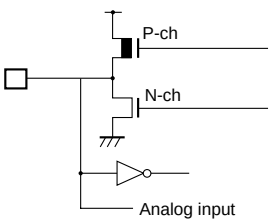
Type	Circuit	Remarks
F		• N-ch open-drain I/O • Also serves as LCD controller/driver common/ segment output.
G		• CMOS I/O • Analog input

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P928

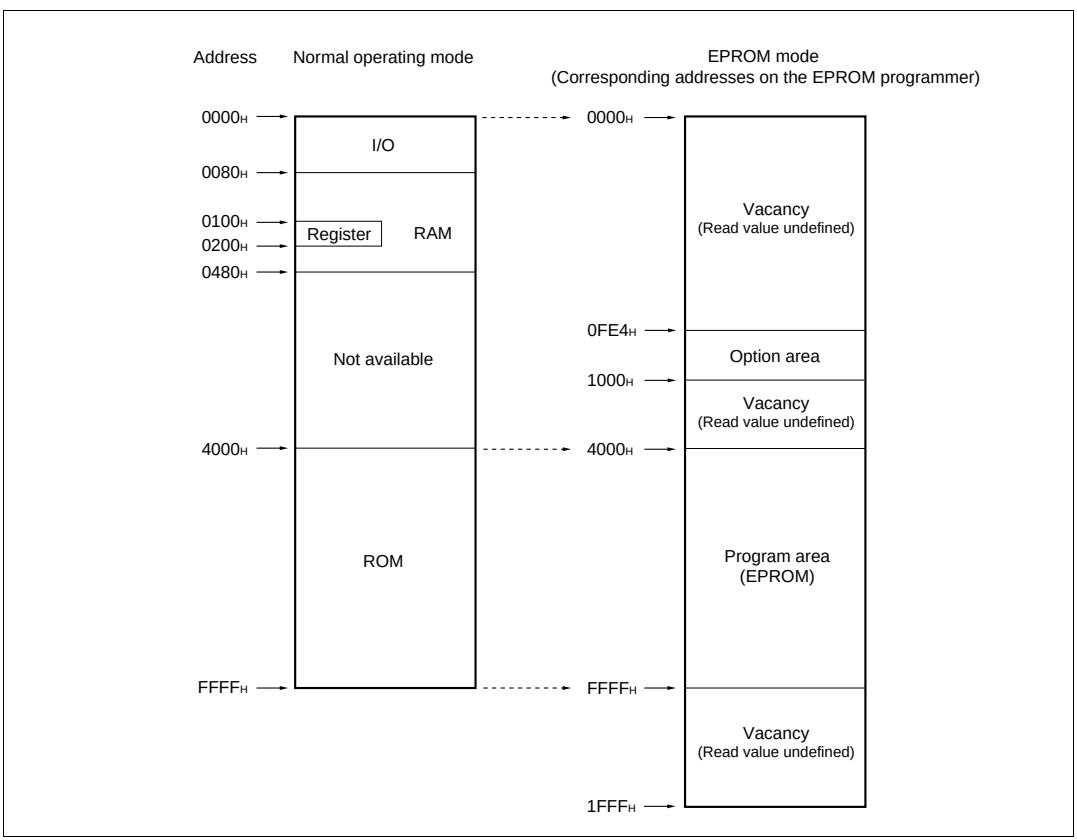
The MB89P928 is an OTPROM version of the MB89920 series.

1. Features

- 48-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C1001A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in the EPROM mode is diagrammed below.



3.Programming to the EPROM

In EPROM mode, the MB89P928 functions equivalent to the MBM27C1001A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

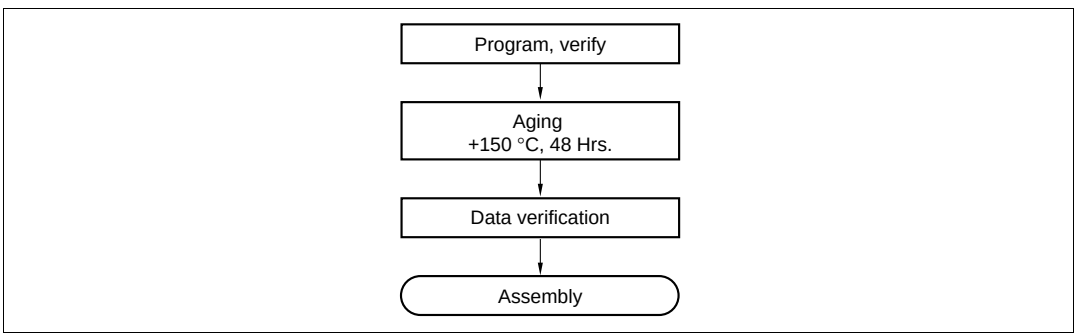
(1) Set the EPROM programmer to the MBM27C1001A.

(2) Load program data into the EPROM programmer at $0FE4_H$ to $FFFF_H$.

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-80P-M06	ROM-80QF-32DP-8LA

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: Depending on the EPROM programmer, inserting a capacitor of about 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

7. PROM Option Bit Map

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0FE4H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Oscillation stabilization time 1: Crystal 0: Ceramic	Reset pin output 1: Yes 0: No	Power-on reset 1: Yes 0: No	Vacancy Readable	Vacancy Readable
0FE8H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
0FECH	P27 Pull-up 1: No 0: Yes	P26 Pull-up 1: No 0: Yes	P25 Pull-up 1: No 0: Yes	P24 Pull-up 1: No 0: Yes	P23 Pull-up 1: No 0: Yes	P22 Pull-up 1: No 0: Yes	P21 Pull-up 1: No 0: Yes	P20 Pull-up 1: No 0: Yes
0FF0H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	P32 Pull-up 1: No 0: Yes	P31 Pull-up 1: No 0: Yes	P30 Pull-up 1: No 0: Yes
0FF4H	P97 Pull-up 1: No 0: Yes	P96 Pull-up 1: No 0: Yes	P95 Pull-up 1: No 0: Yes	P94 Pull-up 1: No 0: Yes	P93 Pull-up 1: No 0: Yes	P92 Pull-up 1: No 0: Yes	P91 Pull-up 1: No 0: Yes	P90 Pull-up 1: No 0: Yes
0FF8H	Vacancy Readable	Vacancy Readable	WDT/low-voltage control 1: Register 0: Option EPROM	Low-voltage detection voltage 00: — 10: 3.6 V	01: 3.3 V 11: 4.0 V	Low-voltage reset 1: Yes 0: No	Low-voltage detection 1: Automatic 0: Prohibited	Watchdog timer (WDT) 1: Automatic 0: Prohibited
0FFCH	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable

Notes:
- Set each bit to 1 to erase.
- Do not write 0 to the vacant bit.
  The read value of the vacant bit is 1, unless 0 is written to it.
- Write the same value as each option register to the 3-byte vacant address that follows above option registers.

  Example: In the case of 0FE4H, write the same value to 0FE5H, 0FE6H and 0FF7H.
- This optional information is taken into the OTPROM while the oscillation is being reset. Therefore, if the hardware state is initially shifted to standby state after the power supply is turned on, the optional information will not be valid during the transition (in a state of the initial value 1).

  After the hardware standby state is cleared, the oscillation starts and the optional information becomes valid.

  Note that if the hardware is shifted to the standby or stop state in the course of a normal operation (oscillation), the contents of the optional register are valid since the option data has already been taken into the OTPROM.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C512-20TV

2. Programming Socket Adapter

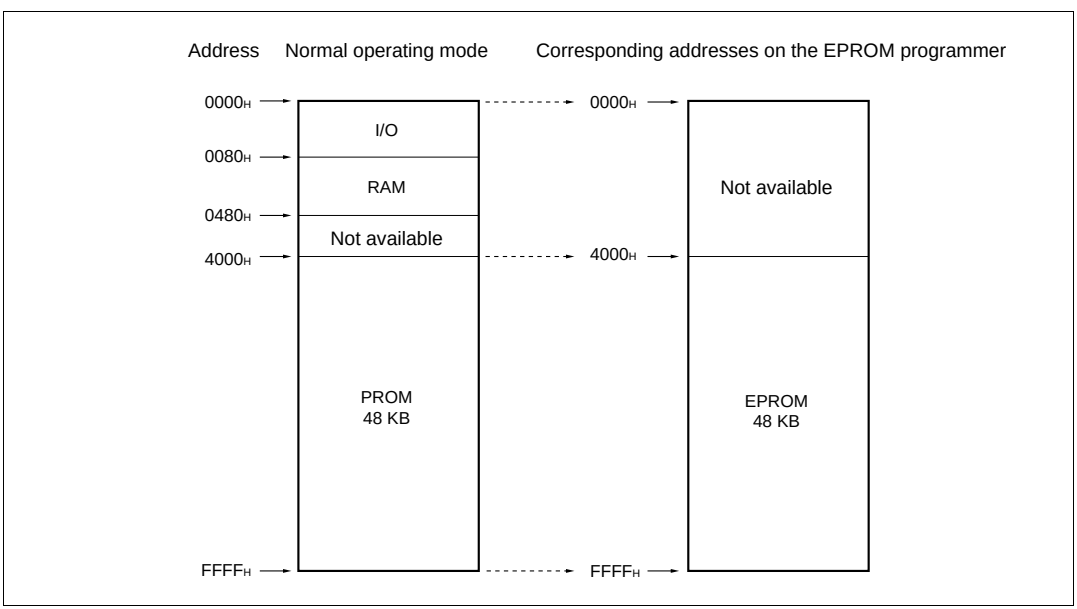
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode is diagrammed below.



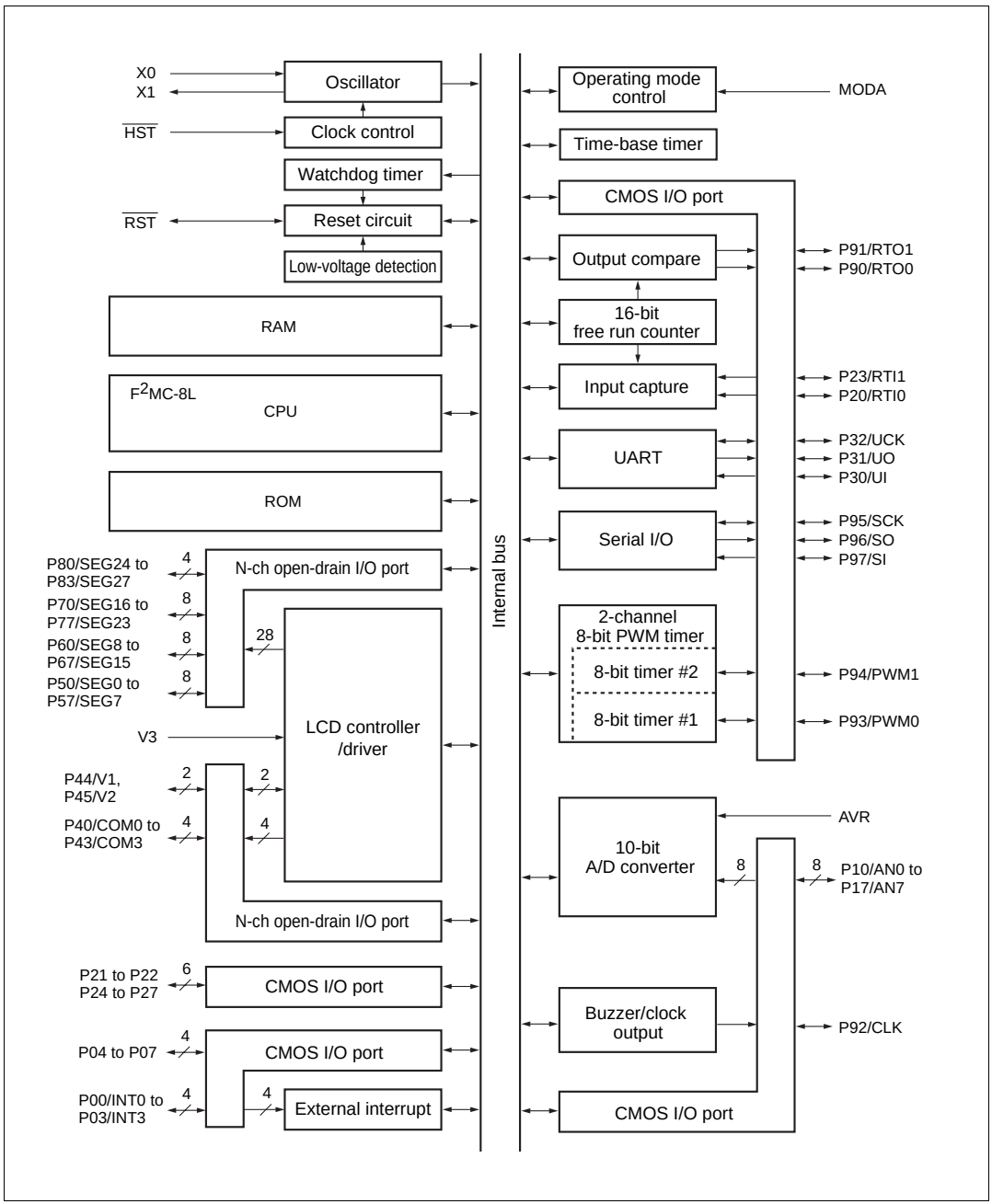
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C512.

(2) Load program data into the EPROM programmer at 4000_H to $FFFF_H$.

(3) Program to 4000_H to $FFFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM

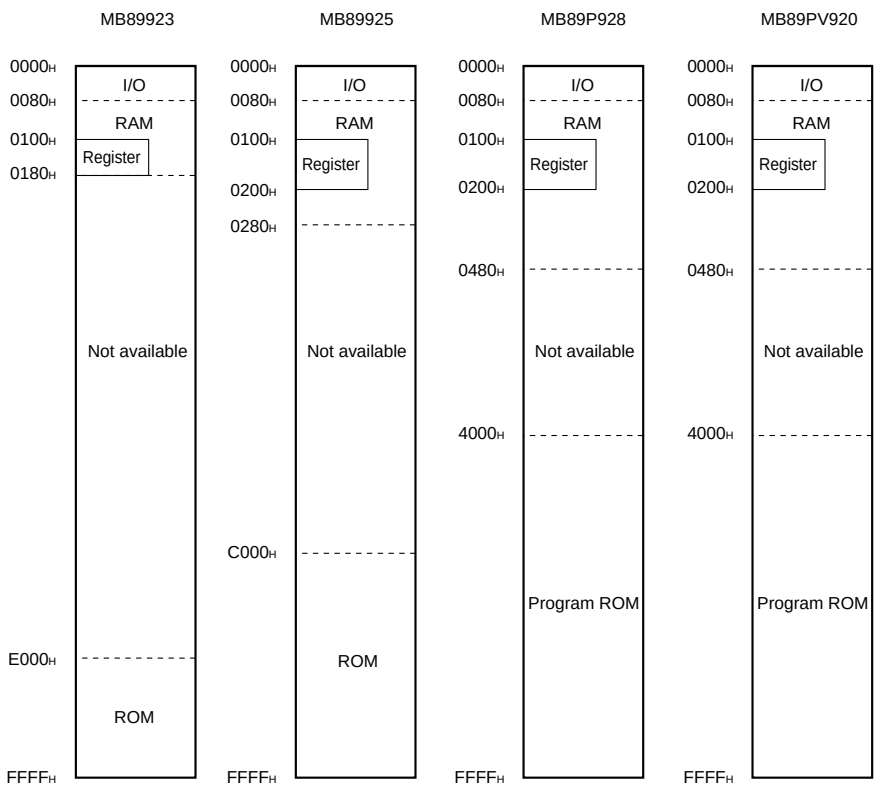


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89920 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89920 series is structured as illustrated below.

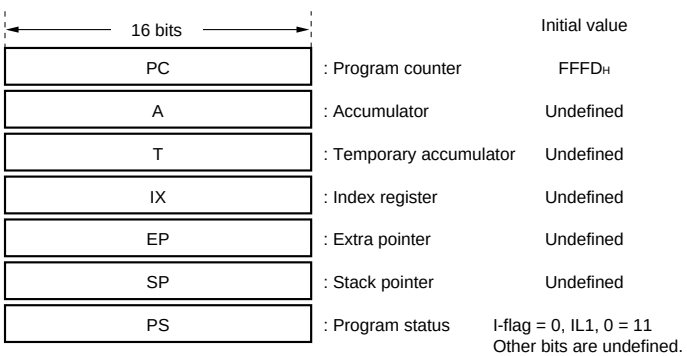
Memory Space



2. Registers

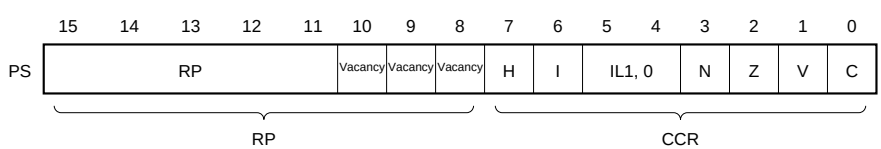
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



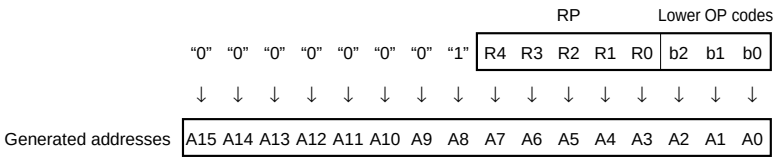
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

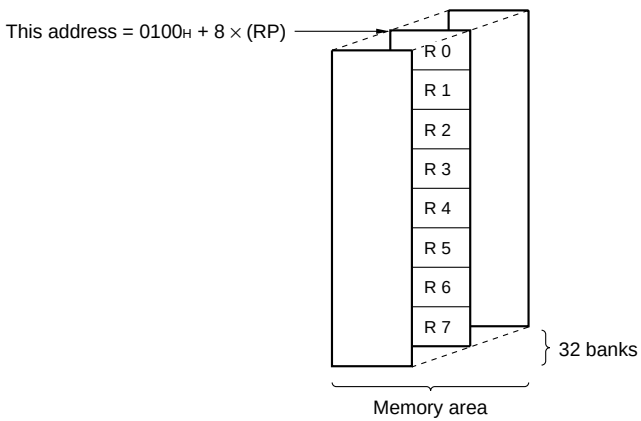
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 16 banks can be used on the MB89925. Up to a total of 16 banks can be used on the MB89923. The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register	Register description	Intial value
00H	(R/W)	PDR0	Port 0 data register	X X X X X X X X B
01H	(W)	DDR0	Port 0 data direction register	0 0 0 0 0 0 0 0 B
02H	(R/W)	PDR1	Port 1 data register	X X X X X X X X B
03H	(W)	DDR1	Port 1 data direction register	0 0 0 0 0 0 0 0 B
04H			Vacancy	
05H			Vacancy	
06H			Vacancy	
07H			Vacancy	
08H	(R/W)	STBC	Standby control register	0 0 0 1 X X X X B
09H	(R/W)	WDTE	Watchdog timer control register	X X X X X X X X B
0AH	(R/W)	TBCR	Time-base timer control register	X X X 0 0 0 0 0 B
0BH	(R/W)	LVRC	Low-voltage detection reset control register	0 X 1 1 X 0 0 X B
0CH	(R/W)	PDR3	Port 3 data/peripheral I/O control register	0 0 0 0 – X X X B
0DH	(W)	DDR3	Port 3 data direction register	– – – – – 0 0 0 B
0EH	(R/W)	PDR4	Port 4 data register	– – 1 1 1 1 1 1 B
0FH	(R/W)	PDR5	Port 5 data register	1 1 1 1 1 1 1 1 B
10H	(R/W)	PDR6	Port 6 data register	1 1 1 1 1 1 1 1 B
11H	(R/W)	PDR7	Port 7 data register	1 1 1 1 1 1 1 1 B
12H	(R/W)	PDR8	Port 8 data register	– – – – 1 1 1 1 B
13H	(R/W)	PDR9	Port 9 data register	X X X X X X X X B
14H	(W)	DDR9	Port 9 data direction register	0 0 0 0 0 0 0 0 B
15H	(R/W)	PDR2	Port 2 data register	X X X X X X X X B
16H	(R/W)	DDR2	Port 2 data direction register	0 0 0 0 0 0 0 0 B
17H	(R/W)	BUZR	Buzzer control register	X X X X 0 0 0 0 B
18H	(R/W)	ADC1	AD converter control register 1	0 0 0 0 0 0 0 0 B
19H	(R/W)	ADC2	AD converter control register 2	X 0 0 0 0 0 0 1 B
1AH	(R/W)	ADCH	AD converter data register “H”	– – – – – – X X B
1BH	(R/W)	ADCL	AD converter data register “L”	X X X X X X X X B
1CH	(R/W)	SMR	Serial mode register	0 0 0 0 0 0 0 0 B
1DH	(R/W)	SDR	Serial data register	X X X X X X X X B
1EH			Vacancy	
1FH	(W)	ICR1	Port 1 input control register	0 0 0 0 0 0 0 0 B

–: Unused X: Undefined *(Continued)*

Note: Do not use vacancies

Address	Read/write	Register	Register description	Initial value
20H	(R/W)	CNTR1	PWM timer control register 1	0 0 0 0 0 0 0 0 B
21H	(R/W)	CNTR2	PWM timer control register 2	0 0 0 0 0 0 0 0 B
22H	(R/W)	CNTR3	PWM timer control register 3	0 0 0 X 0 0 0 0 B
23H	(W)	COMR2	PWM timer compare register 2	X X X X X X X X B
24H	(W)	COMR1	PWM timer compare register 1	X X X X X X X X B
25H			Vacancy	
26H			Vacancy	
27H			Vacancy	
28H	(R/W)	TMCR	Timer control register	0 0 X X 0 0 0 0 B
29H	(R)	TCHR	Timer count register (H)	0 0 0 0 0 0 0 0 B
2AH	(R)	TCLR	Timer count register (L)	0 0 0 0 0 0 0 0 B
2BH	(R/W)	OPCR	Output control register	0 0 0 0 0 0 0 0 B
2CH	(R/W)	CPR0H	Output compare register 0 (H)	0 0 0 0 0 0 0 0 B
2DH	(R/W)	CPR0L	Output compare register 0 (L)	0 0 0 0 0 0 0 0 B
2EH	(R/W)	CPR1H	Output compare register 1 (H)	0 0 0 0 0 0 0 0 B
2FH	(R/W)	CPR1L	Output compare register 1 (L)	0 0 0 0 0 0 0 0 B
30H	(R/W)	ICCR	Input capture control register	X 0 0 0 X 0 0 0 B
31H	(R/W)	ICIC	Input capture interrupt control register	X 0 0 0 0 X 0 0 B
32H	(R)	ICR0H	Input capture register 0 (H)	X X X X X X X X B
33H	(R)	ICR0L	Input capture register 0 (L)	X X X X X X X X B
34H	(R)	ICR1H	Input capture register 1 (H)	X X X X X X X X B
35H	(R)	ICR1L	Input capture register 1 (L)	X X X X X X X X B
36H			Vacancy	
37H			Vacancy	
38H	(R/W)	EIC1	External interrupt control register 1	0 0 0 0 0 0 0 0 B
39H	(R/W)	EIC2	External interrupt control register 2	0 0 0 0 0 0 0 0 B
3AH			Vacancy	
3BH			Vacancy	
3CH			Vacancy	
3DH			Vacancy	
3EH			Vacancy	
3FH			Vacancy	

–: Unused X: Undefined *(Continued)*

Note: Do not use vacancies

(Continued)

Address	Read/write	Register	Register description	Initial value
40H	(R/W)	USMR	UART mode register	0 0 0 0 0 0 0 0 B
41H	(R/W)	USCR	UART control register	0 0 0 0 0 0 0 0 B
42H	(R/W)	USTR	UART status register	0 0 0 0 1 X X X B
43H	(R) (W)	RXDR TXDR	UART receiver data register UART transmitter data register	X X X X X X X X B X X X X X X X X B
44H			Vacancy	
45H	(R/W)	RRDR	Baud rate generator/reload data register	X X X X X X X X B
46H			Vacancy	
47H			Vacancy	
48 to 5FH			Vacancy	
60 to 6DH	(R/W)	VRAM	Display data RAM	X X X X X X X X B
70H	(R/W)	LCR1	LCD controller/driver control register 1	0 0 0 0 0 0 0 0 B
71H	(R/W)	LCR2	LCD controller/driver control register 2	0 0 0 – – – – – B
72H	(R/W)	LCR3	LCD controller/driver control register 3	0 0 0 0 0 0 0 0 B
73 to 7BH			Vacancy	
7CH	(W)	ILR1	Interrupt level setting register 1	1 1 1 1 1 1 1 1 B
7DH	(W)	ILR2	Interrupt level setting register 2	1 1 1 1 1 1 1 1 B
7EH	(W)	ILR3	Interrupt level setting register 3	1 1 1 1 1 1 1 1 B
7FH			Vacancy	

–: Unused X: Undefined

Note: Do not use vacancies

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{CC} + 0.3	V	*1
	AVR	V_{SS} – 0.3	V_{SS} + 7.0	V	AVR must not exceed AV_{CC} + 0.3 V.
LCD power supply voltage	V1 to V3	V_{SS} – 0.3	V_{SS} + 7.0	V	V1 ≤ V2 ≤ V3 *2
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P90 to P97
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83 Must not exceed “V3 + 0.3 V”
“L” level maximum output current	I_{OL}	—	20	mA	Peak value
“L” level average output current	I_{OLAV}	—	4	mA	Average value
“L” level total maximum output current	$\sum I_{OL}$	—	100	mA	Peak value
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value
“H” level maximum output current	I_{OH}	—	–20	mA	Peak value
“H” level average output current	I_{OHAV}	—	–4	mA	Average value
“H” level total maximum output current	$\sum I_{OH}$	—	–50	mA	Peak value
“H” level total average output current	$\sum I_{OHAV}$	—	–20	mA	Average value
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: Use AV_{CC} and V_{CC} set at the same voltage.
Take care so that AV_{CC} does not exceed V_{CC}, such as when power is turned on.

*2: V_{CC} must not exceed V3.

Precautions: Permanent device damage may occur if the above “Absolute Maximum Ratings” are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*1	6.0	V	Normal operation assurance range
		2.7*1	6.0	V	MB89PV920/P928
		1.5	6.0	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	3.0	AV_{CC}	V	
LCD power supply voltage	V1 to V3	V_{SS}	V_{SS} + 6.0	V	V1 ≤ V2 ≤ V3*2
Operating temperature	T_A	–40	+85	°C	

*1: These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and "5. A/D Converter Electrical Characteristics."

*2: V_{CC} must not exceed V3.

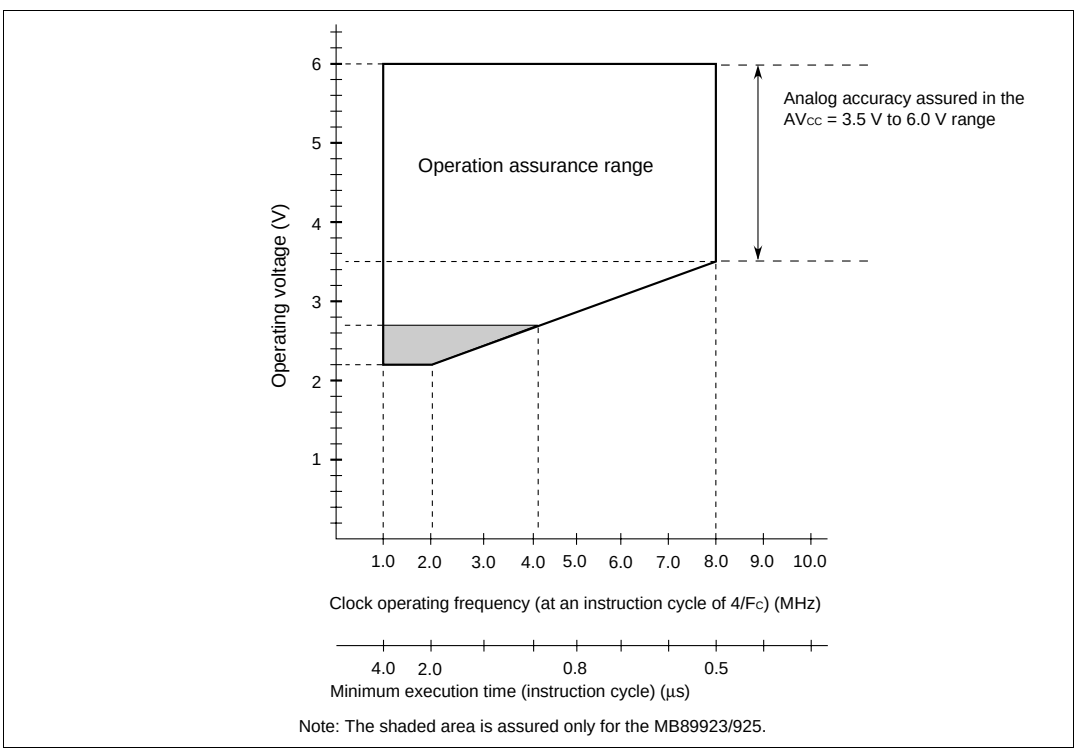


Figure 1 Operating Voltage vs. Clock Operating Frequency

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of 4/F_C.
Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

3. DC Characteristics

(V_{CC} = 5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	
	V_{IHS}	$\overline{RST}$, MODA, $\overline{HST}$	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	Peripheral input of the port 0, 2, 3, and 9
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	
	V_{ILS}	$\overline{RST}$, MODA, $\overline{HST}$	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	Peripheral input of the port 0, 2, 3, and 9
Open-drain output pin application voltage	V_D	P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83*1	—	V_{SS} – 0.3	—	V_{SS} + 6.0	V	
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17, P30 to P32, P90 to P97	I_{OH} = –2.0 mA	4.0	—	—	V	
	V_{OH2}	P20 to P27	I_{OH} = –5.0 mA	2.4	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P10 to P17, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97	I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P20 to P27	I_{OL} = 5.0 mA	—	—	0.4	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = 4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakage current)	I_{LI1}	P00 to P07, P10 to P17, P20 to P27, P30 to P32, P40 to P45, P50 to P57, P60 to P67, P70 to P77, P80 to P83, P90 to P97, MODA	0.45 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
Pull-up resistance	R_{PULU}	P00 to P07, P20 to P27, P30 to P32, P90 to P97	V_I = 0.0 V	25	50	100	kΩ	Without pull-up resistor

(Continued)

(V_{CC} = 5.0 V, V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*2	I_{CC}	V_{CC}	V_{CC} = 5.0 V	—	12	20	mA	t_{inst} = 0.5 µs
	I_{CCS}		V_{CC} = 5.0 V	—	3	7	mA	Sleep mode t_{inst} = 0.5 µs
	I_{CCH}		T_A = +25°C	—	—	1	µA	Stop mode
	I_A	AV_{CC}	when A/D conversion is activated	—	6	8	mA	
	I_{AH}		when A/D conversion is stopped T_A = +25°C	—	—	1	µA	
LCD divided resistance	R_{LCD}	Between V3 and V_{SS}		200	300	450	kΩ	
COM0 to 3 output impedance	R_{VCOM}	COM0 to 3	V1 to V 3 = 5.0 V	—	—	2.5	kΩ	
SEG0 to 27 output impedance	R_{VSEG}	SEG0 to 27	V1 to V 3 = 5.0 V	—	—	15	kΩ	
LCD controller/ driver leakage current	I_{LCDL}	V1 to V3, COM0 to 3, SEG0 to 27	V1 to V 3 = 5.0 V	—	—	±1	µA	
Input capacitance	C_{IN}	Other than AV_{CC}, AV_{SS}, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: V_D must not exceed V3.

*2: The measurement conditions of power supply current are as follows: the external clock and T_A = +25°C.
In the case of the MB89PV920, the current consumed by the connected EPROM and ICE is not included.

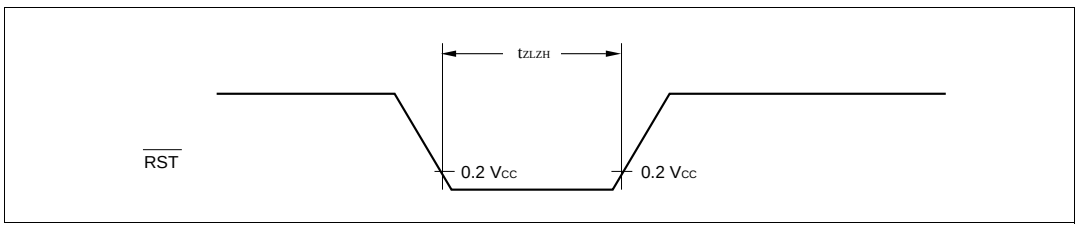
Note: For pins which serve as the LCD and ports (P40 to P45, P50 to P57, P60 to P67, P70 to P77, and P80 to P83), see the port parameter when these pins are used as ports and the LCD parameter when they are used as LCD pins.

4. AC Characteristics

(1) Reset Timing

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

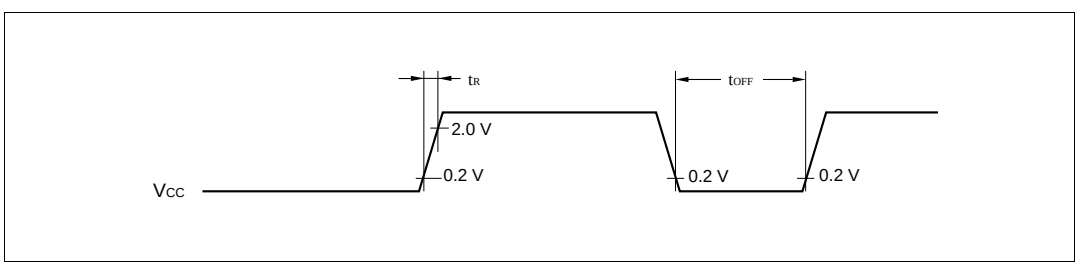


(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

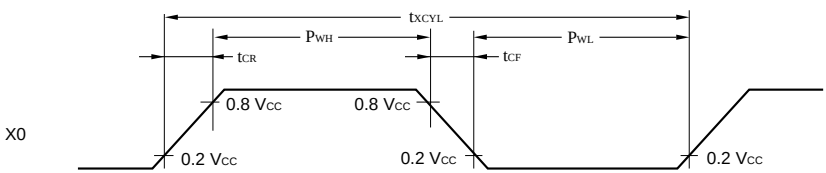


(3) Clock Timing

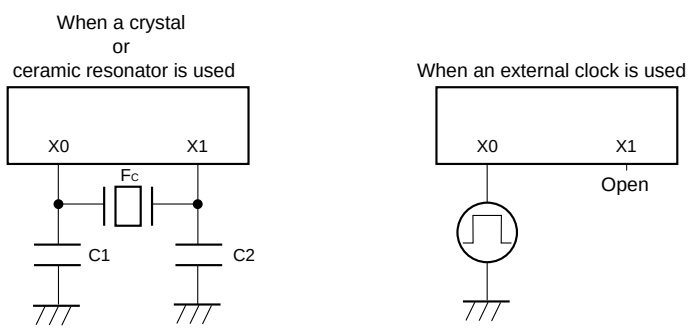
($AV_{SS} = V_{SS} = 0.0$ V, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Clock frequency	F_C	X0, X1	—	1	8	MHz	
Clock cycle time	t_{XCYL}	X0, X1		125	1000	ns	
Input clock pulse width	P_{WH} P_{WL}	X0		20	—	ns	External clock
Input clock rising/falling time	t_{CR} t_{CF}	X0		—	10	ns	External clock

X0 and X1 Timing and Conditions



Clock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_C$	µs	$(4/F_C)$ t_{inst} = 0.5 µs when operating at F_C = 8 MHz

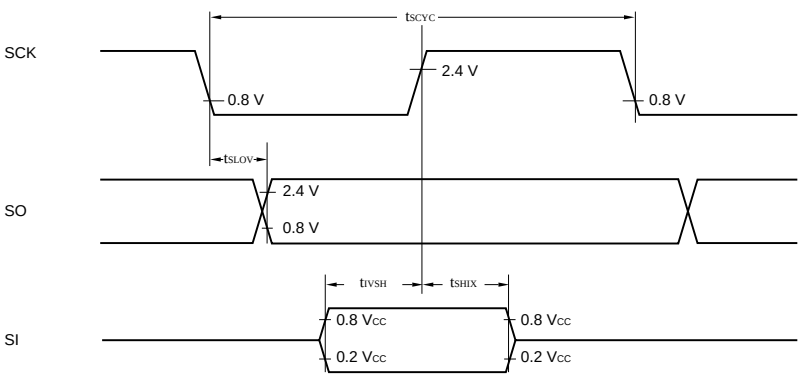
(5) Serial I/O Timing

(AV_{CC} = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

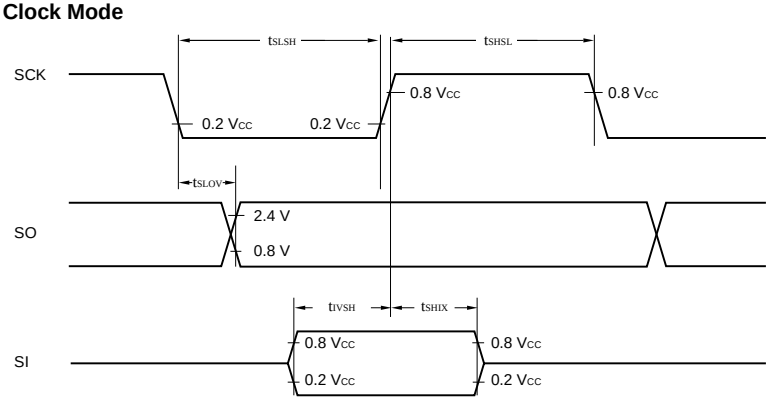
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

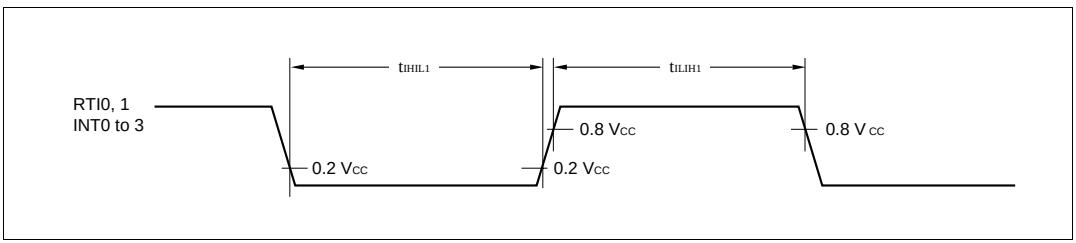


(6) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT0 to INT3, RTI0, 1	2 t_{inst}*	—	—	
Peripheral input “L” pulse width 1	t_{IHIL1}	INT0 to INT3, RTI0, 1	2 t_{inst}*	—	—	

* : For information on t_{inst}, see “(4) Instruction Cycle.”



5. A/D Converter Electrical Characteristics

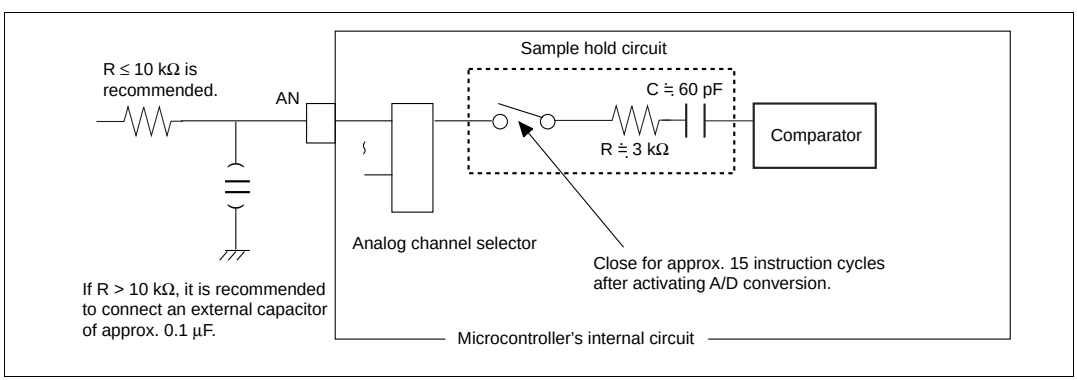
($AV_{CC} = V_{CC}$ = +3.5 V to +6.0 V, F_C = 8 MHz, $AV_{SS} = V_{SS}$ = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit
				Min.	Typ.	Max.	
Resolution	—	—	AV_{CC} = AVR = V_{CC}	—	—	10	bit
Linearity error				—	—	±2.0	LSB
Differential linearity error				—	—	±1.5	LSB
Differential total error				—	—	±3.0	LSB
Zero transition voltage	V_{OT}	AN0 to AN7		AV_{SS} – 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	mV
Full-scale transition voltage	V_{FST}	AN0 to AN7		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR + 0.5 LSB	mV
Interchannel disparity	—	—		—	—	4	LSB
A/D mode conversion time				—	—	16.5	µs
Analog port input current	V_{AIN}	AN0 to AN7	At 8-MHz oscillattion	—	—	10	µA
Analog input voltage	—	AN0 to AN7		0.0	—	AVR	V
Reference voltage		AVR		0.0	—	AV_{CC}	V
Reference voltage supply current	I_R	AVR	AVR = 5.0 V	—	200	—	µA

Precautions: • The smaller | AVR – AV_{SS} |, the greater the error would become relatively.

• The output impedance of the external circuit for the analog input must satisfy the following conditions:
Output impedance of the external circuit < Approx. 10 kΩ
If the output impedance of the external circuit is too high, an analog voltage sampling time might be insufficient (sampling time = 7.5 µs at 8 MHz oscillation).

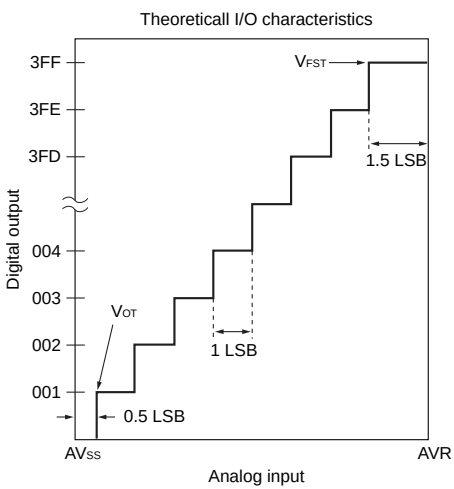
An analog input equivalent circuit is shown below.

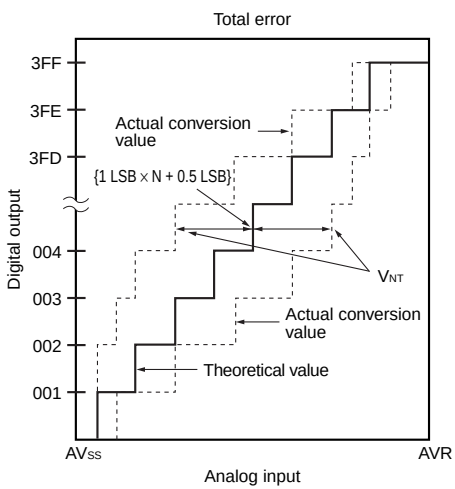


Since the A/D converter contains sample hold circuit, the level of the analog input pin might not stabilize within the sampling period after A/D activation, resulting in inaccurate A/D conversion values, if the input impedance to the analog pin is too high. Be sure to maintain an appropriate input impedance to the analog pin.
It is recommended to keep the input impedance to the analog pin not exceed 10 kΩ. If it exceeds 10 kΩ, it is recommended to connect a capacitor of about 0.1 µF for the analog input pin.
Except for the sampling period after A/D activation, the input leakage current of the analog input pin is less than 10 µA.

(1) A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter.
- Linearity error
  The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1111” ↔ “11 1111 1110”) from actual conversion characteristics
- Differential linearity error
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error
  The difference between theoretical and actual conversion values, caused by the zero transition error, full-scale transition error, linearity error, quantization error, and noise.





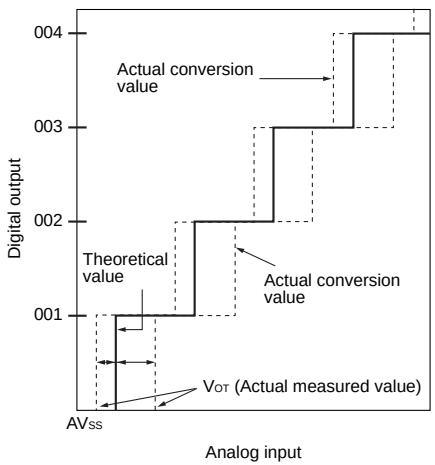
$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ (\text{V})$$

$$\text{Total error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times N + 0.5\ \text{LSB}\}}{1\ \text{LSB}}$$

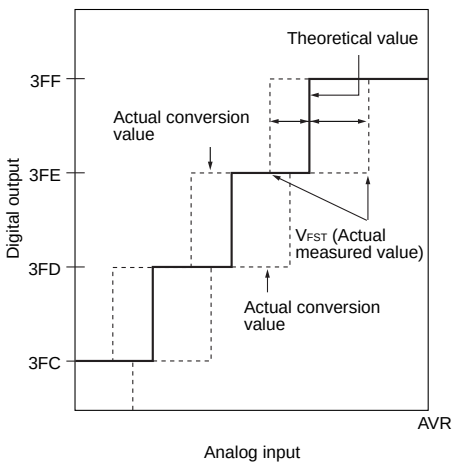
(Continued)

(Continued)

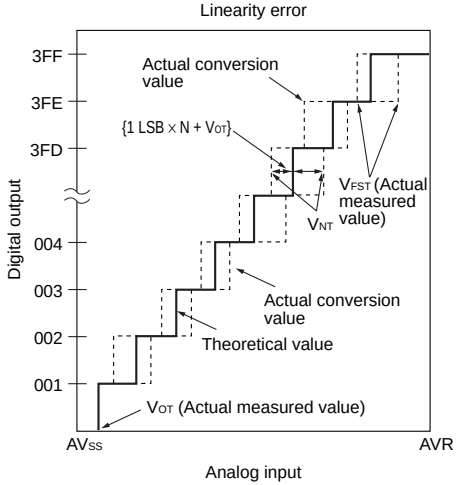
Zero transition error



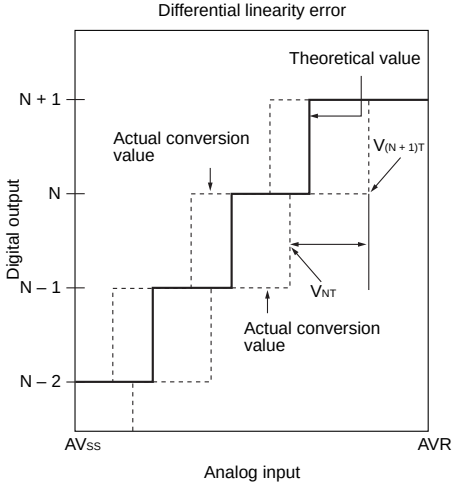
Full-scale transition error



Linearity error



Differential linearity error



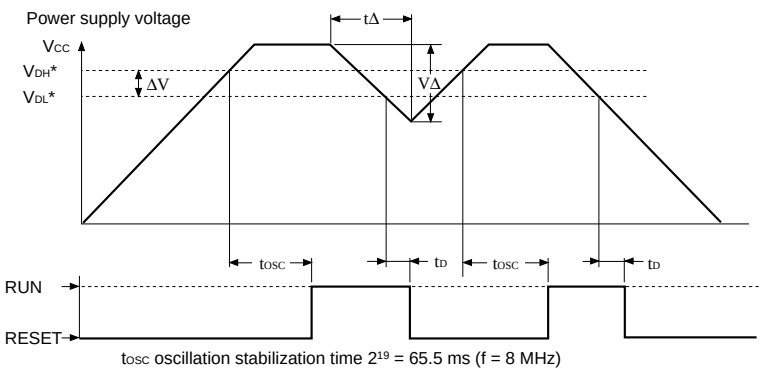
Linearity error of digital output N = $\frac{V_{NT} - \{1\ LSB \times N + V_{OT}\}}{1\ LSB}$ Differential linearity error of digital output N = $\frac{V_{(N+1)T} - V_{NT}}{1\ LSB} - 1$

6. Low-voltage Detection Reset

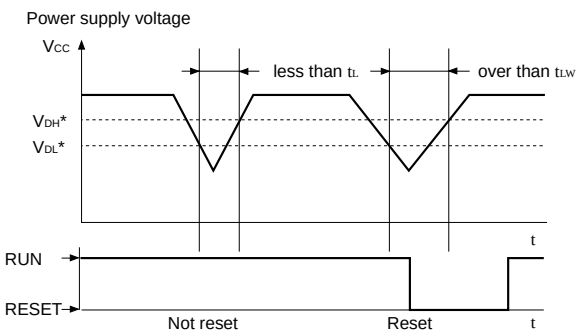
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Voltage detected at power supply voltage drop	V_{DL1}		3.00	3.60	V	*1
	V_{DL2}		3.30	3.90	V	
	V_{DL3}		3.70	4.30	V	
Voltage detected at power supply voltage rise	V_{DH1}		3.10	3.80	V	
	V_{DH2}		3.40	4.10	V	
	V_{DH3}		3.80	4.50	V	
Hysteresis width	ΔV		0.10	—	V	
Reset ignore time	t_L		0.3	—	µs	
Reset sense time	t_{LW}		16 t_{XCYL}	—	ns	
Reset detection deley time	t_D		—	2.0	µs	
Voltage regulation (VΔ/tΔ)	VCR		—	0.10	V/µs	

*1: VDH and VDL can be set for the MB89923 and MB89925 by mask options; for the MB89PV920 and MB89P928 by registers.



t_{OSC} oscillation stabilization time 2^{19} = 65.5 ms (f = 8 MHz)



■ INSTRUCTIONS (136 INSTRUCTIONS)

Execution instructions can be divided into the following four groups:
- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: The number of instructions

#: The number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:
- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH prior to the instruction executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:
Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Note During byte transfer to A, T ← A is restricted to low bytes.
Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

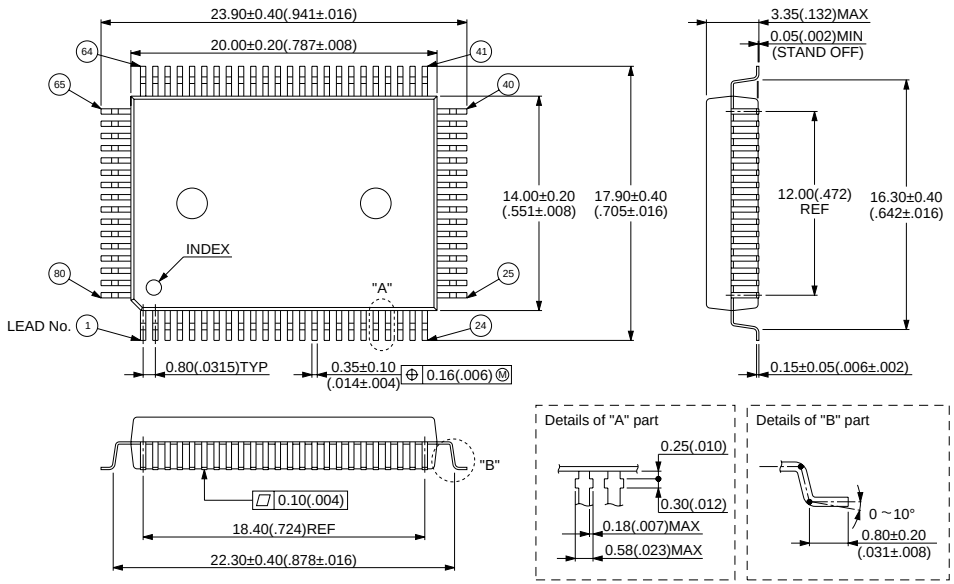
No.	Part number	MB89923 MB89925	MB89P928	MB89PV920
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P20 to P27, P30 to P32, P90 to P97	P00 to P07, P20 to P27, P30 to P32, P90 to P97 : Selectable by pin	Can be set per pin	No pull-up resistor
2	Power-on reset Power-on reset provided No power-on reset	Selectable	Can be set	With power-on reset
3	Oscillation stabilization time slection (at 8 Hz) Cystal oscillator (32.8 ms/8MHz) Ceramic oscillator (2.05 ms/8 MHz)	Selectable	Can be set	Crystal oscillator (32.8 ms/8 MHz)
4	Reset pin output Reset output provided No reset output	Selectable	Can be set	With reset output
5	Watchdog timer Activation prohibited Automatic activation	Selectable	Can be set	Inactive by default (Can be activated by software)
6	Low-voltage detection reset circuit Activation prohibited Automatic activation	Selectable	Can be set	Inactive by default (Can be activated by software)
7	Low-voltage detection reset output Output disabled Output enabled	Selectable	Can be set	Inactive by default (Can be activated by software)
8	Low-voltage detection voltage 3.3 V ± 0.3 V 3.6 V ± 0.3 V 4.0 V ± 0.3 V	Selectable	Can be set	Register setting
9	Low-voltage detection reset/watchdog timer function selection Register setting valid Option setting valid	Selectable	Can be set	Fixed to register setting

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89923PF MB89925PF MB89P928PF	80-pin Plastic QFP (FPT-80P-M06)	
MB89PV920CF	80-pin Ceramic MQFP (MQP-80C-P01)	

■ PACKAGE DIMENSIONS

80-pin Plastic QFP
(FPT-80P-M06)



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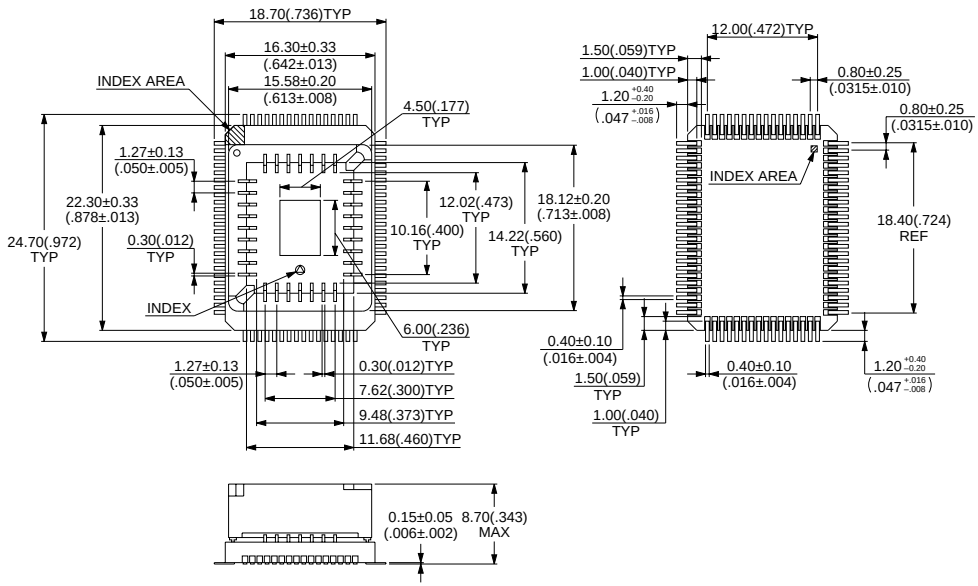
Dimensions in mm (inches)

80-pin Ceramic MQFP
(MQP-80C-P01)



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Dimensions in mm (inches)

FUJITSU LIMITED

For further information please contact:

Japan

FUJITSU LIMITED
Corporate Global Business Support Division
Electronic Devices
KAWASAKI PLANT, 4-1-1, Kamikodanaka,
Nakahara-ku, Kawasaki-shi,
Kanagawa 211-8588, Japan
Tel: +81-44-754-3763
Fax: +81-44-754-3329

http://www.fujitsu.co.jp/

North and South America

FUJITSU MICROELECTRONICS, INC.
3545 North First Street,
San Jose, CA 95134-1804, U.S.A.
Tel: +1-408-922-9000
Fax: +1-408-922-9179

Customer Response Center
Mon. - Fri.: 7 am - 5 pm (PST)
Tel: +1-800-866-8608
Fax: +1-408-922-9179

http://www.fujitsumicro.com/

Europe

FUJITSU MICROELECTRONICS EUROPE GmbH
Am Siebenstein 6-10,
D-63303 Dreieich-Buchschlag,
Germany
Tel: +49-6103-690-0
Fax: +49-6103-690-122

http://www.fujitsu-fme.com/

Asia Pacific

FUJITSU MICROELECTRONICS ASIA PTE. LTD.
#05-08, 151 Lorong Chuan,
New Tech Park,
Singapore 556741
Tel: +65-281-0770
Fax: +65-281-0220

http://www.fmap.com.sg/

Korea

FUJITSU MICROELECTRONICS KOREA LTD.
1702 KOSMO TOWER, 1002 Daechi-Dong,
Kangnam-Gu,Seoul 135-280
Korea
Tel: +82-2-3484-7100
Fax: +82-2-3484-7111

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