FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12521-3E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89910 Series

MB89913/915/P915/PV910

■ DESCRIPTION

The MB89910 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, timers, a serial interface, an A/D converter, a buzzer output, a low-voltage detection reset, high-voltage driver, a watch prescaler, and external interrupts.
The MB89910 series is applicable to a wide range of applications from consumer products to industrial equipments.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- Minimum execution time: 0.50 µs/8.0 MHz oscillation
- Interrupt processing time: 4.50 µs/8.0 MHz oscillation
- F²MC-8L family CPU core

  Instruction set optimized for controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operations
  - Test and branch instructions
  - Bit manipulation instructions, etc.

- Dual-clock control system

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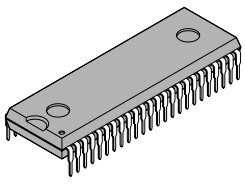
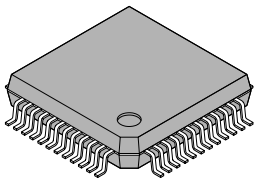
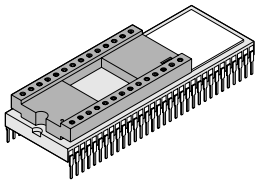
■ PACKAGE

48-pin Plastic SH-DIP	48-pin Plastic QFP	64-pin Ceramic MDIP
		
(DIP-48P-M01)	(FPT-48P-M15)	(MDP-64C-P02)

(Continued)

- High-voltage ports (built-in a pull-down resistor capable)
  8 ports for large current
  10 ports for small current
- 8-bit PWM timer: 1 channel
- 16-bit timer/counter: 1 channel
- 21-bit timebase timer
- 8-bit serial I/O: 1 channel
- 8-bit A/D converter: 8 channels
- External interrupt
  Edge detection function
  Two channels, including one of which voltage can be applied from –0.3 to +7.0 V
- Low-voltage detection reset (excluding the MB89PV910)
- Low-power consumption modes (subclock mode, watch mode, sleep mode, and stop mode)
- Reset output and power-on reset function
- Watch prescaler

■ PRODUCT LINEUP

Parameter \ Partnumber	MB89913	MB89915	MB89P915	MB89PV910
Classification	Mass production product (mask ROM product)		One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	8 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal mask ROM)	16 K × 8 bits (internal PROM, programmable with general-purpose EPROM programmer)	32K × 8 bits (Piggyback) (External ROM)
RAM size	256 × 8 bits	512 × 8 bits		1 K × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.50 µs/8.0 MHz to 8.00 µs/8.0 MHz, or 61 µs/32.768 kHz Interrupt processing time: 4.5 µs/8.0 MHz to 72.0 µs/8.0 MHz, or 549.3 µs/32.768 kHz Note: The above times depend on the gear function.			
Ports	High-voltage output ports (P-ch open-drain): 8 (P10 to P17 for large current) 10 (P20 to P27 and P50 to P51 for small current) I/O ports (CMOS): 13 (P00 to P07, P34 to P37, and P40) I/O ports (N-ch open-drain): 6 (P30 to P33, P41, P42) Input ports (CMOS): 2 (P60 and P61 also serve as a subclock pin) Total: 39			
Timebase timer (Timer 1)	Capable of generating four different intervals at 8.0-MHz oscillation: 0.26, 0.51, 1.02, and 524.0 ms			
8-bit PWM timer (Timer 2)	8-bit timer operation (square wave output capable. Operation clock: 1, 2, 8, or 16 instruction cycles) 8-bit resolution PWM operation (Conversion cycle: 128 µs to 2.0 ms at 8.0 MHz)			
16-bit timer/counter (Timer 3)	16-bit timer operation (operating clock: 1 instruction cycle) 16-bit event counter operation (Rising/falling/both edges selectable)			
8-bit serial I/O	8 bits LSB first/MSB first selectable Transfer clock (external, 4/8/16 instruction cycles)			
8-bit A/D converter	8-bit resolution × 8 channels A/D conversion mode (conversion time of 22.0 µs/8.0 MHz) Sense mode (conversion time of 6.0 µs/8.0 MHz) Continuous activation enabled by external clock or internal clock Reference voltage input (AVR) is provided.			

(Continued)

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Parameter \ Partnumber	MB89913	MB89915	MB89P915	MB89PPV910
External interrupt	2 independent channels (edge selection, interrupt vector, factor flag) Rising/ falling/both edges selectable Built-in analog noise canceller Used also for wake-up stop/sleep modes. (Edge detection is also permitted in stop mode.)			
Low-voltage detection reset	Continuous operation (detection power supply voltage of 4.0±0.3 V, 3.6±0.3 V or 3.3±0.3 V) Intermittent operation (Activated for each watch interrupt under the dual-clock system)			Not available
Low-power consumption (Standby mode)	Sleep mode, stop mode, and watch mode			
Process	CMOS			
Operating voltage*	3.8 V to 5.5 V 4.5 V to 5.5 V			
EPROM for use	—			MBM27C256A-20CZ

* : Varies with conditions such as the operating frequency. (See section "■ Electrical Characteristics.")
In the case of the MB89PV910, the voltage varies with the ICE or the EPROM to be connected.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89913 MB89915 MB89P915	MB89PV910
DIP-48P-M01	○	×
FPT-48P-M15	○*1	×
MDP-64C-P02	×	○*2

○ : Available × : Not available

*1: Under examination for development
*2: Available by conversion from MDIP-64 to SH-DIP-48
64SD-48SD-8L2: For conversion (MDP-64C-P02) → DIP-48P-M01
Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV910, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see sections "■ Electrical Characteristics" and "■ Example Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

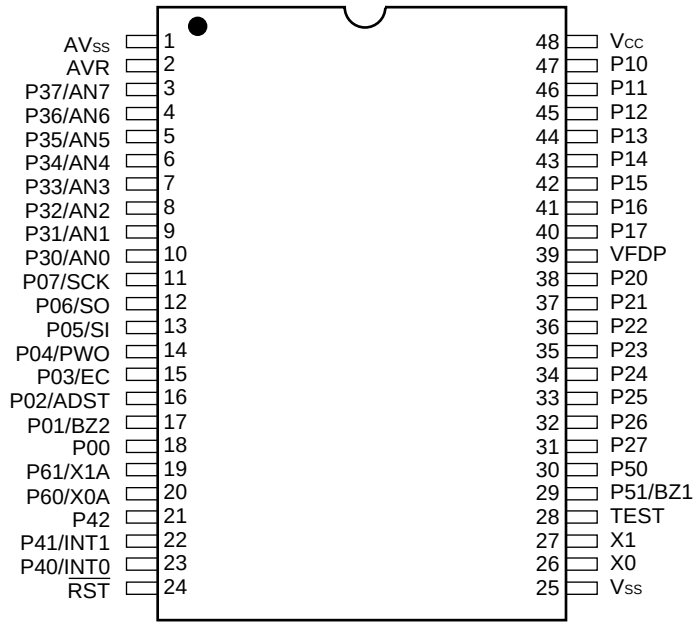
Before using options check section "■ Mask Options."

Take particular care on the following points:

- A pull-down resistor for P10 to P17, P20 to P27, and for P50 to P51 cannot be set for the MB89P915 and MB89PV910. The MB89915 and MB89913 allow a pull-down resistor to be set for individual pins. Such pins on the MB89P915 and MB89PV910 are fixed to have no pull-down resistor.
- The low-voltage detection reset cannot be used on the MB89PV910. The voltage to be detected by the low-voltage detection reset is set by using a register for the MB89P915 and by using a mask option for the MB89915 and MB89913. If the detection voltage has been set to a lower value than the operating voltage, however, use the gear function to operate the device with the faster clock at a lower speed, or operate the device with the slower clock. Note that the results of operation are unpredictable if the device is attempted to operate at a lower voltage than the operating voltage with the faster clock put in top gear.

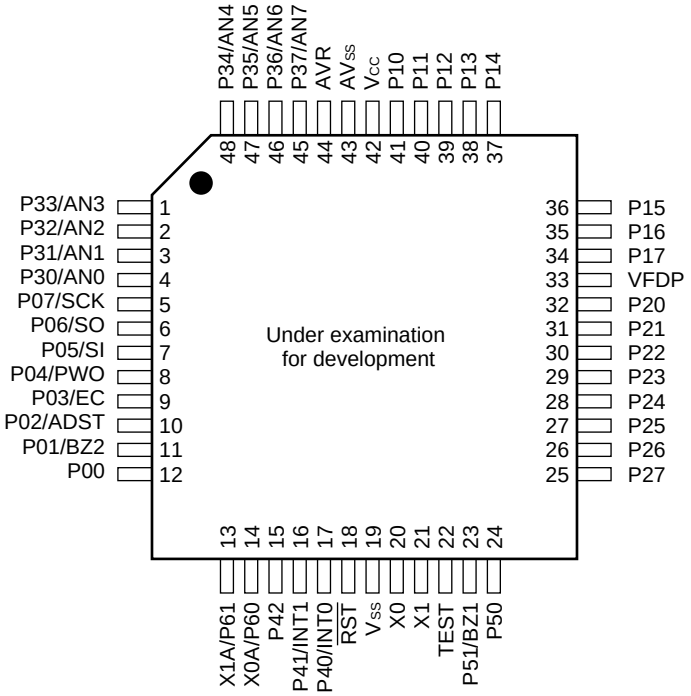
■ PIN ASSIGNMENT

(Top view)



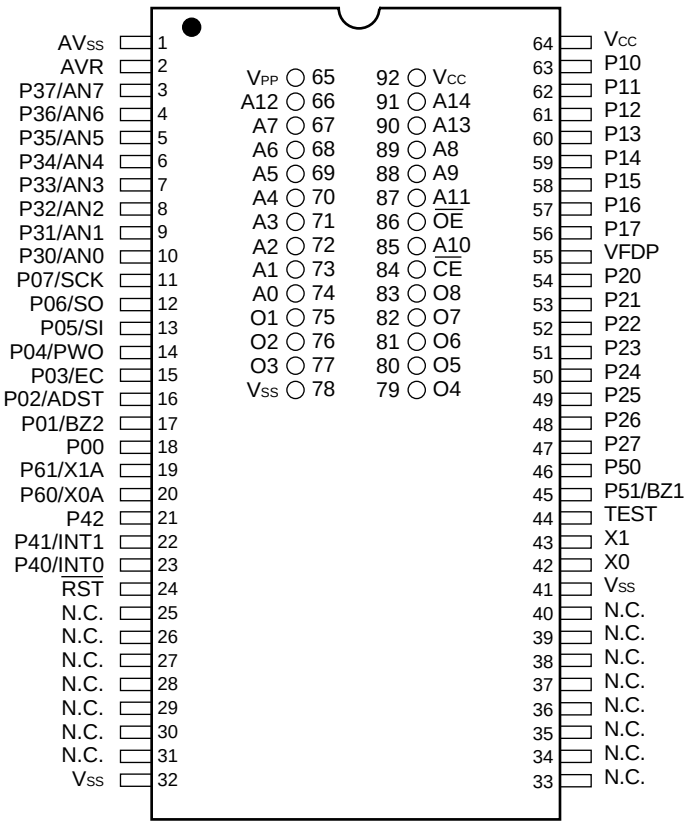
(DIP-48P-M01)

(Top view)



(FPT-48P-M15)

(Top view)



(MDP-64C-P02)

■ PIN DESCRIPTION

Pin no.			Pin name	Circuit type	Function
SH-DIP*1	QFP*2	MDIP*3			
26	20	42	X0	A	Main clock crystal oscillator pins
27	21	43	X1		
20	14	20	X0A/P60	I	These pins can select either general-purpose CMOS inputs or subclock oscillator pins by the mask options. When these pins are used as a general-purpose input pin, the pin is a hysteresis input with a built-in noise canceller.
19	13	19	X1A/P61		
24	18	24	$\overline{RST}$	C	Reset I/O pin This pin is an N-ch open-drain output type with pull-up resistor and a hysteresis input type. “L” is output from this pin by an internal source. The internal circuit is initialized by the input of “L”. This pin is with a noise canceller.
18	12	18	P00	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller.
17	11	17	P01/BZ2	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as a buzzer output.
16	10	16	P02/ADST	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as the external activation pin for the A/D converter.
15	9	15	P03/EC	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as the external clock input for the 16-bit timer/counter.
14	8	14	P04/PWO	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as the PWM output for the 8-bit PWM timer.
13, 12	7, 6	13, 12	P05/SI, P06/SO	D	General-purpose CMOS I/O ports These port inputs are a hysteresis input, with a built-in noise canceller. Also serve as serial data outputs for the 8-bit serial interface.
11	5	11	P07/SCK	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as the serial transfer clock output for the 8-bit serial interface.
47 to 40	41 to 34	63 to 56	P10 to P17	G	P-ch high-voltage open-drain output ports for large current

(Continued)

*1: DIP-48P-M01
*2: FPT-48P-M15
*3: MDP-64C-P02

(Continued)

Pin no.			Pin name	Circuit type	Function
SH-DIP*1	QFP*2	MDIP*3			
38 to 31	32 to 25	54 to 47	P20 to P27	G	P-ch high-voltage open-drain output ports for small current
10 to 7	4 to 1	10 to 7	P30/AN0 to P33/AN3	H	General-purpose N-ch open-drain I/O ports These port inputs are a hysteresis input, each with a built-in noise canceller. Although the pins are also serve as an analog inputs, an analog input does not pass through their noise cancellers.
6 to 3	48 to 45	6 to 3	P34/AN4 to P37/AN7	F	General-purpose CMOS I/O ports These port inputs are a hysteresis input, each with a built-in noise canceller. Although the pins are also serve as an analog inputs, an analog input does not pass through their noise cancellers.
23	17	23	P40/INT0	D	General-purpose CMOS I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as an external interrupt. External interrupt input passes through the noise canceller.
22	16	22	P41/INT1	E	General-purpose N-ch open-drain I/O port This port input is a hysteresis input, with a built-in noise canceller. Also serves as an external interrupt. External interrupt input passes through the noise canceller.
21	15	21	P42	E	General-purpose N-ch open-drain I/O port This port input is a hysteresis input, with a built-in noise canceller.
30	24	46	P50	G	P-ch high-voltage open-drain output ports for small current
29	23	45	P51/BZ1	G	P-ch high-voltage open-drain output port for small current Also serves as a buzzer output.
28	22	44	TEST	B	Operating mode selection pin Usually, connect to V_{SS} directly. On the product with an EPROM, the pin is the V_{PP} pin.
39	33	55	VFDP	—	Voltage supply pin connected to a pull-down resistor for ports 1, 2, and 5 In products without a pull-down resistor, in the MB89P915, and in the MB89PV910, this pin should be left open.

(Continued)

*1: IP-48P-M01
*2: FPT-48P-M15
*3: MDP-64C-P02

(Continued)

Pin no.			Pin name	Circuit type	Function
SH-DIP*1	QFP*2	MDIP*3			
48	42	64	V_{CC}	—	Power supply pin
25	19	32,41	V_{SS}	—	Power supply (GND) pin
1	43	1	AV_{SS}	—	A/D converter power supply pin Use this pin at the same voltage as V_{SS}.
2	44	2	AVR	—	A/D converter reference voltage input pin

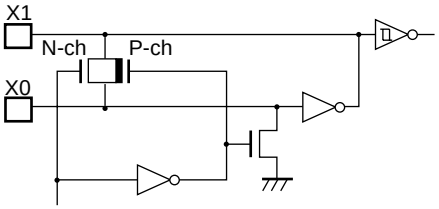
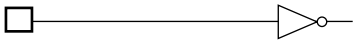
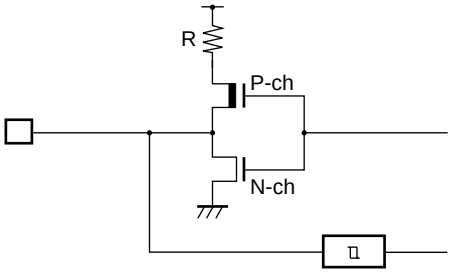
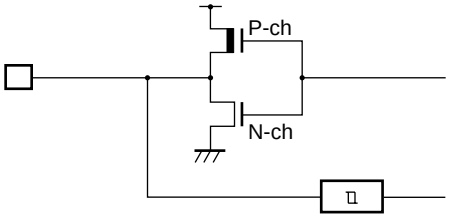
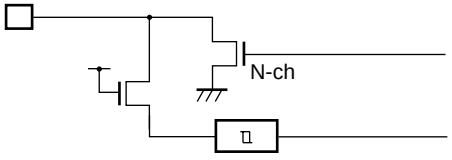
*1: IP-48P-M01
*2: FPT-48P-M15
*3: MDP-64C-P02

- **External EPROM pins (MDIP only)**

Pin no. MDIP*	Pin name	I/O	Function
65	V_{PP}	O	“H” level output pin
66 67 68 69 70 71 72 73 74	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
75 76 77	O1 O2 O3	I	Data input pins
78	V_{SS}	O	Power supply (GND) pin
79 80 81 82 83	O4 O5 O6 O7 O8	I	Data input pins
84	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
85	A10	O	Address output pin
86	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
87 88 89	A11 A9 A8	O	Address output pin
90	A13	O	
91	A14	O	
92	V_{CC}	O	EPROM power supply pin

* : MDP-64C-P02

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	 Main clock control signal	• Main clock At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
B		
C	 Hysteresis input (with a noise canceller)	• At an output pull-up resistor (P-ch) of approximately 50 kΩ/5.0 V • CMOS hysteresis input (with a noise canceller)
D	 Hysteresis input (with a noise canceller)	• CMOS I/O • CMOS hysteresis input (with a noise canceller)
E	 Hysteresis input (with a noise canceller)	• N-ch open-drain I/O • CMOS hysteresis input (with a noise canceller)

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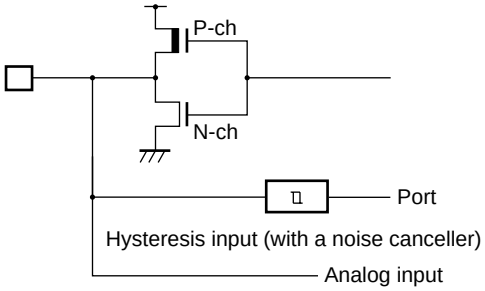
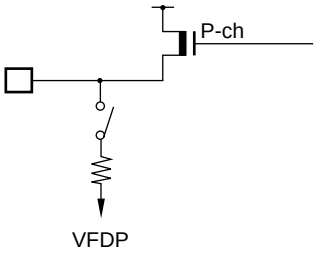
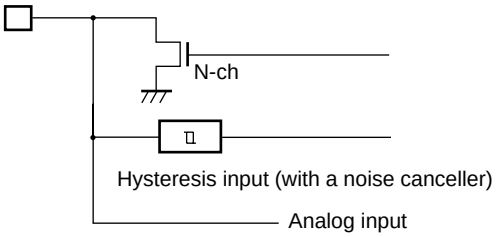
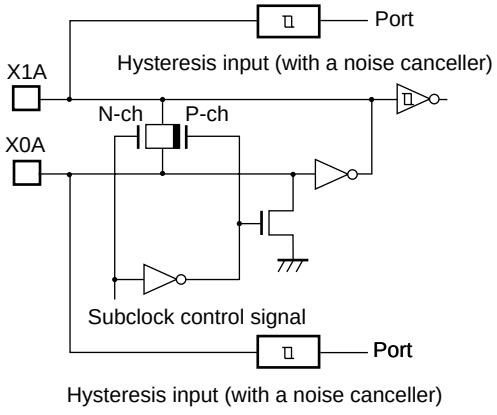
Type	Circuit	Remarks
F		• CMOS output • CMOS hysteresis input (with a noise canceller excluding analog inputs)
G		• P-ch high-voltage open-drain output • At an output pull-down resistor of approximately 100 kΩ/5.0 V
H		• N-ch open-drain output • CMOS hysteresis input (with a noise canceller excluding analog inputs)
I		• Subclock The oscillation feedback resistor is built only in the MB89PV910. • CMOS hysteresis input (with a noise canceller) when no subclock is being used

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- and high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

When an external clock is used, oscillation stabilization time is required even for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO EPROM ON THE MB89P915

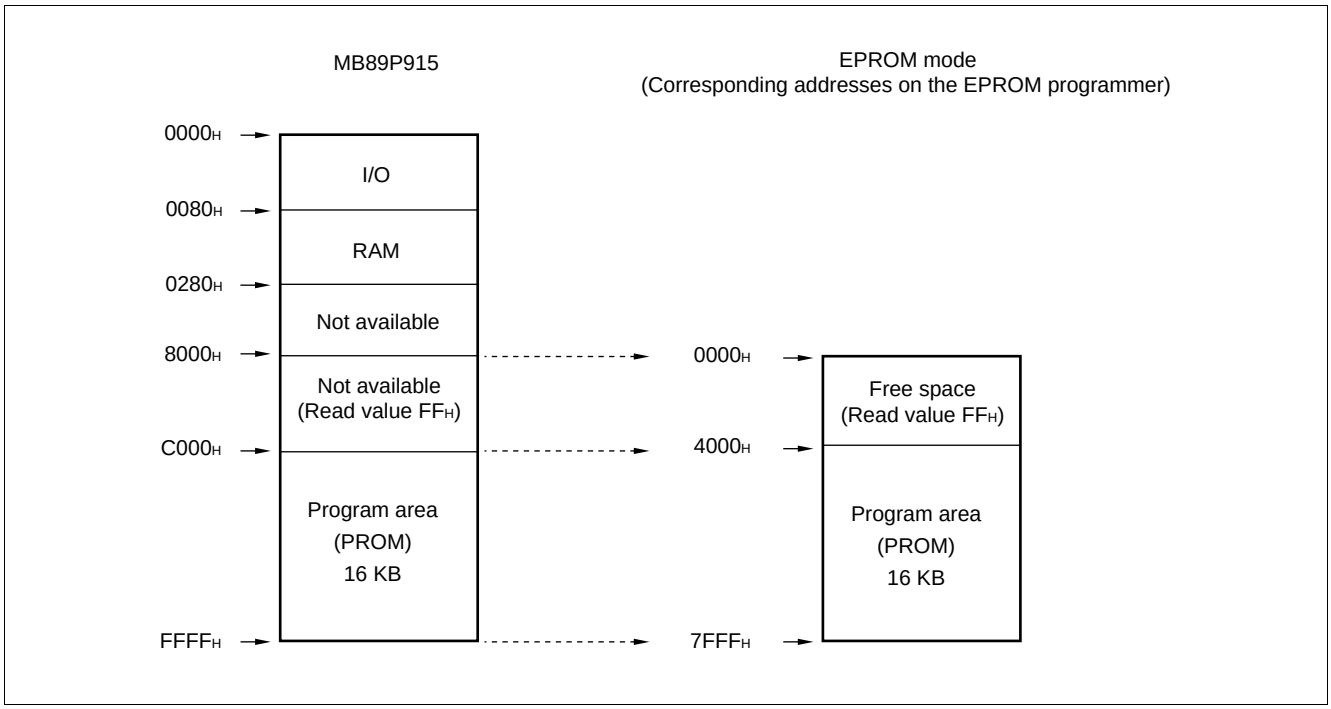
The MB89P915 is an OTPROM version of the MP89910 series.

1. Features

- 16-Kbyte PROM on chip

2. Memory Space

Memory space in each mode such as 16-Kbyte PROM mode is diagrammed below.



3. Programming to the EPROM

Since the MB89P915 requires a special method for programming to its PROM, the types of general-purpose EPROM programmers applicable to the MB89P915 are limited. Programming to the PROM on the MB89P915 requires an EPROM programmer applicable to the MB89P915 and a dedicated adapter.

When the operating ROM area for a single chip is 16 Kbytes ($C000_H$ to $FFFF_H$) the PROM can be programmed as follows:

- **Programming procedure**

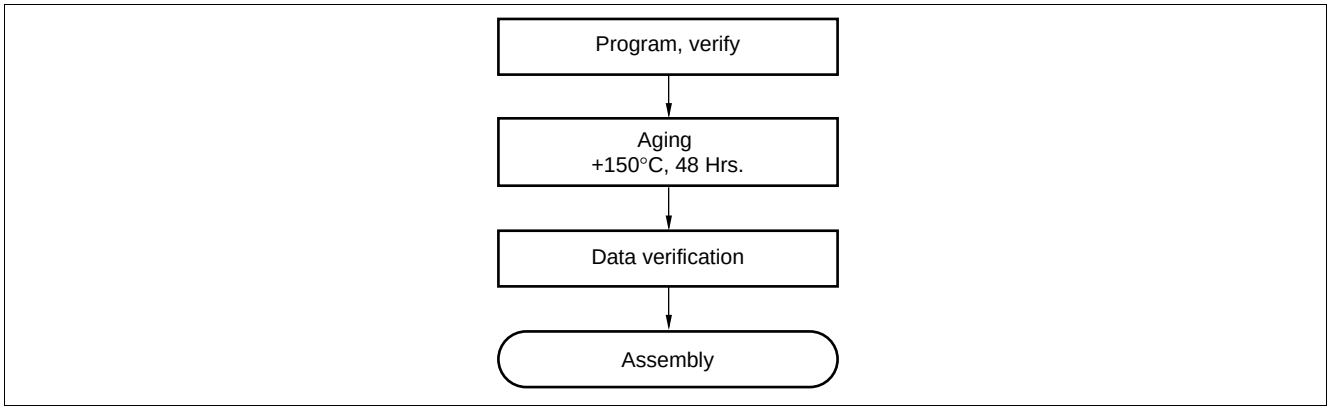
(1) Set the EPROM programmer to the MB89P195.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$. (note that addresses $0C000_H$ to $0FFFF_H$ in the operation mode correspond to 4000_H to $7FFF_H$ in EPROM mode.)

(3) Program with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter and Recommended Programmer Manufacturer

Part no.	Package	Compatible socket adapter Sun Hayato Co., Ltd.	Recommended programmer manufacturer and programmer name		
			Data I/O Co., Ltd.		
			UNISITE (ver.5.0 or later)	3900 (ver.2.8 or later)	2900 (ver.3.8 or later)
MB89P915P-SH	SH-DIP-48	ROM-48QF2-28DP-8L	Recommended		

Inquiry: Sun Hayato Co., Ltd.: TEL: (81)-3-3986-0403
FAX: (81)-3-5396-9106
Data I/O Co., Ltd.: TEL: USA/ASIA (1)-206-881-6444
EUROPE (49)-8-985-8580

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

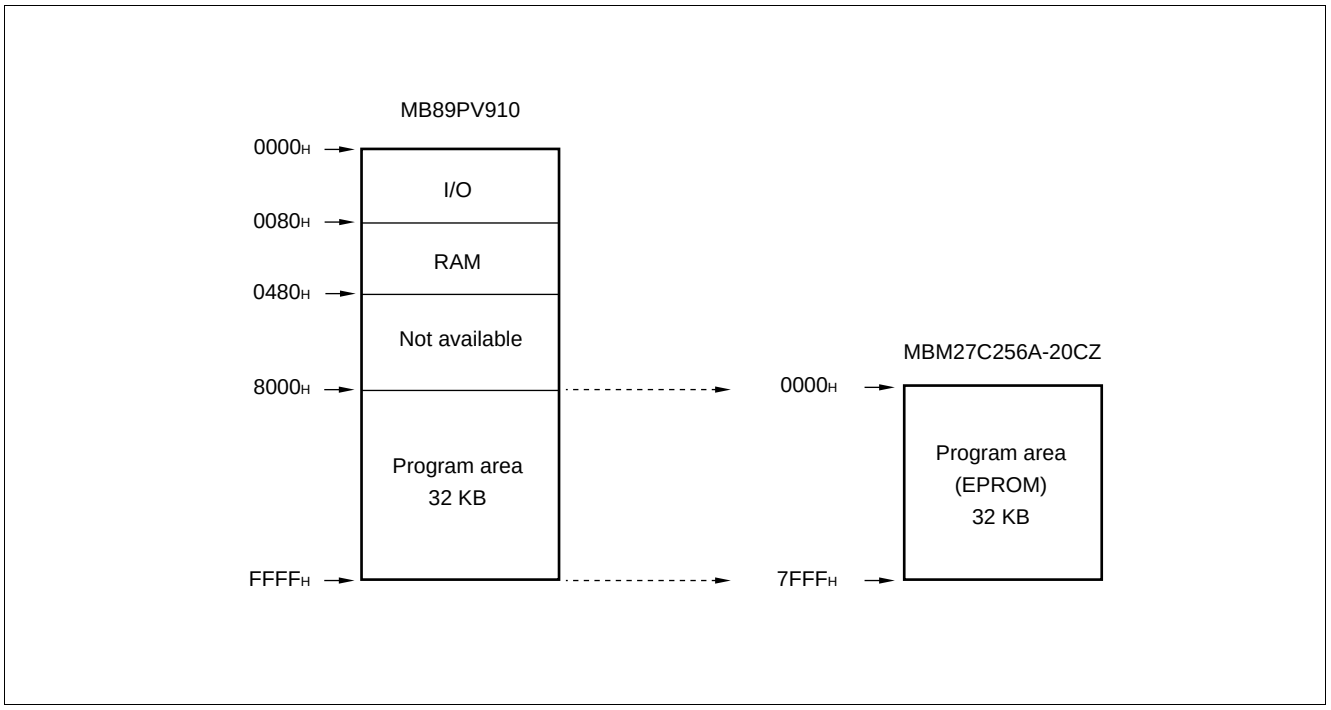
MBM27C256A-20CZ

2. Programming Socket Adapter

Any special programming adapter is not required since the package for the EPROM to be used is DIP-28.

3. Memory Space

EPROM memory space and the memory space on the MB89PV910 are diagrammed below.



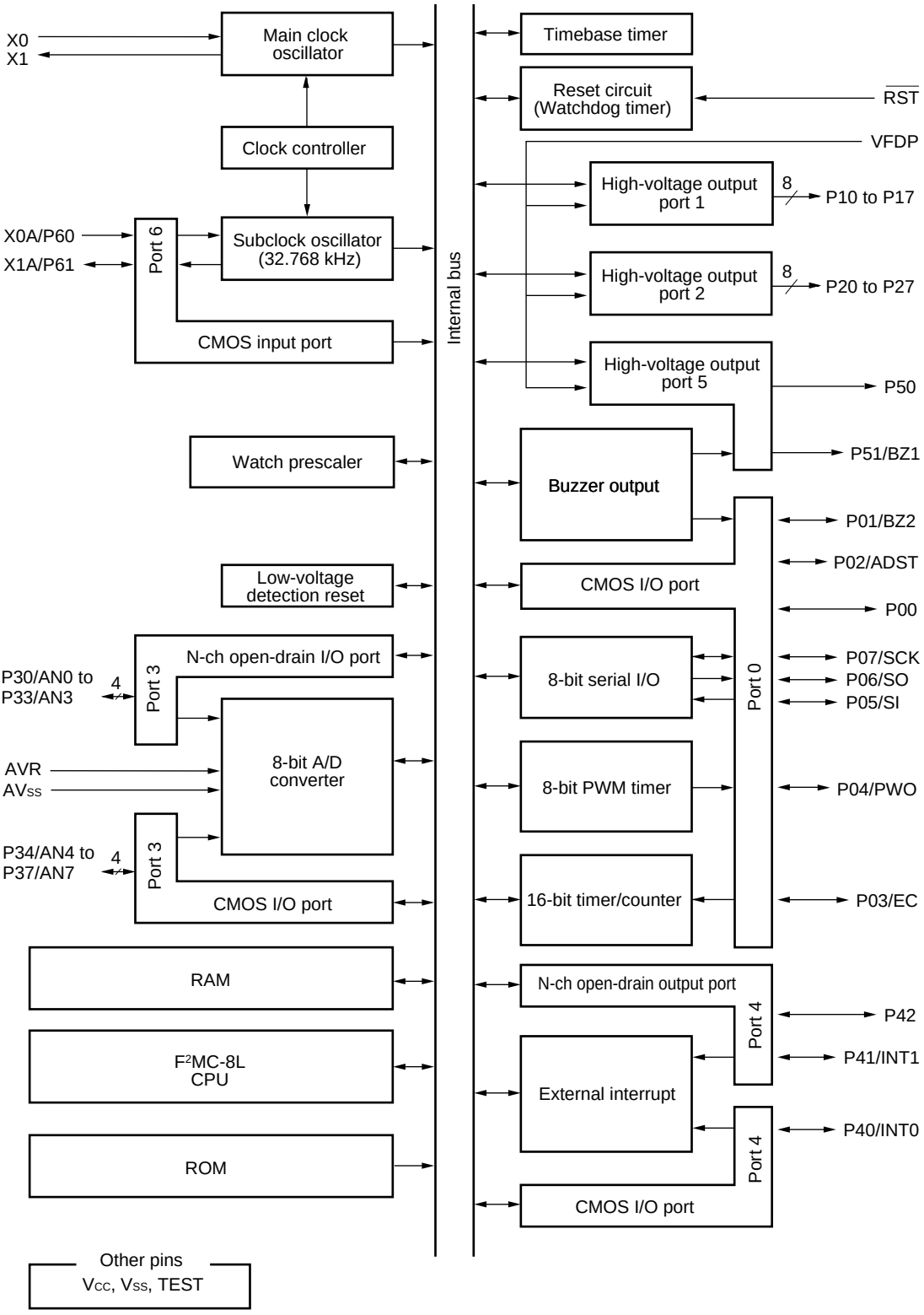
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A-20CZ.

(2) Load program data into the EPROM programmer at 0000_H to $7FFF_H$. (note that addresses 08000_H to $0FFFF_H$ in the operation mode correspond to 0000_H to $7FFF_H$ in the EPROM mode.)

(3) Program with the EPROM programmer.

■ BLOCK DIAGRAM

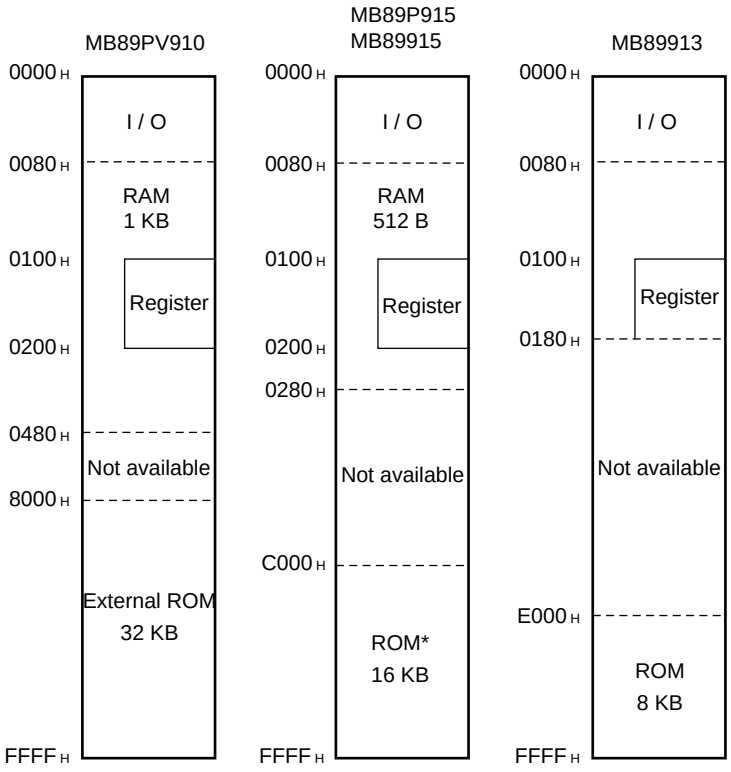


■ CPU CORE

1. Memory Space

The microcontrollers of the MB89910 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area.

- **Memory Space**

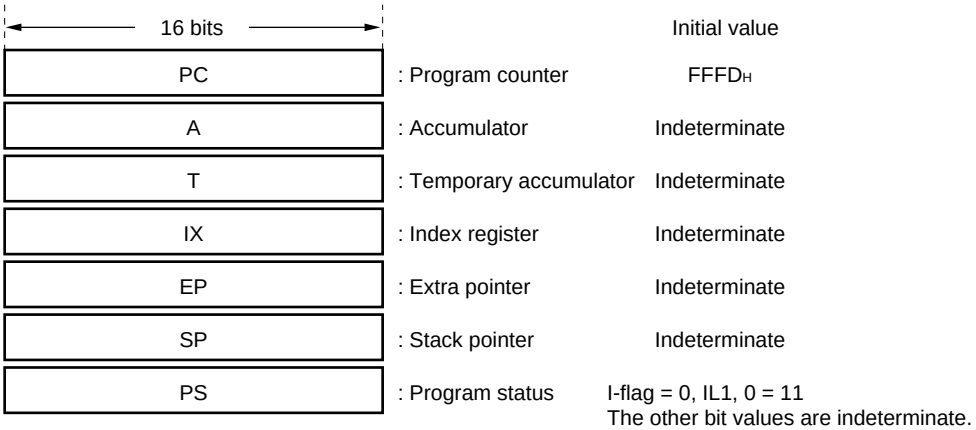


*: This is an internal PROM on the MB89P915.

2. Registers

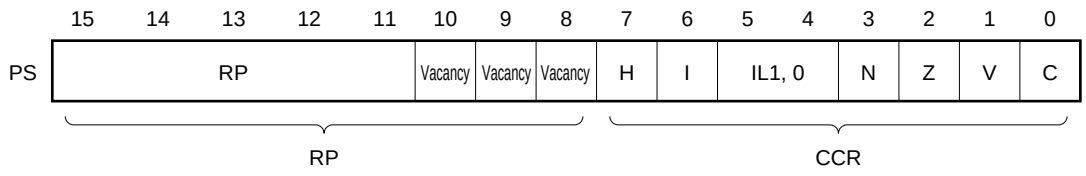
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



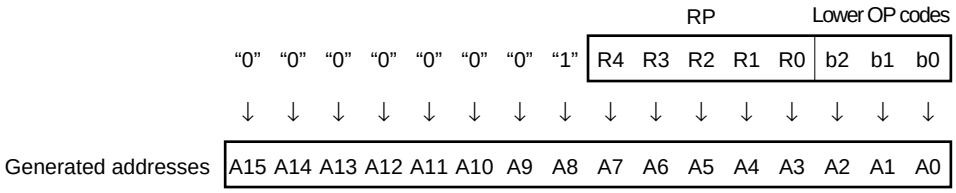
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- **Structure of the Program Status Register**



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

- **Rule for Conversion of Actual Addresses of the General-purpose Register Area**



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set to '1' when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is enabled when this flag is set to '1'. Interrupt is disabled when the flag is cleared to '0'. Cleared to '0' at the reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low

N-flag: Set to '1' if the MSB becomes to '1' as the result of an arithmetic operation. Cleared to '0' when the bit is cleared to '0'.

Z-flag: Set to '1' when an arithmetic operation results in 0. Cleared to '0' otherwise.

V-flag: Set to '1' if the complement on 2 overflows as a result of an arithmetic operation. Cleared to to '0' if the overflow does not occur.

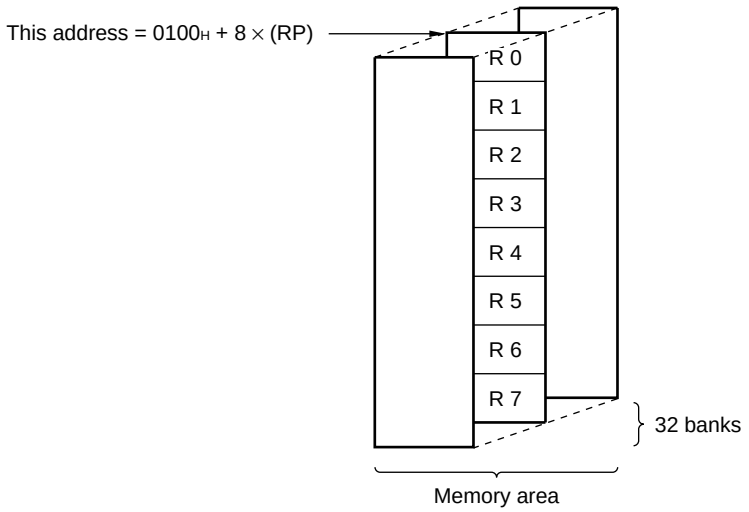
C-flag: Set to '1' when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to '0' otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: An 8-bit resister for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers and up to a total of 32 banks can be used on the MB89915. The bank currently in use is indicated by the register bank pointer (RP).

- **Register Bank Configuration**



■ I/O MAP

Address	Read/write	Register name	Register description
00H	(R/W)	PDR0	Port 0 data register
01H	(W)	DDR0	Port 0 data direction register
02H			Vacancy
03H			Vacancy
04H			Vacancy
05H			Vacancy
06H			Vacancy
07H	(R/W)	SYCC	System clock control register
08H	(R/W)	STBC	Standby control register
09H	(R/W)	WDTC	Watchdog timer control register
0AH	(R/W)	TBCR	Time-base timer control register
0BH	(R/W)	WPCR	Watch prescaler control register
0CH	(R/W)	PDR3	Port 3 data register
0DH	(W)	DDR3	Port 3 direction register
0EH	(R/W)	BUZR	Buzzer register
0FH	(R/W)	EIC	External interrupt control register
10H	(R/W)	PDR1	Port 1 data register
11H	(R/W)	PDR2	Port 2 data register
12H	(R/W)	PDR5	Port 5 data register
13H	(R)	PDR6	Port 6 data register
14H	(R/W)	PDR4	Port 4 data register
15H	(W)	DDR4	Port 4 direction register
16H	(W)	COMR	PWM compare register
17H	(R/W)	CNTR	PWM control register
18H	(R/W)	TMCR	16-bit timer control register
19H	(R/W)	TCHR	16-bit timer control register (H)
1AH	(R/W)	TCLR	16-bit timer control register (L)
1BH			Vacancy
1CH	(R/W)	SMR	Serial mode register
1DH	(R/W)	SDR	Serial data register
1EH	(R/W)	ADC1	A/D converter control register 1
1FH	(R/W)	ADC2	A/D converter control register 2

(Continued)

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Address	Read/write	Register name	Register description
20H	(R/W)	ADCD	A/D converter data register
21H	Vacancy		
22H	(W)	PCR	Port input control register
23H	(R/W)	LVRC	Low-voltage detection reset control register
24H to 7BH	Vacancy		
7CH	(W)	ILR1	Interrupt level setting register 1
7DH	(W)	ILR2	Interrupt level setting register 2
7EH	(W)	ILR3	Interrupt level setting register 3
7FH	Vacancy		

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

($AV_{SS} = V_{SS} = 0.0$ V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC} AVR	$V_{SS} - 0.3$	$V_{SS} + 7.0$	V	AVR ≤ V_{CC} + 0.3*1
	V_{PP}	– 0.6	13.0	V	
	VFDP	$V_{CC} - 40$	$V_{CC} + 0.3$	V	
Input voltage	V_{I1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P41*2
	V_{I2}	$V_{SS} - 0.3$	7.0	V	P41
Output voltage	V_{O1}	$V_{SS} - 0.3$	$V_{CC} + 0.3$	V	Except P10 to P17, P20 to P27, P50, P51*2
	V_{O2}	$V_{CC} - 40.0$	$V_{CC} + 0.3$	V	P10 to P17, P20 to P27 P50, P51
“H” level total maximum output current	$\sum I_{OH}$	—	–120	mA	
“H” level total average output current	$\sum I_{OHAV}$	—	–90	mA	Average value (operating current × operating rate)
“H” level maximum output current	I_{OH}	—	–12	mA	P00 to P07, P34 to P37, P40
		—	–20	mA	P20 to P27, P50, P51
		—	–36	mA	P10 to P17
“H” level average output current	I_{OHAV}	—	–6	mA	P00 to P07, P34 to P37, P40 Average value (operating current × operating rate)
		—	–10	mA	P20 to P27, P50, P51 Average value (operating current × operating rate)
		—	–20	mA	P10 to P17 Average value (operating current × operating rate)
“L” level total maximum output current	$\sum I_{OL}$	—	36	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	20	mA	Average value (operating current × operating rate)
“L” level maximum output current	I_{OL}	—	10	mA	P00 to P07, P30 to P37, P40 to P47
“L” level average output current	I_{OLAV}	—	4	mA	

(Continued)

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(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power consumption	P_D	—	440	mW	SH-DIP: DIP-48-M01
		—	360	mW	QFP: FPT-48-M15
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1: Take care so that AVR does not exceed V_{CC} + 0.3 V and V_{CC} does not exceed V_{CC}, such as when power is turned on.

*2: V_I and V_O must not exceed V_{CC} + 0.3 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(AV_{SS} = V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	4.5*	5.5*	V	Normal operation assurance range*(MB89PV910)
		3.8*	5.5*	V	Normal operation assurance range*(MB89P915/915/913)
		2.7	5.5	V	Watch mode, sub-RUN mode
		1.5	5.5	V	Retains the RAM state in stop mode
A/D converter reference input voltage	AVR	0.0	V_{CC}	V	
High-voltage pull-down resistor supply voltage	VFDP	V_{CC} – 35.0	V_{CC} + 0.3	V	
Operating temperature	T_A	–40	+85	°C	

* : These values vary with the operating frequency, instruction cycle, and analog assurance range. See Figure 1 and “5. A/D Converter Electrical Characteristics.”

Figure 1 Operating Voltage vs. Main Clock Operating Frequency

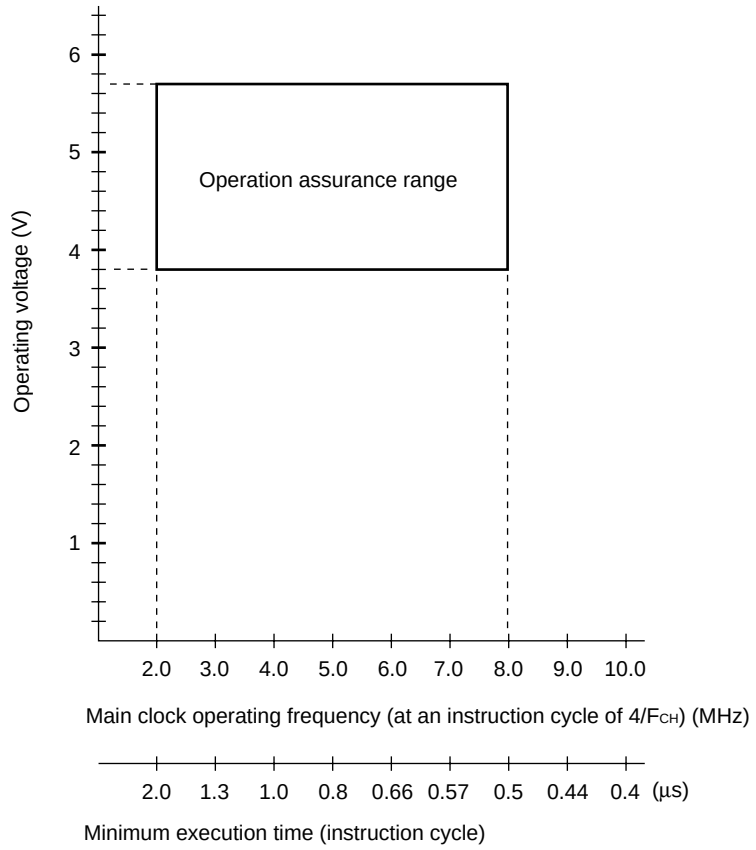

Figure 1 indicates the operating frequency of the external oscillator at an instruction cycle of $4/F_{CH}$.

Since the operating voltage range is dependent on the instruction cycle, see minimum execution time if the operating speed is switched using a gear.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

3. DC Characteristics

(AVR = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IHS}	P00 to P07, P30 to P37, P40 to P42, P60, P61 X0, $\overline{RST}$ X1, TEST	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	P00 to P07, P30 to P37, P40 to P42, P60, P61 X0, $\overline{RST}$ X1, TEST	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
Open-drain output pin application voltage	V_{D1}	P30 to P33, P42	—	V_{SS} – 0.3	—	V_{CC} + 0.3	V	
	V_{D2}	P41	—	V_{SS} – 0.3	—	7.0	V	
"H" level output voltage	V_{OH1}	P00 to P07, P30 to P37, P40 to P42, P60, P61	I_{OH} = –2.0 mA	2.4	—	—	V	Excluding P30 to P33 and P41, P42
	V_{OH2}	P20 to P27, P50, P51	I_{OH} = –10 mA	3.0	—	—	V	
	V_{OH3}	P10 to P17	I_{OH} = –20 mA	3.0	—	—	V	
"L" level output voltage	V_{OL1}	P00 to P07, P30 to P37, P40 to P42, P60, P61	I_{OL} = 1.8 mA	—	—	0.4	V	
	V_{OL2}	$\overline{RST}$,	I_{OL} = 4.0 mA	—	—	0.6	V	
Input leakage current	I_{LI1}	P00 to P07, P30 to P37, P40 to P42, P60, P61	0 < V_I < V_{CC}	—	—	±5	µA	
Output leakage current	I_{LO1}	P20 to P27, P50, P51	V_I = VFDP	—	—	–10	µA	VFDP = V_{CC} – 35.0 V
	I_{LO2}	P10 to P17	V_I = VFDP	—	—	–20	µA	VFDP = V_{CC} – 35.0 V
Pull-up resistance	R_{PULL}	$\overline{RST}$,	V_{IN} = 0.0 V	25	50	100	kΩ	
Pull-down resistance	R_{PD}	P10 to P17, P20 to P27, P50, P51	V_{IN} = 5.0 V	50	100	150	kΩ	Assuming the pull-down resistor option selected

(Continued)

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(AVR = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1 When low-voltage detection reset operation is enabled, I_{LVD} is added to each power supply current.	I_{CC1}	V_{CC}	F_{CH} = 8 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.5 µs when A/D conversion is stopped	—	10.0	18.0	mA	MB89P915
				—	9	15	mA	MB89913/ 915/PV910
	I_{CC2}		F_{CH} = 8 MHz, V_{CC} = 3.8 V, t_{inst}*2 = 8.0 µs when A/D conversion is stopped	—	3.0	6.0	mA	MB89P915
				—	1.8	2.4	mA	MB89913/ 915/PV910
	I_{CS1}		Sleep mode: F_{CH} = 8 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.5 µs when A/D conversion is stopped	—	3	7	mA	
	I_{CS2}		Sleep mode: F_{CH} = 8 MHz, V_{CC} = 3.8 V, t_{inst}*2 = 8.0 µs when A/D conversion is stopped	—	1.2	1.8	mA	
	I_{CSB}		F_{CL} = 32 kHz, V_{CC} = 3.0 V, Subclock mode	—	1.2	3.6	mA	MB89P915
				—	60	180	µA	MB89913/ 915/PV910
	I_{CS3}		F_{CL} = 32 kHz, V_{CC} = 3.0 V, Subclock sleep mode	—	32	64	µA	
	I_{CCT}		F_{CL} = 32 kHz, V_{CC} = 3.0 V • Watch mode • Main clock stop mode at dual- clock system	—	4	20	µA	
	I_{CCA}		F_{CH} = 8 MHz, T_A = +25°C, V_{CC} = 5.0 V, t_{inst}*2 = 0.5 µs when A/D conversion is activated	—	12.5	22.5	mA	

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(AVR = V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Sym-bol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Power supply current*1	I_{CCH}	V_{CC}	F_{CL} = 32.678 kHz, V_{CC} = 3.0 V, T_A = +25°C, • Subclock stop mode • Main clock stop mode at single clock system	—	—	10	µA	
When low-voltage detection reset operation is enabled, I_{LVD} is added to each power supply current.	I_{LVD}		V_{CC} = 5.0 V, T_A = +25°C, • Subclock stop mode • Main clock stop mode at single clock system	—	60	120	µA	Power consumption of low-voltage detection reset
	I_R	AVR	F_{CH} = 8 MHz, T_A = +25°C, when A/D conversion is activated	—	200	—	µA	
	I_{RH}	AVR	F_{CH} = 8 MHz, T_A = +25°C, when A/D conversion is stopped	—	—	10	µA	
Input capacitance	C_{IN}	Other than AV_{SS}, AVR, V_{CC}, and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The power supply current is measured at external clock.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

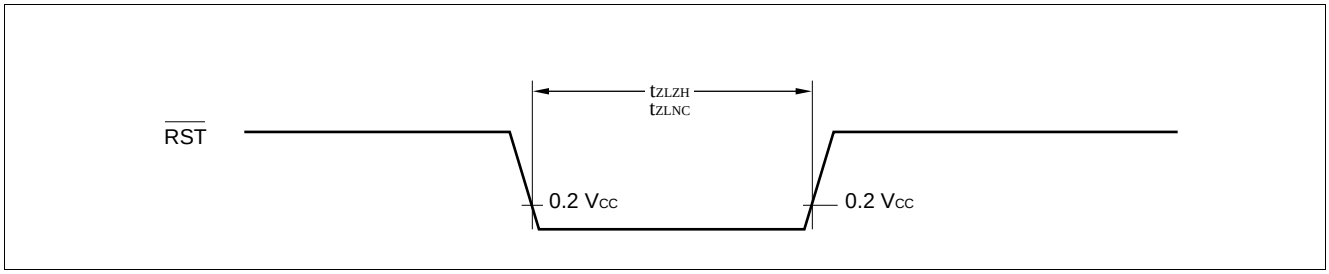
4. AC Characteristics

(1) Reset Timing

($AVR = V_{CC} = +5.0\ V \pm 10\%$, $AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min.	Typ.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{XCYL}	—	—	ns	
$\overline{RST}$ noise limit width	t_{ZLNC}	—	30	50	80	ns	

Note: t_{XCYL} is the oscillation period ($1/F_{CH}$) to input to the X0.

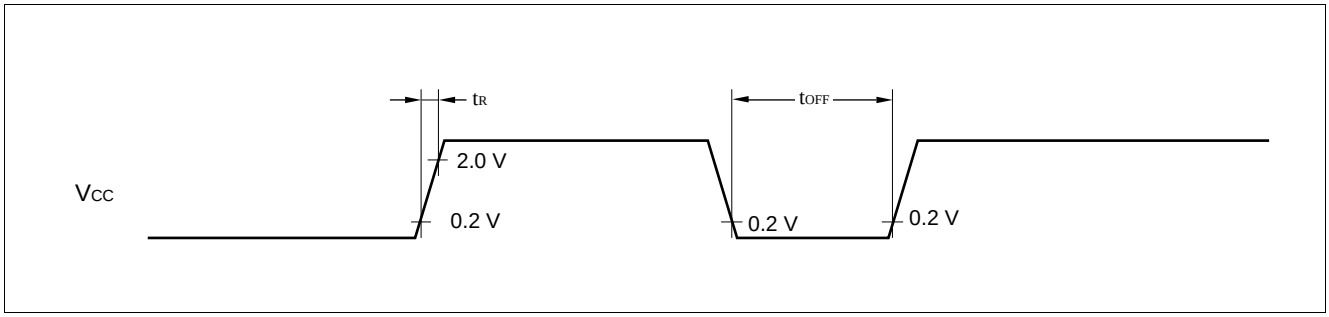


(2) Power-on Reset

($AV_{SS} = V_{SS} = 0.0\ V$, $T_A = -40°C$ to $+85°C$)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}	—	1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

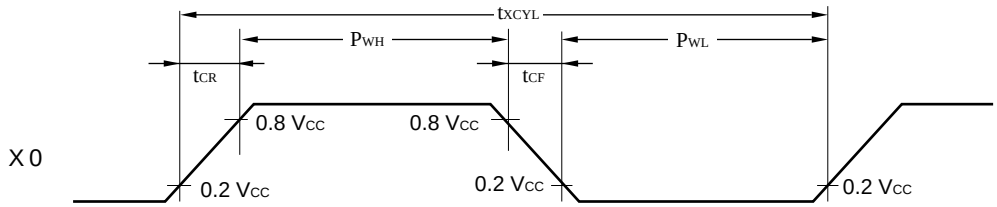


(3) Clock Timing

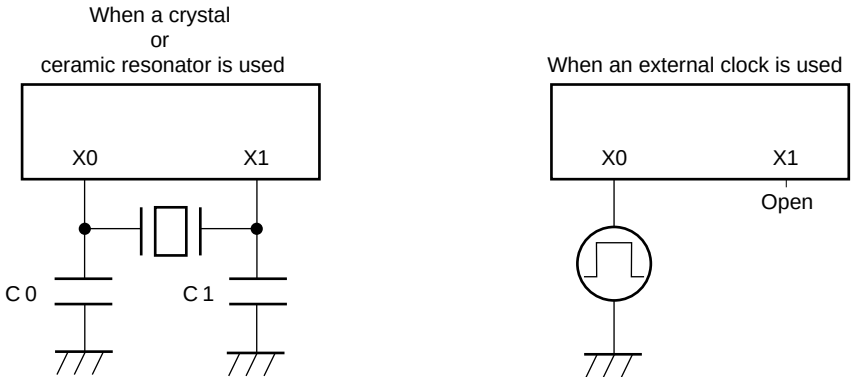
(AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	—	2	—	8	MHz	
	F_{CL}	X0A, X1A	—	—	32.768	—	kHz	
Clock cycle time	t_{XCYL}	X0, X1	—	125	—	500	ns	
	t_{LXCYL}	X0A, X1A	—	—	30.5	—	µs	
Input clock pulse width	P_{WH} P_{WL}	X0	—	30	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A	—	—	15.2	—	µs	
Input clock rising/falling time	t_{CR} t_{CF}	X0, X0A	—	—	—	10	ns	External clock

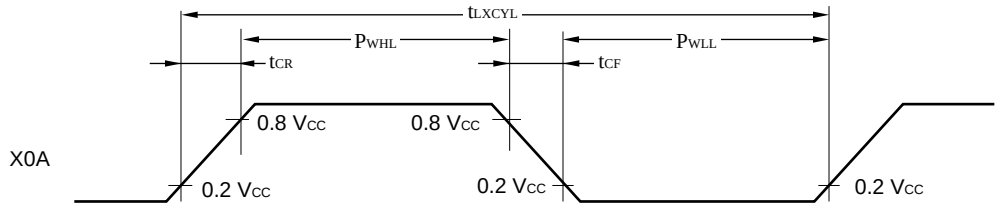
• **X0 and X1 Timing and Conditions**



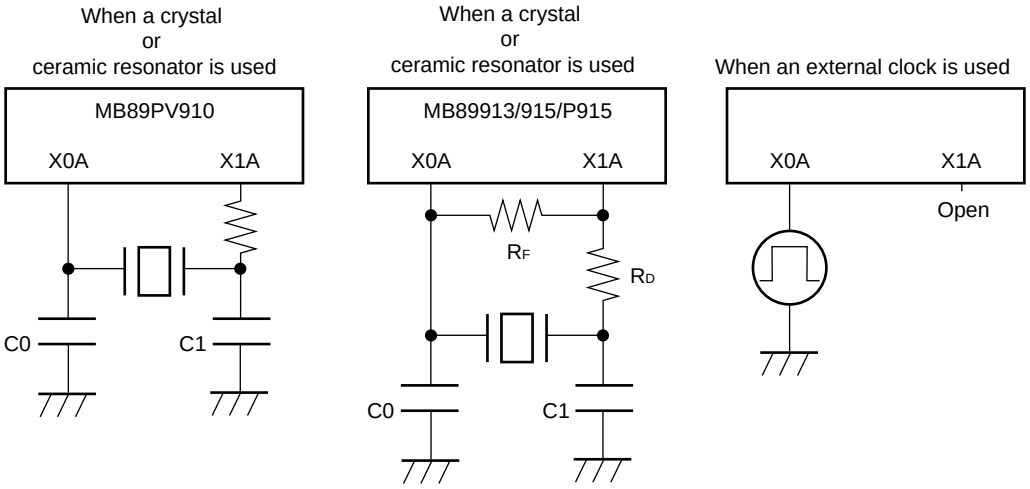
• **Main Clock Conditions**



• **X0A and X1A Timing and Conditions**



• **Subclock Conditions**



(4) Instruction Cycle

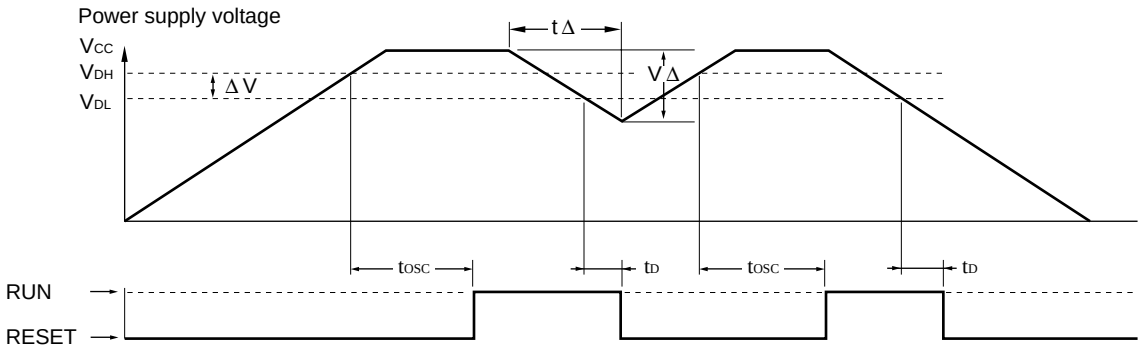
Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $32/F_{CH}$	µs	Operation at F_{CH} = 8 MHz; $(4/F_{CH})t_{inst}$ = 0.5 µs
		$2/F_{CL}$	µs	Operation at F_{CL} = 32.768 kHz; $(4/F_{CH})t_{inst}$ = 61.036 µs

Note: When operating at 8 MHz, the cycle varies with the execution time.

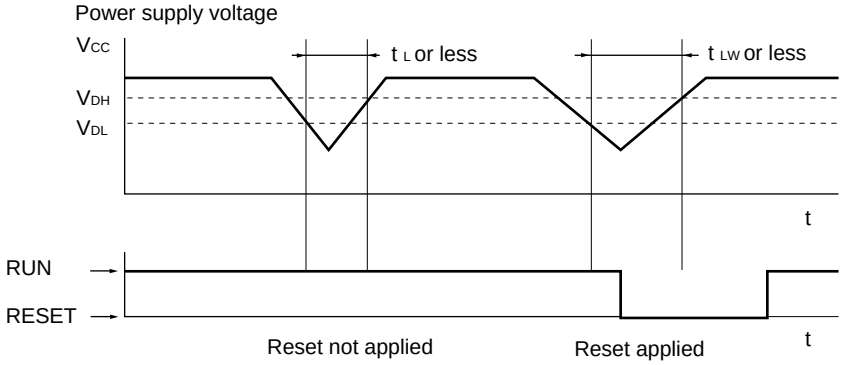
(5) Low-voltage Detection Reset

(AV_{SS} = V_{SS} 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Detection voltage at power supply voltage fall	V_{DL1}	—	3.00	3.60	V	V_{DH} and V_{DL} are set for the MB89913/915 by mask options and for the MB89P915 by a register.
	V_{DL2}	—	3.30	3.90	V	
	V_{DL3}	—	3.70	4.40	V	
Detection voltage at power supply voltage rise	V_{DH1}	—	3.10	3.80	V	
	V_{DH2}	—	3.40	4.10	V	
	V_{DH3}	—	3.80	4.60	V	
Hysteresis width	ΔV	—	0.10	—	V	
Reset insensitive time	t_L	—	0.3	—	µs	
Reset sensitive width	t_{LW}	—	16 t_{XCYL}	—	ns	
Reset detection delay time	t_D	—	—	2.0	µs	
Voltage regulation (VΔ/tΔ)	VCR	—	—	0.10	V/µs	



t_{OSC} oscillation stabilization time 2^{18} = 32.8 ms (F_{CH} = 8 MHz)



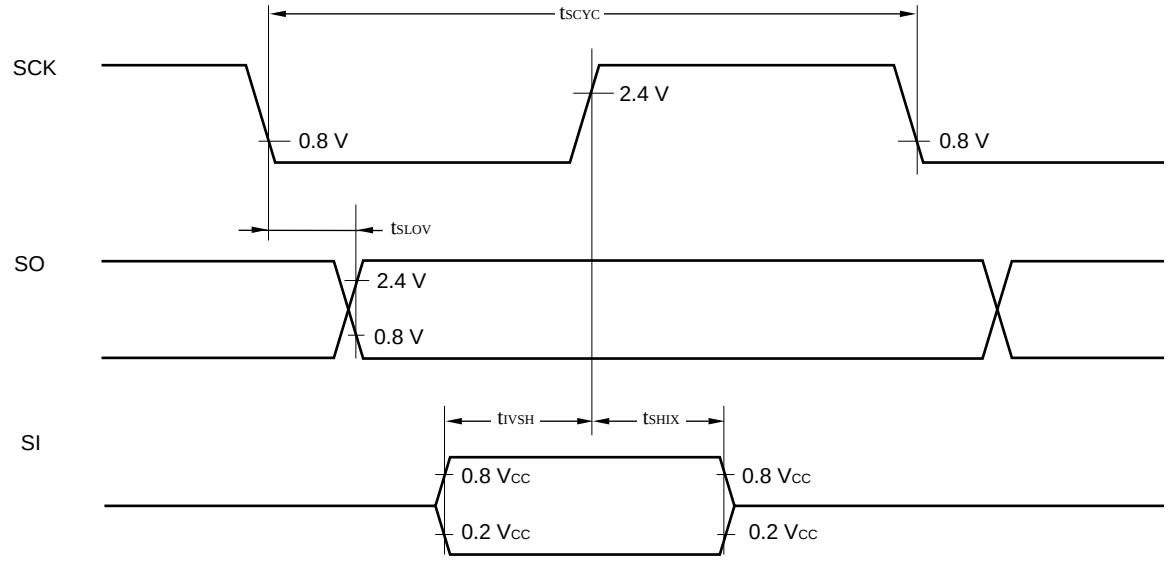
(6) Serial I/O Timing

(AVR = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

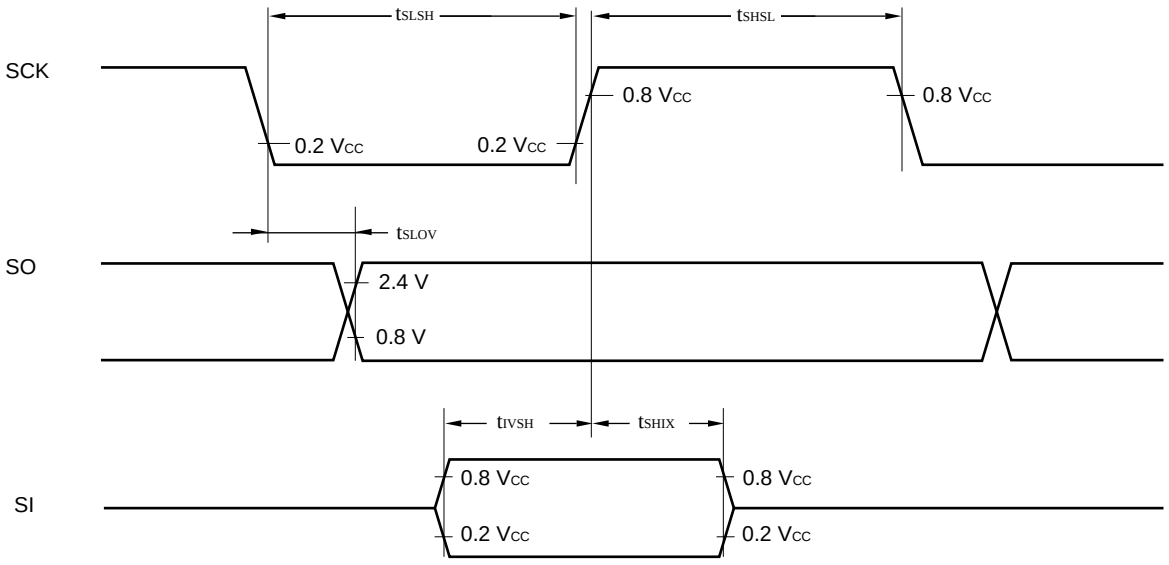
Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		1/2 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		1/2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**

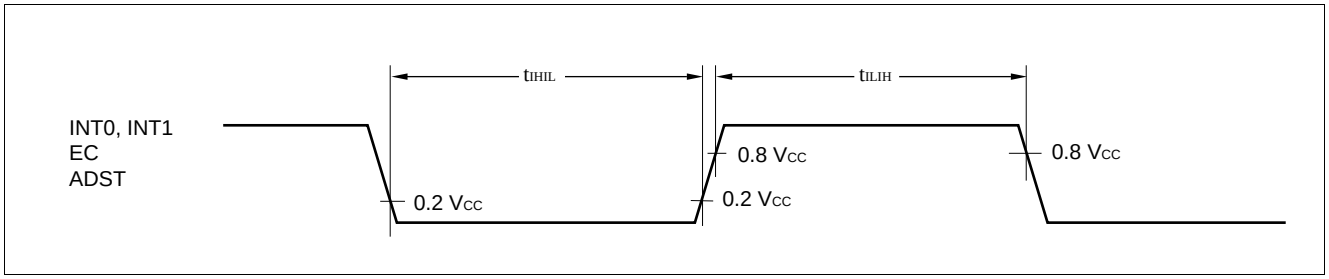


(7) Peripheral Input Timing

(AVR = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min.	Max.		
Peripheral input “H” level pulse width	t_{ILIH}	EC, ADST INT0, INT1	—	2 t_{inst}*	—	µs	
Peripheral input “L” level pulse width	t_{IHIL}	EC, ADST INT0, INT1		2 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

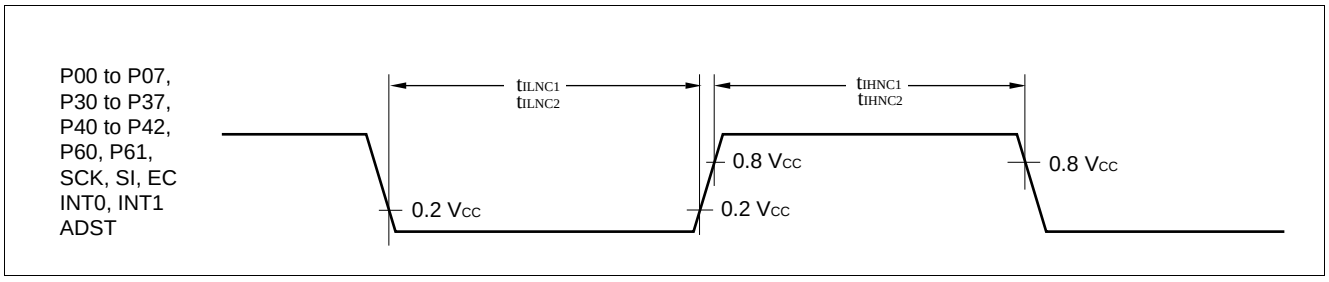


(8) Peripheral input noise limit width

(AVR = V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Peripheral input “H” level noise limit width 1	t_{IHNC1}	All inputs excluding INT1 and INT0	7	15	30	ns	MB89PV910 MB89P915
			15	30	60	ns	MB89913/ 915
Peripheral input “L” level noise limit width 1	t_{ILNC1}	All inputs excluding INT1 and INT0	7	15	30	ns	MB89PV910 MB89P915
			15	30	60	ns	MB89913/ 915
Peripheral input “H” level noise limit width 2	t_{IHNC2}	INT1, INT0	30	50	100	ns	MB89PV910 MB89P915
			50	100	250	ns	MB89913/ 915
Peripheral input “L” level noise limit width 2	t_{ILNC2}	INT1, INT0	30	50	100	ns	MB89PV910 MB89P915
			50	100	250	ns	MB89913/ 915

Note: The minimum rating is always cancelled, while values equal to or greater than maximum ratings are not cancelled.



5. A/D Converter Electrical Characteristics

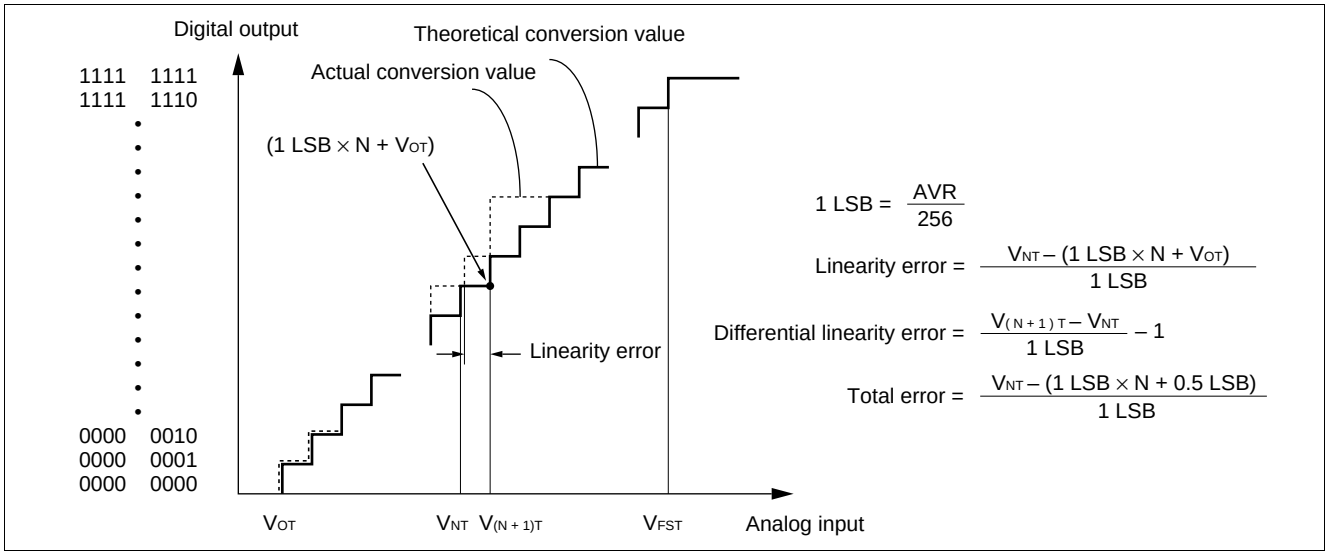
(V_{CC} = +3.8 V to +5.5 V, F = 8 MHz, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Resolution	—	—	—	—	—	8	bit	
Total error				—	—	±3.0	LSB	
Linearity error				—	—	±1.0	LSB	
Differential linearity error				—	—	±0.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	—	AV_{SS} – 1.5 LSB	AV_{SS} +0.5 LSB	AV_{SS} + 2.5 LSB	mV	
Full-scale transition voltage	V_{FST}	AN0 to AN7		AVR – 3.5 LSB	AVR – 1.5 LSB	AVR +0.5 LSB	mV	
Interchannel disparity	—	—		—	—	1.0	LSB	
A/D mode conversion time				—	44 t_{inst}*	—	µs	
Sense mode conversion time				—	12 t_{inst}*	—	µs	
Analog port input current	I_{AIN}	AN0 to AN7	AVR = V_{CC} = 5.0 V	—	—	10	µA	
Analog input voltage	—	AN0 to AN7	—	0.0	—	AVR	V	
Reference voltage		AVR		3.4	—	AV_{CC}	V	
Reference voltage supply current	I_R	AVR	AVR = 5.0 V	—	200	—	µA	

* : For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

6. A/D Converter Glossary

- Resolution
  Analog changes that are identifiable with the A/D converter
  When the number of bits is 8, analog voltage can be divided into 2^8 = 256.
- Linearity error (unit: LSB)
  The deviation of the straight line drawn connecting the zero transition point (“0000 0000 ” ↔ “0000 0001”) with the full-scale transition point (“1111 1111 ” ↔ “1111 1110”) from actual conversion characteristics
- Differential linearity error (unit: LSB)
  The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value
- Total error (unit: LSB)
  The difference between theoretical and actual conversion values



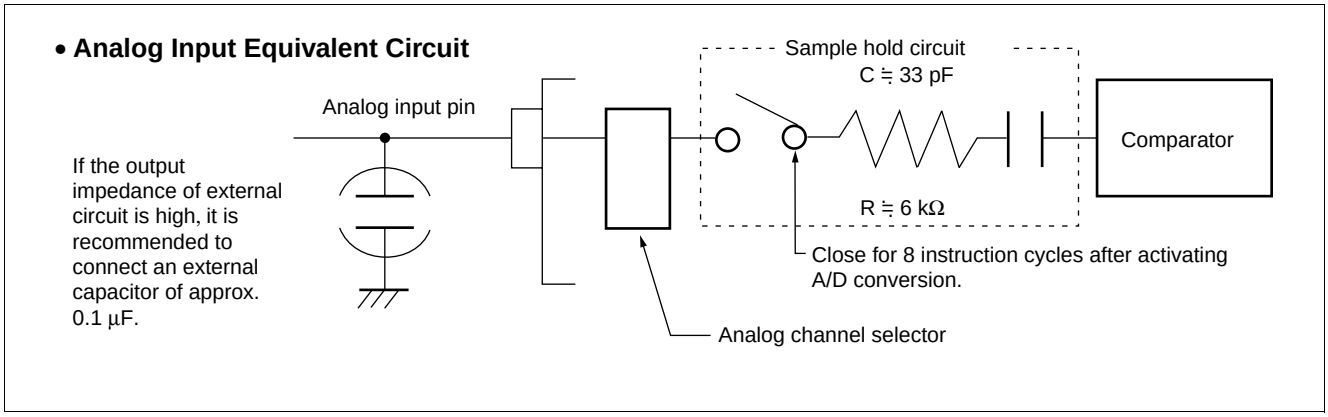
7. Notes on Using A/D Converter

- **Input impedance of the analog input pins**

  The A/D converter used for the MB89910 series contains a sample hold circuit as illustrated below to fetch analog input voltage into the sample hold capacitor for eight instruction cycles after activating A/D conversion.

  For this reason, if the output impedance of the external circuit for the analog input is high, analog input voltage might not stabilize within the analog input sampling period. Therefore, it is recommended to keep the output impedance of the external circuit low. If a higher accurancy is required, set the output impedance in this series to 2 kΩ or less.

  Note that if the impedance cannot be kept low output impedance, it is recommended either to use the software to continuously activate the A/D converter for simulating longer sampling time or to connect an external capacitor of approx. 0.1 μF to the analog input pin.

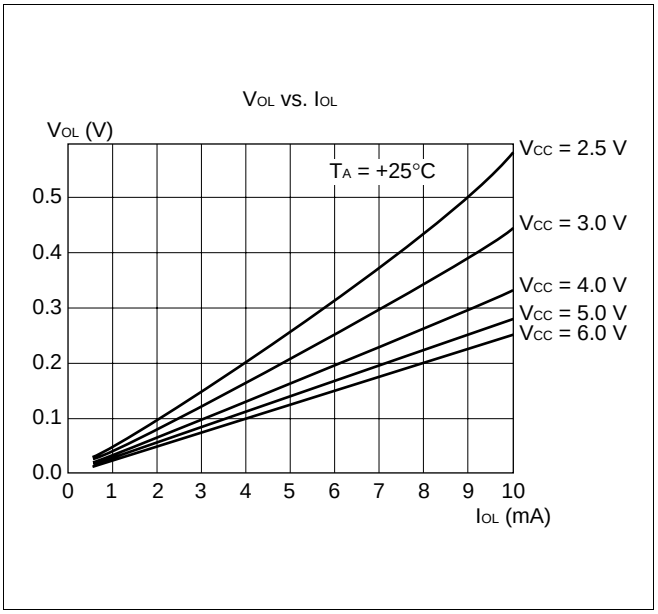


- **Error**

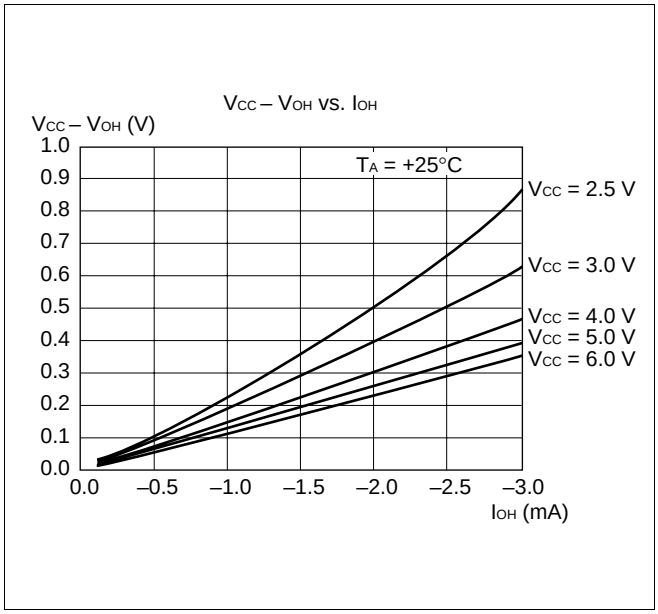
  The smaller the | AVR – AVSS |, the greater the error would become relatively.

■ EXAMPLE CHARACTERISTICS

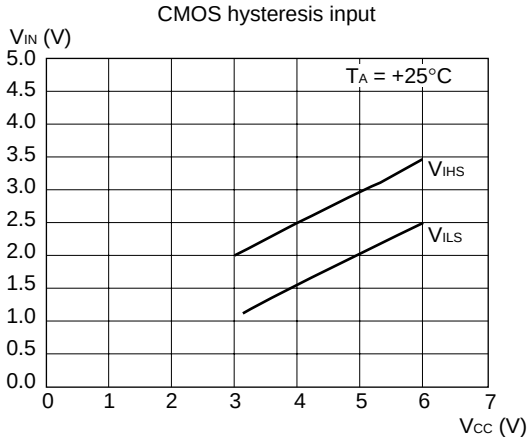
(1) “L” Level Output Voltage



(2) “H” Level Output Voltage



(3) “H” Level Input Voltage/“L” Level Input Voltage (Hysteresis Input)

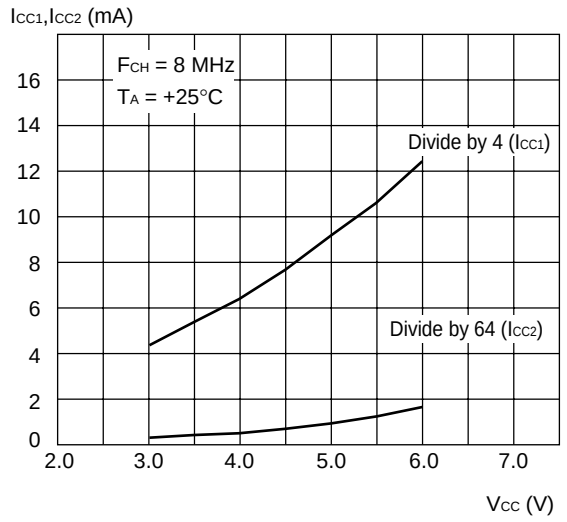


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to “H” level

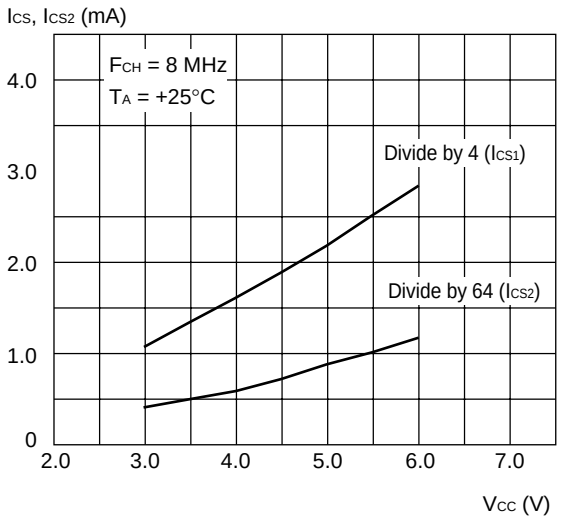
V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to “L” level

(4) Power Supply Current (External Clock)

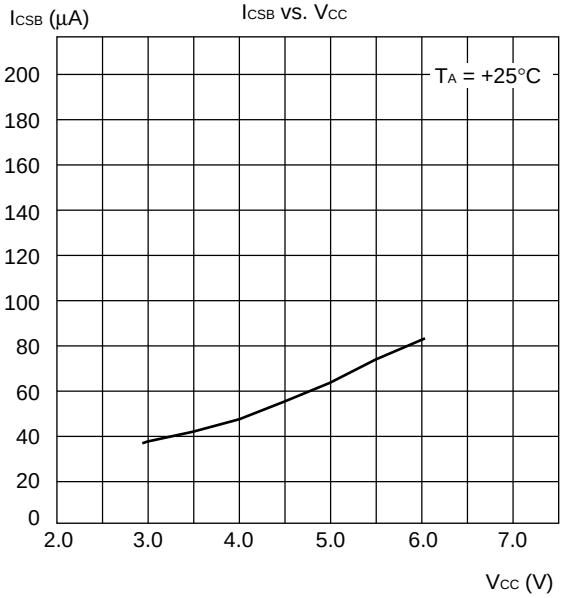
I_{CC1} vs. V_{CC}, I_{CC2} vs. V_{CC}



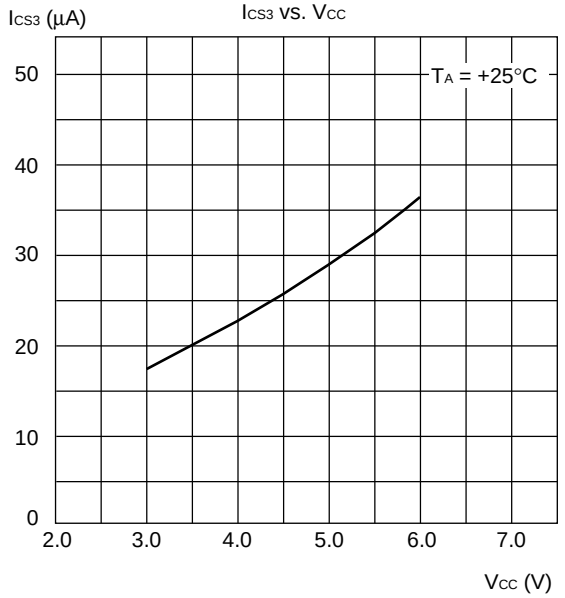
I_{CS1} vs. V_{CC}, I_{CS2} vs. V_{CC}



I_{CSB} vs. V_{CC}



I_{CS3} vs. V_{CC}



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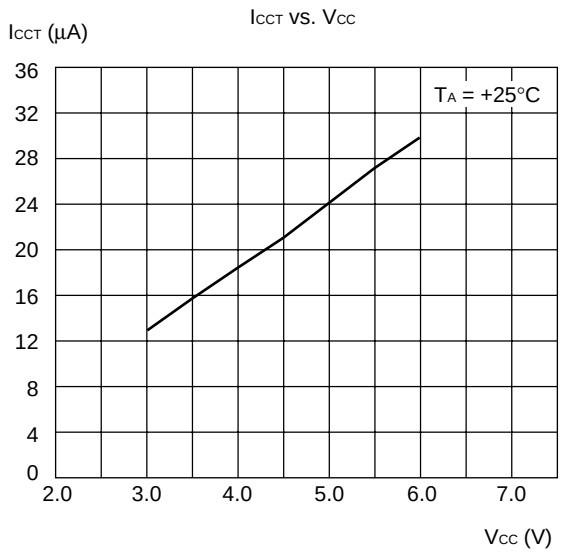
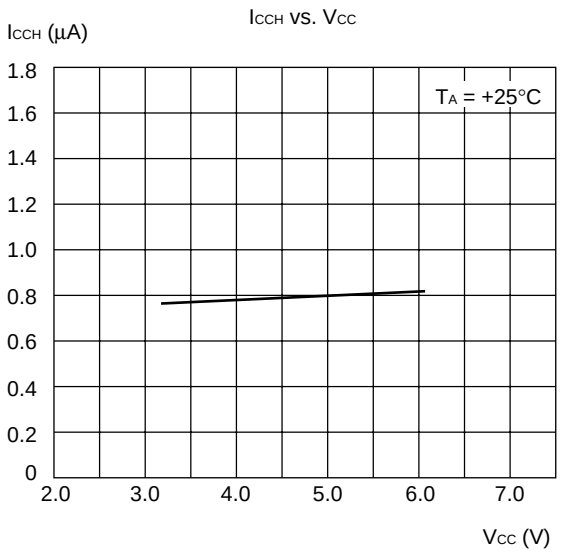
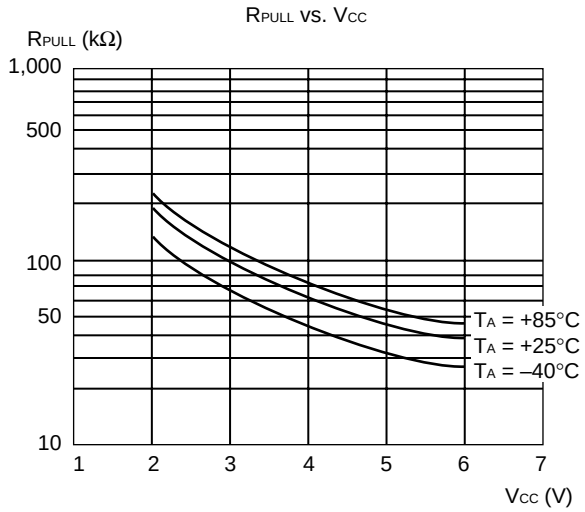




(5) Pull-up Resistance



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

(Continued)

Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR @A,IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

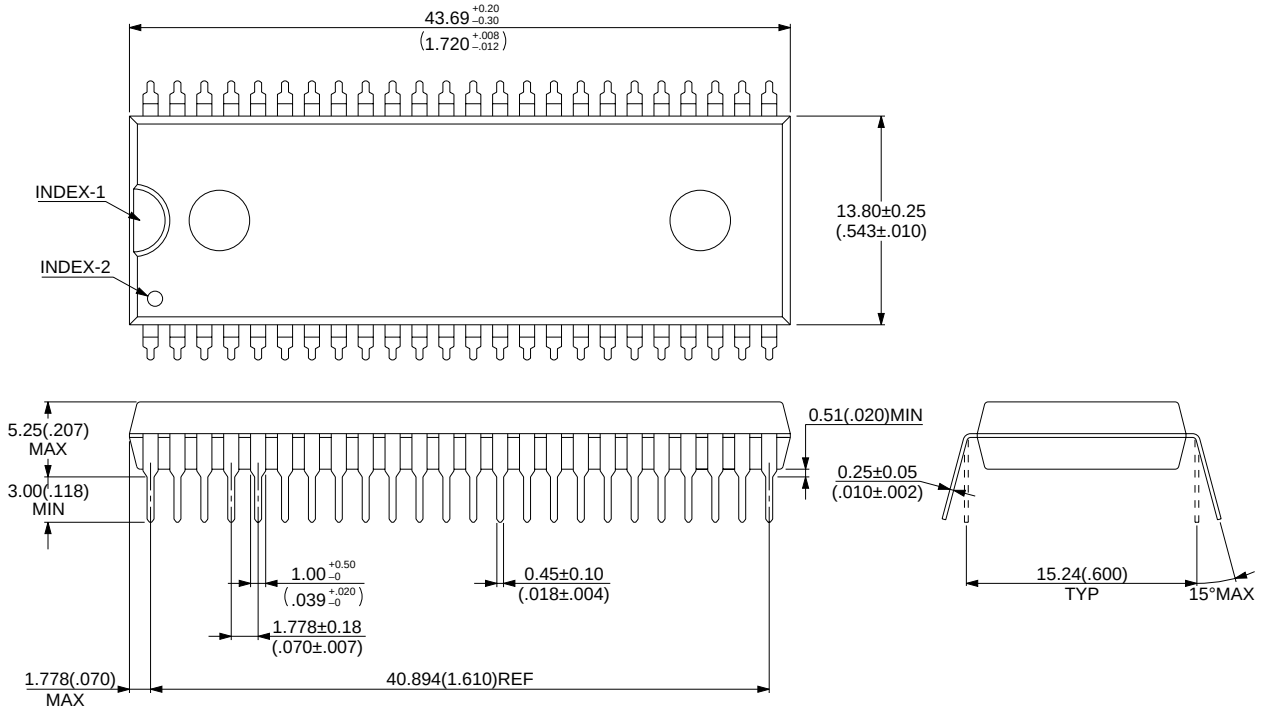
No.	Part number	MB89PV910		MB89913 MB89915	MB89P915	
		–101	–102		–101	–102
	Specifying procedure	Setting not possible	Setting not possible	Specify when ordering masking	Setting not possible	Setting not possible
1	Selection either single or dual clock Single-clock mode Dual-clock mode	Single clock	Dual clock	Selectable	Single clock	Dual clock
2	Pull-down resistors P17 to P10 P27 to P20 P51, P50	All pins fixed to without pull-down resistor		Can be selected per pin.	All pins fixed to without pull-down resistor	
3	Voltage to be detected for low-voltage detection reset 3.3 ± 0.3 V 3.6 ± 0.3 V 4.0 ± 0.3 V	Cannot be used.		Selectable	Can be set by register.	

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89913P-SH MB89915P-SH MB89P915P-101-SH MB89P915P-102-SH	48-pin Plastic SH-DIP (DIP-48P-M01)	
MB89913PF MB89915PF MB89P915PF-101 MB89P915PF-102	48-pin Plastic QFP (FPT-48P-M15)	
MB89PV910C-101-ES-SH MB89PV910C-102-ES-SH	64-pin Ceramic MDIP (MDP-64C-P02)	

■ PACKAGE DIMENSIONS

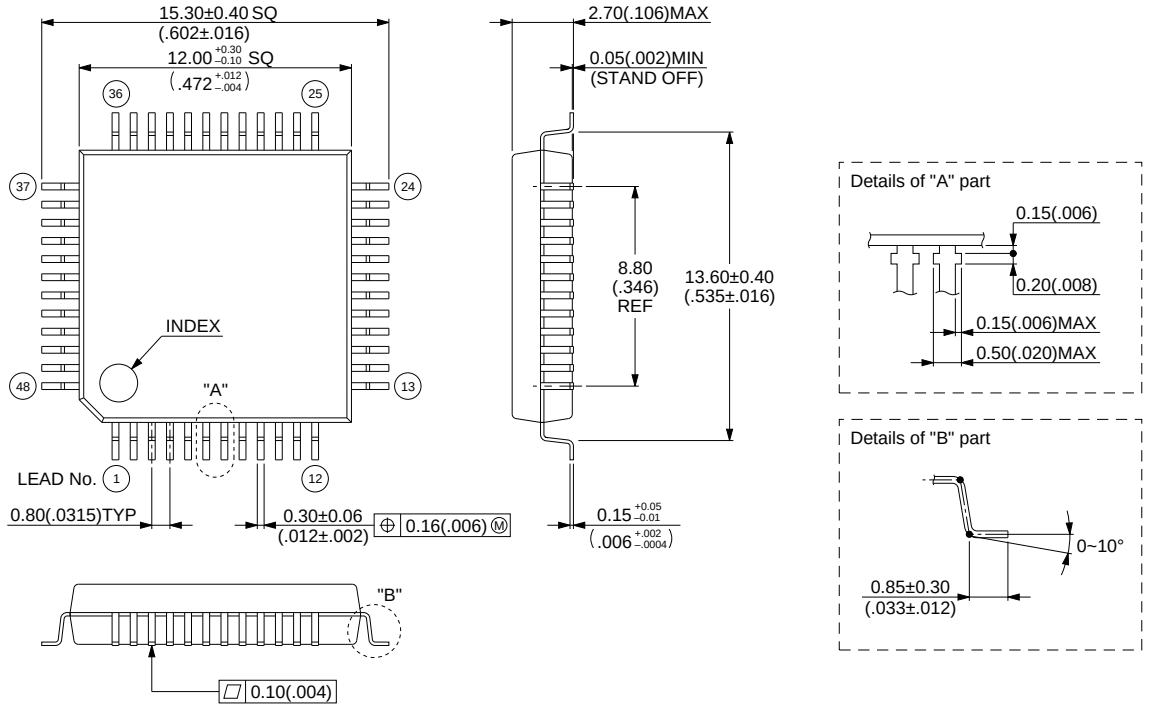
48-pin Plastic SH-DIP
(DIP-48P-M01)



Dimensions in mm (inches)

(Continued)

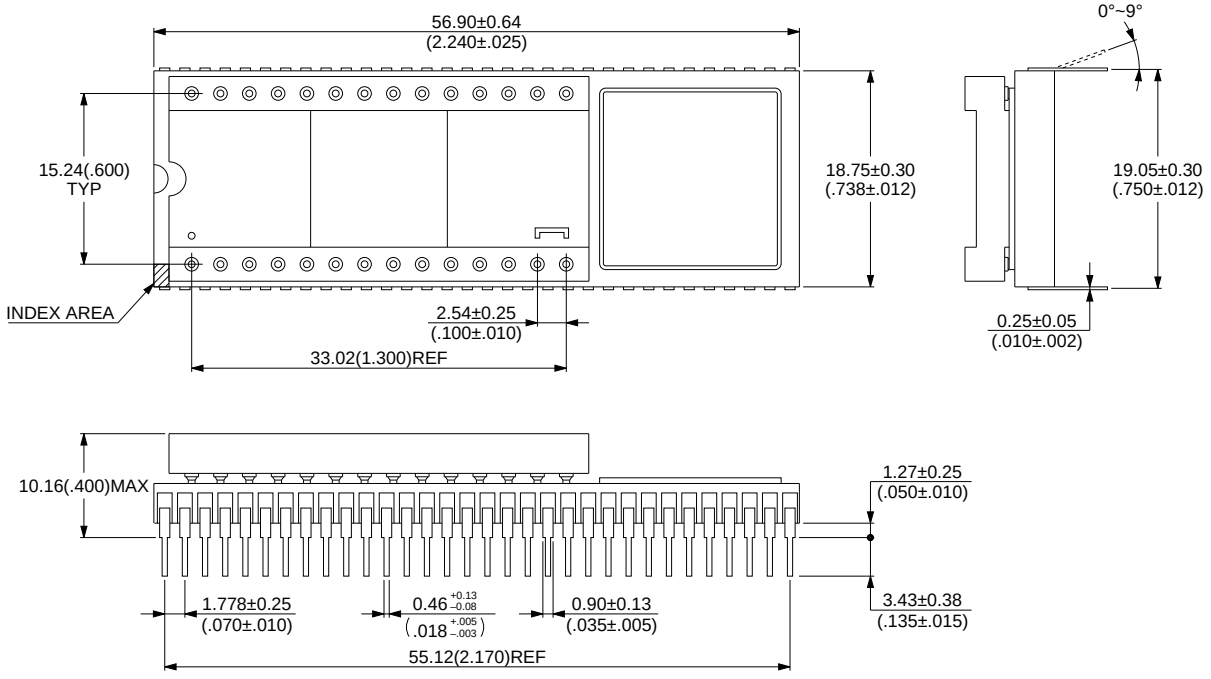
48-pin Plastic QFP
(FPT-48P-M15)



Dimensions in mm (inches)

(Continued)

64-pin Ceramic MDIP
(MDP-64C-P02)



Dimensions in mm (inches)

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