FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-12404-2E

8-bit Proprietary Microcontroller

CMOS

F²MC-8L MB89180 Series

MB89181/182/183/P185/PV180

■ DESCRIPTION

The MB89180 series has been developed as a general-purpose version of the F²MC*-8L family consisting of proprietary 8-bit, single-chip microcontrollers.

In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions such as dual-clock control system, five operating speed control stages, timers, a serial interface, a remote control transmission output, external interrupts, an LCD controller/driver, and a watch prescaler.

*: F²MC stands for FUJITSU Flexible Microcontroller.

■ FEATURES

- F²MC-8L family CPU core
- Dual-clock control system
- High speed operation at low voltage
- Minimum execution time: 0.95 µs/2.7 V, 1.33 µs/2.2 V
- I/O ports: max. 64 channels
- 21-bit time-base timer
- 8/16-bit timer/counter: 1 channel (8 bits × 2 channels)
- 8-bit serial I/O: 1 channel
- LCD controller/driver: max. 32 segments outputs × 4 commons

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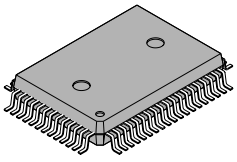
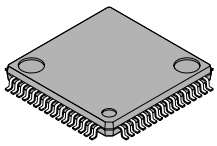
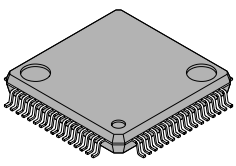
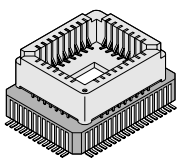
■ PACKAGE

64-pin Plastic QFP	64-pin Plastic QFP	64-pin Plastic SQFP	64-pin Ceramic MQFP
			
(FPT-64P-M06)	(FPT-64P-M09)	(FPT-64P-M03)	(MQP-64C-P01)

(Continued)

- Remote control transmission output
- Buzzer output
- Watch prescaler (15 bits)
- External interrupts (wake-up function)
  Four independent channels with edge detection function plus eight “L” level-interrupt channels

■ PRODUCT LINEUP

Parameter \ Part number	MB89181	MB89182	MB89183	MB89P185	MB89PV180
Classification	Mass production products (mask ROM products)			One-time PROM product	Piggyback/ evaluation product (for evaluation and development)
ROM size	4 K × 8 bits (internal mask ROM)	6 K × 8 bits (internal mask ROM)	8 K × 8 bits (internal mask ROM)	16K × 8 bits (internal PROM, programming with general-purpose EPROM programmer)	32 K × 8 bits (external ROM)
RAM size	128 × 8 bits	256 × 8 bits			512 × 8 bits
CPU functions	Number of instructions: 136 Instruction bit length: 8 bits Instruction length: 1 to 3 bytes Data bit length: 1, 8, 16 bits Minimum execution time: 0.95 µs/4.2 MHz Interrupt processing time: 8.57 µs/4.2 MHz				
Ports	I/O ports (N-ch open drain): 8 (6 ports also serve as peripherals, and 3 ports are a heavy-current drive type.) Output ports (N-ch open drain): 18 (16 ports also serve as segment pins*1, and 2 ports serve as booster capacitor connection pins.) I/O ports (CMOS): 16 (12 ports also serve as an external interrupt, and 8 ports also serve as segment pins*1.) Output port (CMOS): 1 (also serves as a remote control pin.) Total: 43 (max.)				
8/16-bit timer/ counter	8-bit timer/counter × 2 channels or 16-bit event counter × 1 channel				
8-bit serial I/O	8 bits LSB first/MSB first selectability				
LDC controller/driver	Common output: 4 (COM2 and COM3 also serve as output ports.) Segment output: 32 (max.)*1 Bias power supply pins: 3 LCD display RAM size: 32 × 4 bits Dividing resistor for LCD driving (external resistor selectability)				
External interrupt (wake-up function)	4 channels (edge selection, also serve as segment pins.)*1 8 channels (only for a level interrupt)				

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Part number / Parameter	MB89181	MB89182	MB89183	MB89P185	MB89PV180
Buzzer output	1 (7 frequency types are selectable by software.)				
Remote control transmission output	1 (pulse width and cycle are selectable by software.)				
Standby mode	Sleep mode, stop mode, and watch mode				
Process	CMOS				
Operating voltage*2	2.2 V*3 to 6.0 V			2.7 V to 6.0 V	
EPROM for use	—				MBM27C256A-20TV (LCC package)

*1: Selected by the mask option. See section "■ Mask Options."
*2: Varies with conditions such as the operating frequency and the connected ICE. (See section "■ Electrical Characteristics.")
*3: The operation at less than 2.2 V is assured separately. Please contact FUJITSU LIMITED.

■ PACKAGE AND CORRESPONDING PRODUCTS

Package	MB89181 MB89182 MB89183	MB89P185	MB89PV180
FPT-64P-M06	○	○	×
FPT-64P-M09	○	○	×
FPT-64P-M03	○	×	×
MQP-64C-P01	×	×	○

○ : Available × : Not available

Note: For more information about each package, see section "■ Package Dimensions."

■ DIFFERENCES AMONG PRODUCTS

1. Memory Size

Before evaluating using the piggyback product, verify its differences from the product that will actually be used. Take particular care on the following points:

- On the MB89181, addresses 0140_H and later of the register bank cannot be used. On the MB89182, MB89183, and MB89P185 microcontrollers, addresses 0180_H and later of the register bank cannot be used.
- On the MB89P185, addresses $BFF0_H$ to $BFF5_H$ comprise the option setting area, option settings can be read by reading these addresses.
- The stack area, etc., is set at the upper limit of the RAM.

2. Current Consumption

- In the case of the MB89PV180, add the current consumed by the EPROM which is connected to the top socket.
- When operated at low speed, the product with an OTPROM (one-time PROM) or an EPROM will consume more current than the product with a mask ROM.

  However, the current consumption in sleep/stop modes is the same. (For more information, see section "■ Electrical Characteristics.")

3. Mask Options

Functions that can be selected as options and how to designate these options vary by the product.

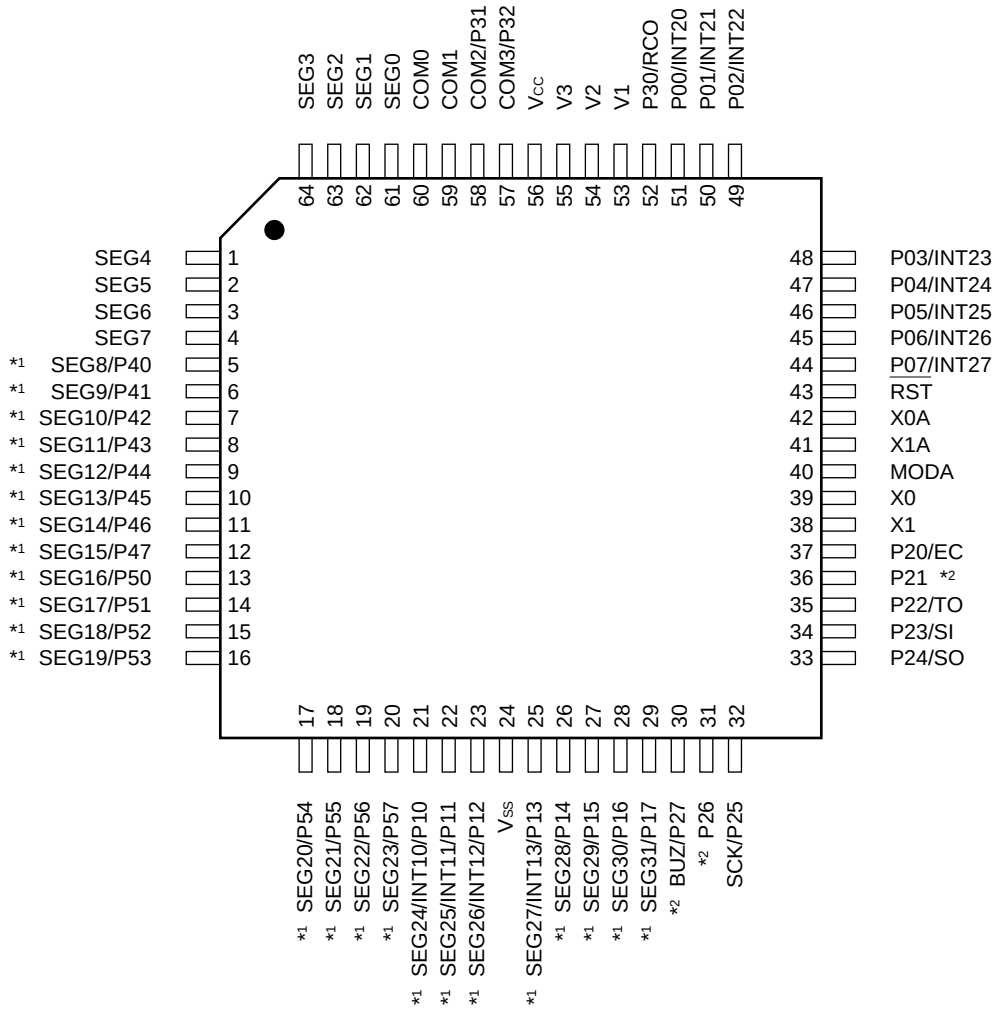
Before using options check section "■ Mask Options."

Take particular care on the following point:

- Options are fixed on the MB89PV180 except the segment output selection.

■ PIN ASSIGNMENT

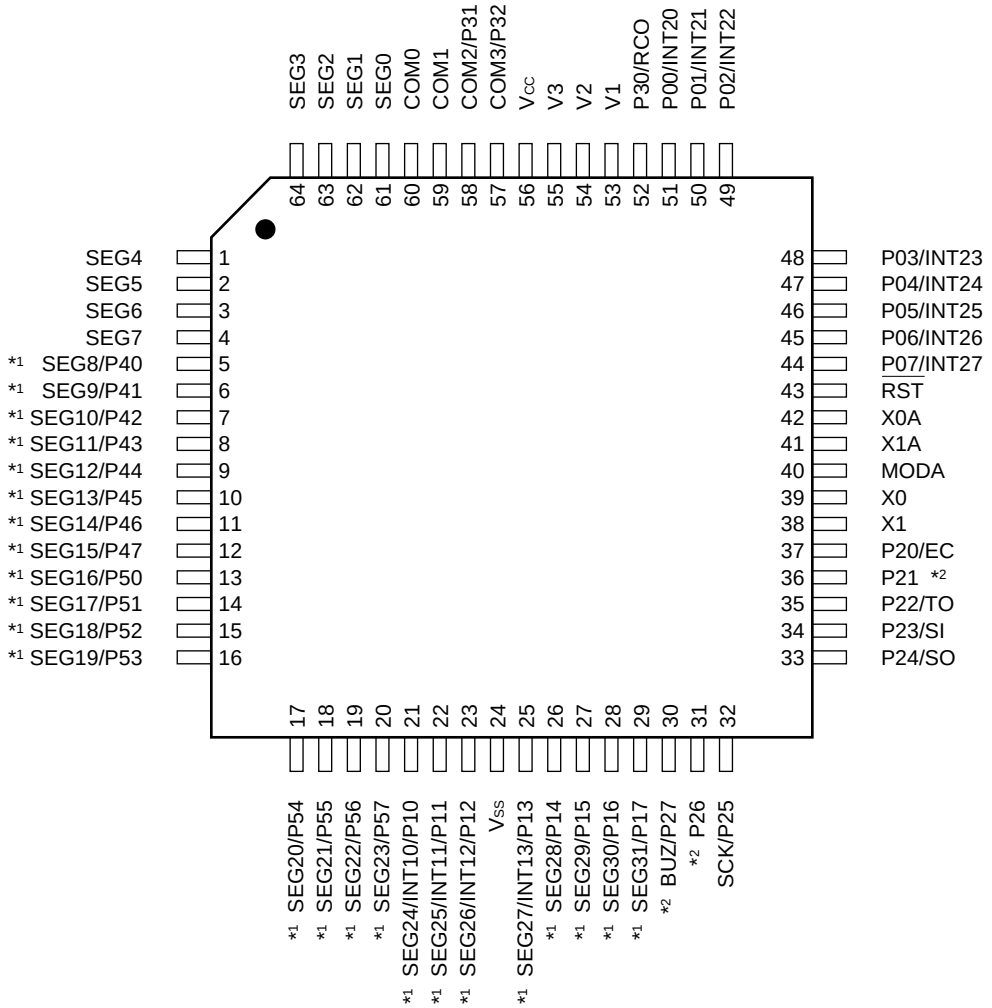
(Top view)



(FPT-64P-M03)

*1: Selected using the mask option (in units of 4 pins).
*2: N-ch open drain heavy-current drive type

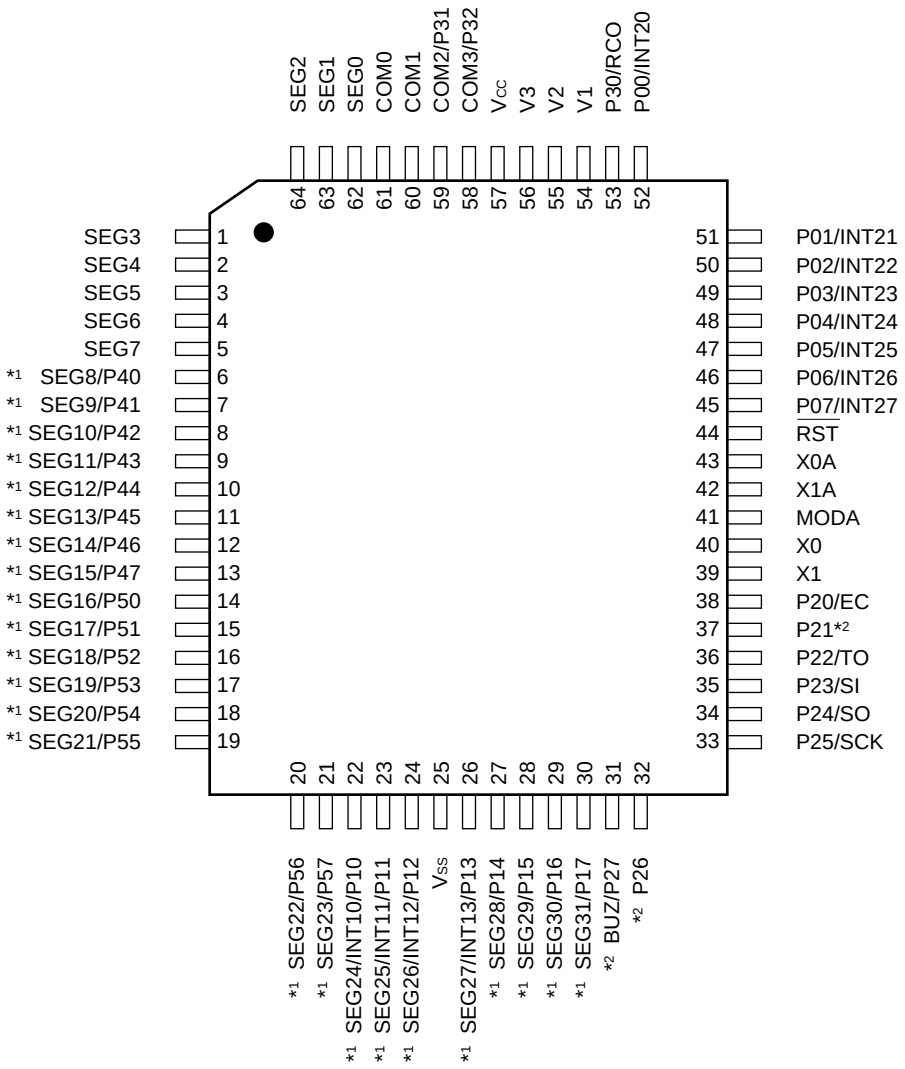
(Top view)



(FPT-64P-M09)

*1: Selected using the mask option (in units of 4 pins).
*2: N-ch open drain heavy-current drive type

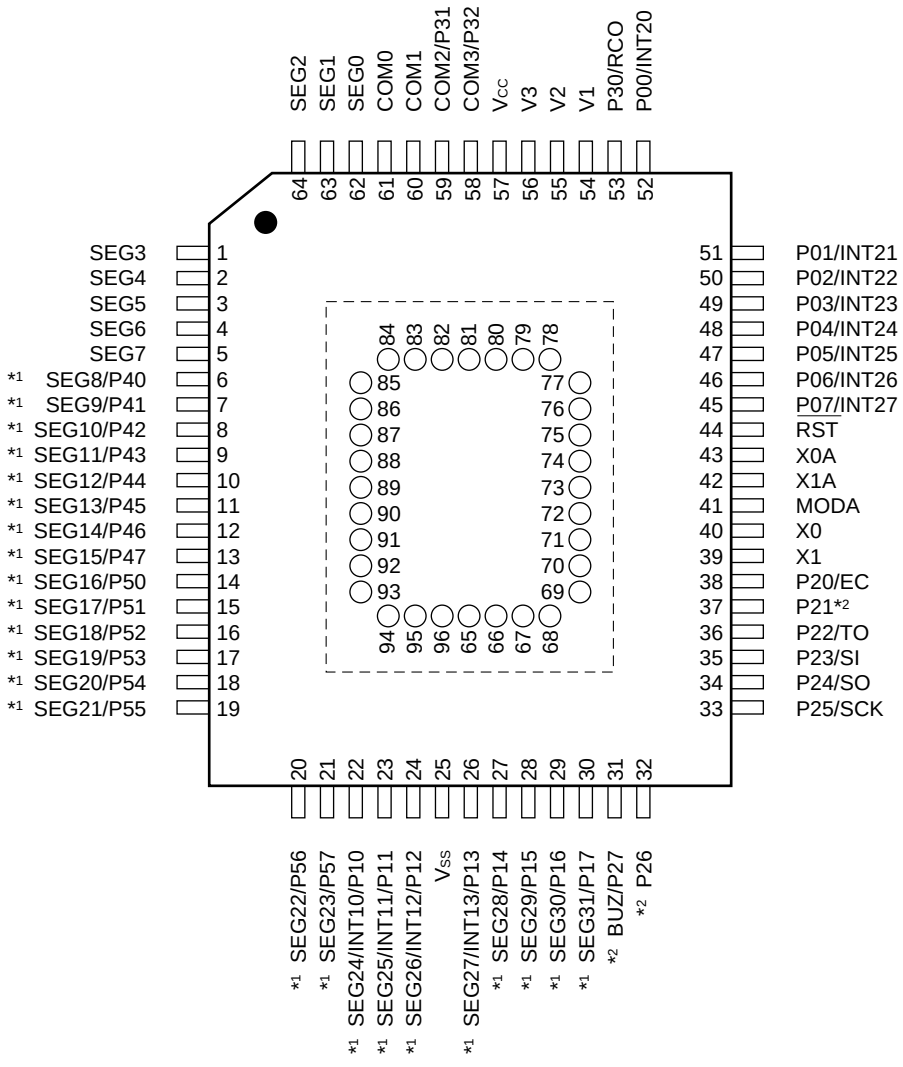
(Top view)



(FPT-64P-M06)

*1: Selected using the mask option (in units of 4 pins).
*2: N-ch open drain heavy-current drive type

(Top view)



(MQP-64C-P01)

*1: Selected using the mask option (in units of 4 pins).
*2: N-ch open drain heavy-current drive type

- **Pin assignment on package top (MB89PV180 only)**

Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name	Pin no.	Pin name
65	N.C.	73	A2	81	N.C.	89	$\overline{OE}$
66	V_{PP}	74	A1	82	O4	90	N.C.
67	A12	75	A0	83	O5	91	A11
68	A7	76	N.C.	84	O6	92	A9
69	A6	77	O1	85	O7	93	A8
70	A5	78	O2	86	O8	94	A13
71	A4	79	O3	87	$\overline{CE}$	95	A14
72	A3	80	V_{SS}	88	A10	96	V_{CC}

N.C.: Internally connected. Do not use.

■ PIN DESCRIPTION

Pin no.		Pin name	Circuit type	Function
QFP*1 SQFP*3	QFP*2 MQFP*4			
39	40	X0	A	Main clock crystal oscillator pins CR oscillation selectability (only for the mask ROM products)
38	39	X1		
40	41	MODA	C	Operating mode selection pin Connect directly to V_{SS}.
43	44	$\overline{RST}$	D	Reset I/O pin This pin is an N-ch open drain output type with a pull-up resistor, and hysteresis input type. “L” is output from this pin by an internal reset source. The internal circuit is initialized by the input of “L”.
44 to 51	45 to 52	P07/INT27 to P00/INT20	E	General-purpose I/O ports Also serve as external interrupt 2 input (wake-up function). External interrupt 2 input is hysteresis input.
21 to 23	22 to 24	P10/INT10/ SEG24 to P12/INT12/ SEG26	E/K	General-purpose I/O ports Also serve as external interrupt 1 input. The interrupt 1 input is a hysteresis type. Also serve as LCD controller/driver segment output. Switching is done by the mask option.
25	26	P13/INT13/ SEG27		
26 to 29	27 to 30	P14/SEG28 to P17/SEG31	F/K	General-purpose I/O ports Also serve as LCD controller/driver segment output. Switching is done by the mask option.
37	38	P20/EC	H	General-purpose N-ch open-drain I/O port Also serves as the external clock input for the 8-bit timer counter. The resource is a hysteresis input type.
36	37	P21	I	General-purpose N-ch open-drain I/O port
35	36	P22/TO	I	General-purpose N-ch open-drain I/O port Also serves as the 8-bit timer/counter output
34	35	P23/SI	H	General-purpose N-ch open-drain I/O port Also serves as the data input for the 8-bit serial I/O. The resource is a hysteresis input type.
33	34	P24/SO	I	General-purpose N-ch open-drain I/O port Also serves as the data output for the 8-bit serial I/O.
32	33	P25/SCK	H	General-purpose N-ch open-drain I/O port Also serves as the clock I/O for the 8-bit serial I/O. The resource is a hysteresis input type.

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*1: FPT-64P-M09
*2: FPT-64P-M06
*3: FPT-64P-M03
*4: MQP-64C-P01

(Continued)

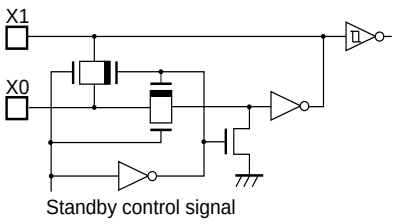
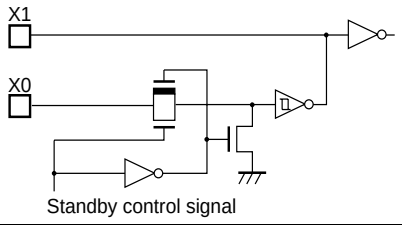
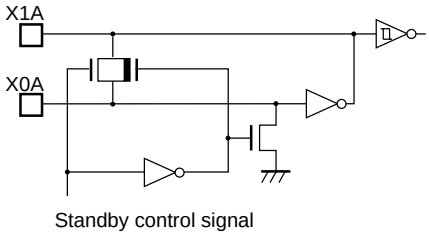
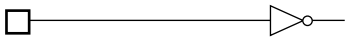
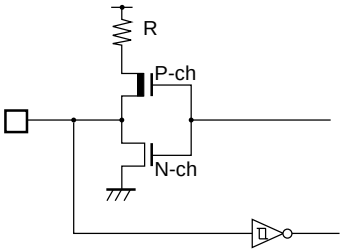
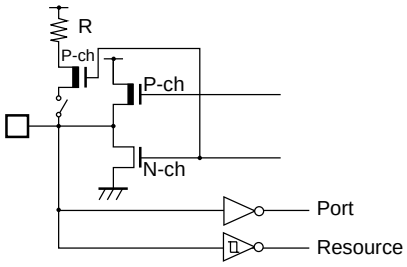
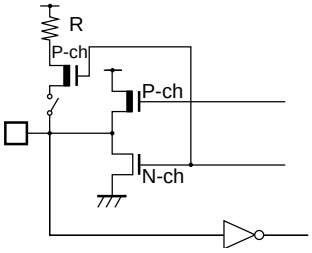
Pin no.		Pin name	Circuit type	Function
QFP*1 SQFP*3	QFP*2 MQFP*4			
31	32	P26	I	General-purpose N-ch open-drain I/O port
30	31	P27/BUZ	I	General-purpose N-ch open-drain I/O port Also serves as a buzzer output.
52	53	P30/RCO	G	General-purpose output-only port Also serves as a remote control transmission output pin.
13 to 20	14 to 21	P50/SEG16 to P57/SEG23	J/K	N-ch open-drain type general-purpose output ports Also serve as LCD controller/driver segment output pins. Switching is done by the mask option.
5 to 12	6 to 13	P40/SEG8 to P47/SEG15	J/K	
61 to 64, 1 to 4	62 to 64, 1 to 5	SEG7 to SEG0	K	LCD controller/driver segment output-only pins
57, 58	58, 59	COM3/P32, COM2/P31	L	N-ch open-drain type general-purpose output ports Also serve as LCD controller/driver common output pins.
59, 60	60, 61	COM1, COM0	K	LCD controller/driver common output-only pins
53, 54, 55	54, 55, 56	V1, V2, V3	—	LCD driving power supply pins
42	43	X0A	B	Subclock crystal oscillator pins (32.768 kHz)
41	42	X1A		
56	57	V_{CC}	—	Power supply pin
24	25	V_{SS}	—	Power supply (GND) pin

*1: FPT-64P-M09
*2: FPT-64P-M06
*3: FPT-64P-M03
*4: MQP-64C-P01

- **External EPROM pins (MB89PV180 only)**

Pin no.	Pin name	I/O	Function
66	V_{PP}	O	“H” level output pin
67 68 69 70 71 72 73 74 75	A12 A7 A6 A5 A4 A3 A2 A1 A0	O	Address output pins
77 78 79	O1 O2 O3	I	Data input pins
80	V_{SS}	O	Power supply (GND) pin
82 83 84 85 86	O4 O5 O6 O7 O8	I	Data input pins
87	$\overline{CE}$	O	ROM chip enable pin Outputs “H” during standby.
88	A10	O	Address output pin
89	$\overline{OE}$	O	ROM output enable pin Outputs “L” at all times.
91 92 93	A11 A9 A8	O	Address output pins
94	A13	O	
95	A14	O	
96	V_{CC}	O	EPROM power supply pin
65 76 81 90	N.C.	—	Internally connected pins Be sure to leave them open.

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• Crystal or ceramic oscillation type (main clock) At an oscillation feedback resistor of approximately 1 MΩ/5.0 V
		• CR oscillation type (main clock) (Selectable only for the MB89181/182/183)
B		• Crystal or ceramic oscillation type (subclock) • At an oscillation feedback resistor of approximately 4.5 MΩ/5.0 V
C		
D		• Output pull-up resistor • P-ch of approximately 50 KΩ/5.0 V • Hysteresis input
E		• CMOS I/O The resource is a hysteresis input type. • Pull-up resistor optional (MB89181/182/183/P185)
F		• CMOS I/O • Pull-up resistor optional (MB89181/182/183/P185)

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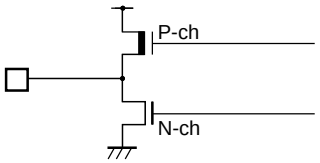
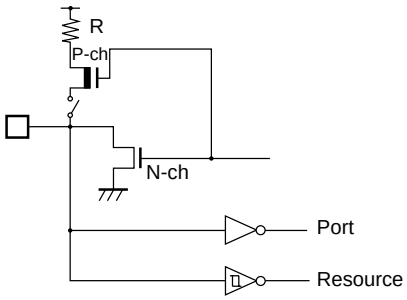
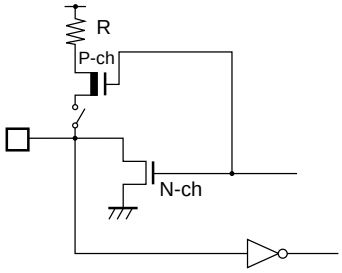
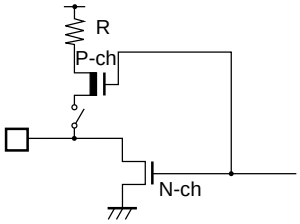
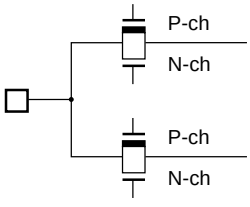
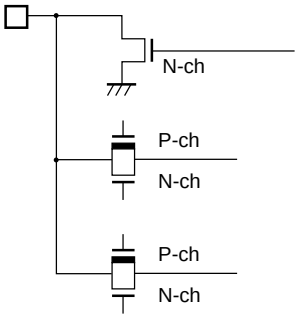
Type	Circuit	Remarks
G		• CMOS output • The P-ch output is a heavy-current drive type.
H		• N-ch open-drain I/O • CMOS input • The resource is a hysteresis input type. • Pull-up resistor optional (MB89181/182/183)
I		• N-ch open-drain I/O • CMOS input • P21, P26, and P27 are a heavy-current drive type. • Pull-up resistor optional (MB89181/182/183)
J		• N-ch open-drain output • Pull-up resistor optional (MB89181/182/183)
K		• LCD controller/driver segment output
L		• N-ch open-drain output • Common output

■ HANDLING DEVICES

1. Preventing Latchup

Latchup may occur on CMOS ICs if voltage higher than V_{CC} or lower than V_{SS} is applied to input and output pins other than medium- to high-voltage pins or if higher than the voltage which shows on “1. Absolute Maximum Ratings” in section “■ Electrical Characteristics” is applied between V_{CC} and V_{SS}.

When latchup occurs, power supply current increases rapidly and might thermally damage elements. When using, take great care not to exceed the absolute maximum ratings.

Also, take care to prevent the analog power supply (AV_{CC} and AVR) and analog input from exceeding the digital power supply (V_{CC}) when the analog system power supply is turned on and off.

2. Treatment of Unused Input Pins

Leaving unused input pins open could cause malfunctions. They should be connected to a pull-up or pull-down resistor.

3. Treatment of Power Supply Pins on Microcontrollers with A/D and D/A Converters

Connect to be AV_{CC} = DAVC = V_{CC} and AV_{SS} = AVR = V_{SS} even if the A/D and D/A converters are not in use.

4. Treatment of N.C. Pins

Be sure to leave (internally connected) N.C. pins open.

5. Power Supply Voltage Fluctuations

Although V_{CC} power supply voltage is assured to operate within the rated range, a rapid fluctuation of the voltage could cause malfunctions, even if it occurs within the rated range. Stabilizing voltage supplied to the IC is therefore important. As stabilization guidelines, it is recommended to control power so that V_{CC} ripple fluctuations (P-P value) will be less than 10% of the standard V_{CC} value at the commercial frequency (50 to 60 Hz) and the transient fluctuation rate will be less than 0.1 V/ms at the time of a momentary fluctuation such as when power is switched.

6. Precautions when Using an External Clock

Even when an external clock is used, oscillation stabilization time is required for power-on reset (optional) and wake-up from stop mode.

■ PROGRAMMING TO THE EPROM ON THE MB89P875

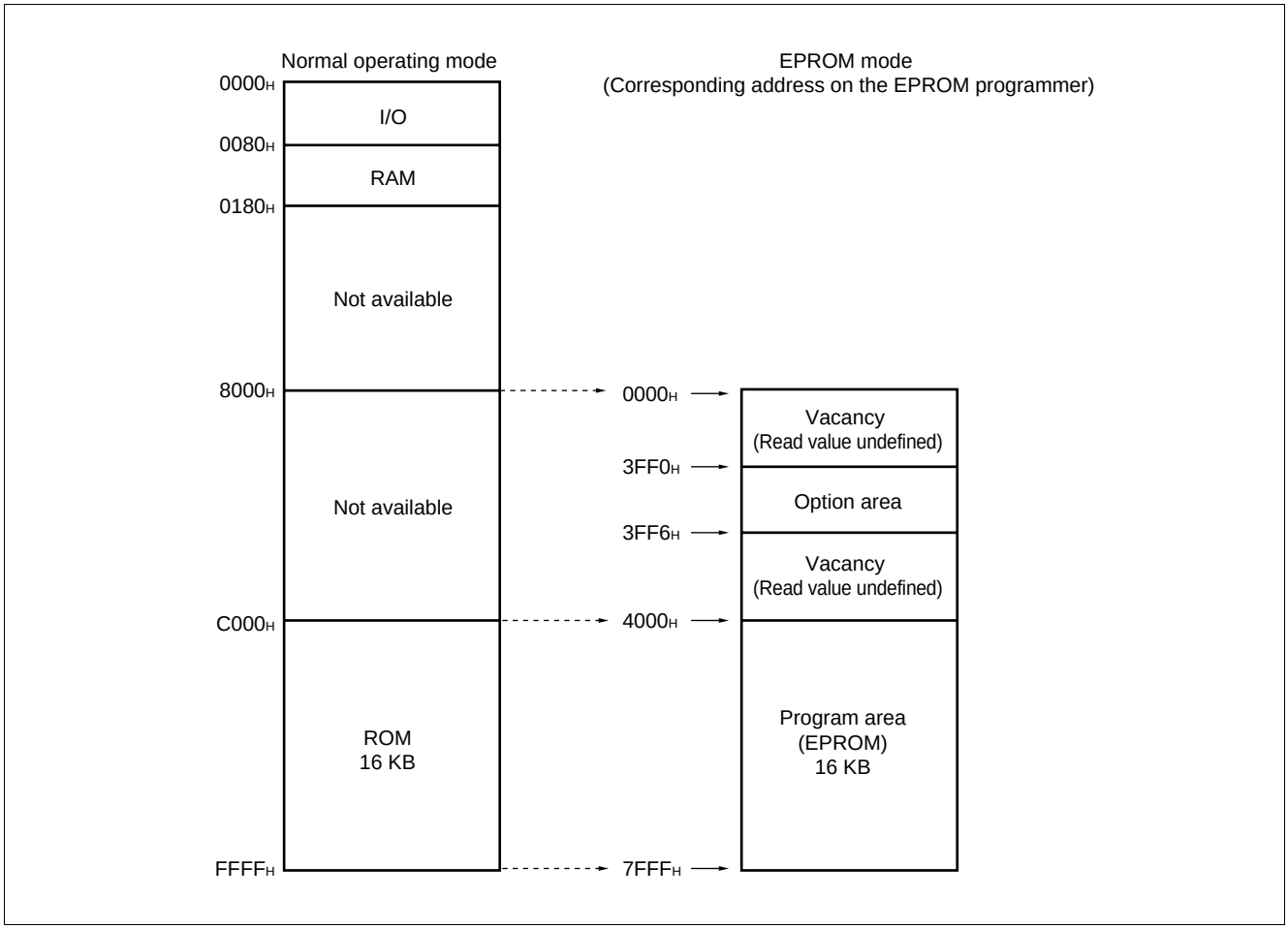
The MB89P185 is an OTPROM version of the MB89180 series.

1. Features

- 16-Kbyte PROM on chip
- Options can be set using the EPROM programmer.
- Equivalency to the MBM27C256A in EPROM mode (when programmed with the EPROM programmer)

2. Memory Space

Memory space in the EPROM mode is diagrammed below.



3. Programming to the EPROM

In EPROM mode, the MB89P185 functions equivalent to the MBM27C256A. This allows the PROM to be programmed with a general-purpose EPROM programmer (the electronic signature mode cannot be used) by using the dedicated socket adapter.

- **Programming procedure**

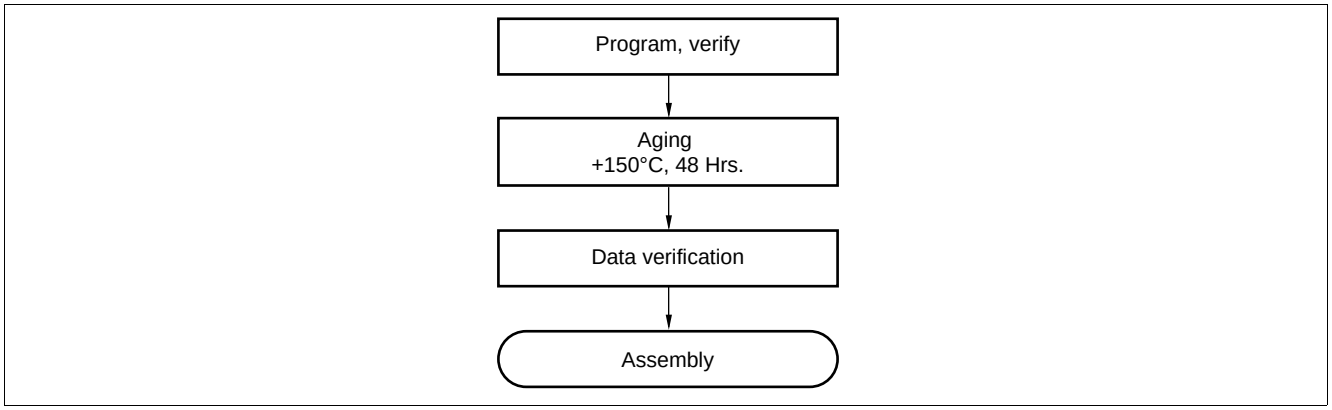
(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$ (note that addresses $C000_H$ to $FFFF_H$ in operating mode assign to 4000_H to $7FFF_H$ in EPROM mode).
Program to 4000_H to $7FFF_H$ with the EPROM programmer.

(3) Load option data into addresses $3FF0_H$ to $3FF5_H$ of the EPROM programmer. (For information about each corresponding option, see “7. PROM Option Bit Map.”)
Program to $3FF0_H$ to $3FF5_H$ with the EPROM programmer.

4. Recommended Screening Conditions

High-temperature aging is recommended as the pre-assembly screening procedure for a product with a blanked OTPROM microcomputer program.



5. Programming Yield

All bits cannot be programmed at Fujitsu shipping test to a blanked OTPROM microcomputer, due to its nature. For this reason, a programming yield of 100% cannot be assured at all times.

6. EPROM Programmer Socket Adapter

Package	Compatible socket adapter
FPT-64P-M09	ROM-64QF2-28DP-8L2
FPT-64P-M06	ROM-64QF-28DP-8L3

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

Note: Depending on the EPROM programmer, inserting a capacitor of about 0.1 µF between V_{PP} and V_{SS} or V_{CC} and V_{SS} can stabilize programming operations.

7. PROM Option Bit Map

The programming procedure is the same as that for the PROM. Options can be set by programming values at the addresses shown on the memory map. The relationship between bits and options is shown on the following bit map:

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
3FF0H	Vacancy Readable	Vacancy Readable	Oscillation stabilization delay time WTM1 See "■ Mask Options"	WTM0	Vacancy Readable	Reset pin output 1: Yes 0: No	Clock mode selection 1: Dual clock 0: Single clock	Power-on reset 1: Yes 0: No
3FF1H	P07 Pull-up 1: No 0: Yes	P06 Pull-up 1: No 0: Yes	P05 Pull-up 1: No 0: Yes	P04 Pull-up 1: No 0: Yes	P03 Pull-up 1: No 0: Yes	P02 Pull-up 1: No 0: Yes	P01 Pull-up 1: No 0: Yes	P00 Pull-up 1: No 0: Yes
3FF2H	P17 Pull-up 1: No 0: Yes	P16 Pull-up 1: No 0: Yes	P15 Pull-up 1: No 0: Yes	P14 Pull-up 1: No 0: Yes	P13 Pull-up 1: No 0: Yes	P12 Pull-up 1: No 0: Yes	P11 Pull-up 1: No 0: Yes	P10 Pull-up 1: No 0: Yes
3FF3H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
3FF4H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable
3FF5H	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable	Vacancy Readable

Notes:
- Set each bit to 1 to erase.
- Do not write 0 to the vacant bit.
  The read value of the vacant bit is 1, unless 0 is written to it.
- Address 3FF6H cannot be read and should not be accessed.

■ PROGRAMMING TO THE EPROM WITH PIGGYBACK/EVALUATION DEVICE

1. EPROM for Use

MBM27C256A-20TV

2. Programming Socket Adapter

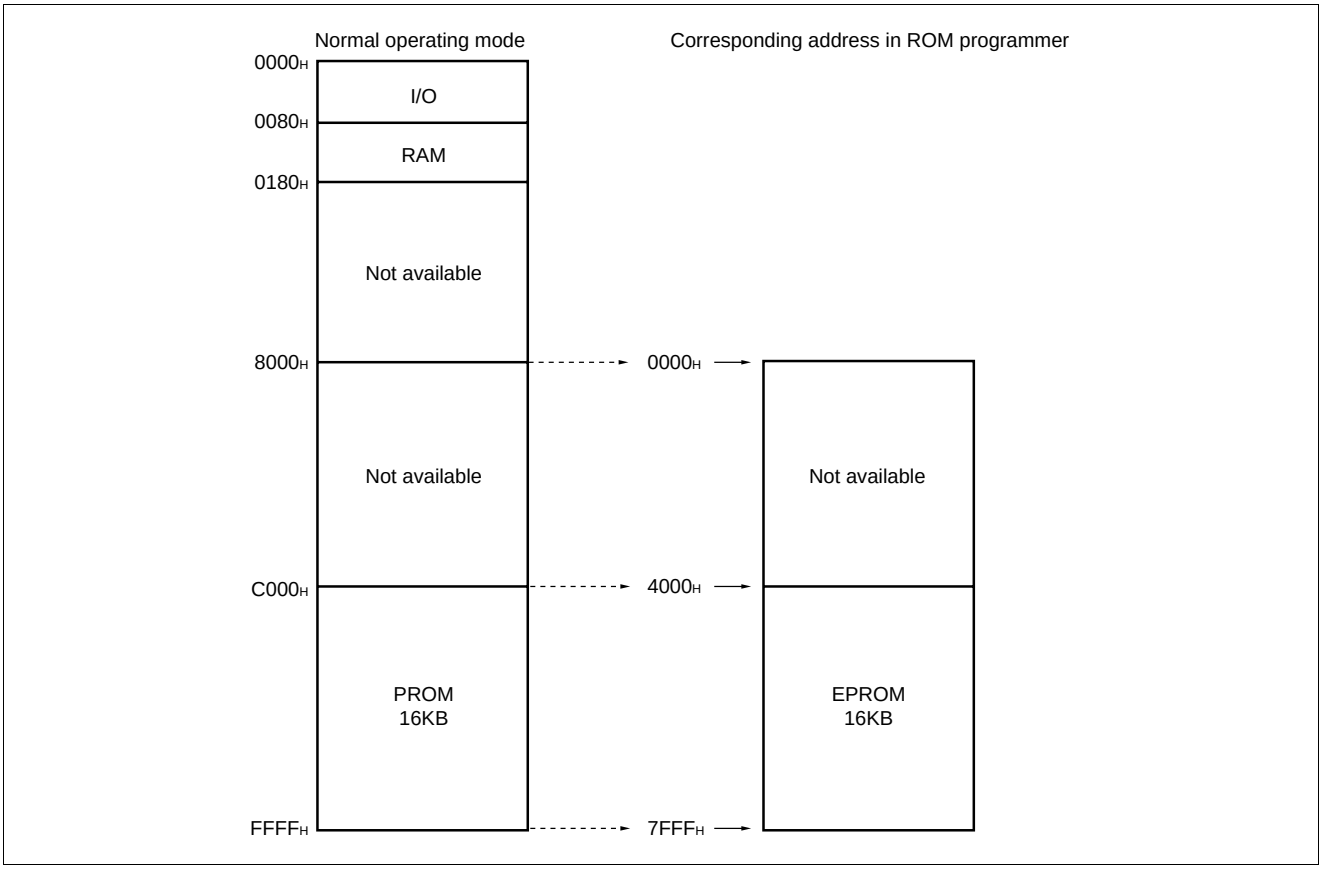
To program to the PROM using an EPROM programmer, use the socket adapter (manufacturer: Sun Hayato Co., Ltd.) listed below.

Package	Adapter socket part number
LCC-32(Rectangle)	ROM-32LC-28DP-YG
LCC-32(Square)	ROM-32LC-28DP-S

Inquiry: Sun Hayato Co., Ltd.: TEL 81-3-3802-5760

3. Memory Space

Memory space in each mode is diagrammed below.



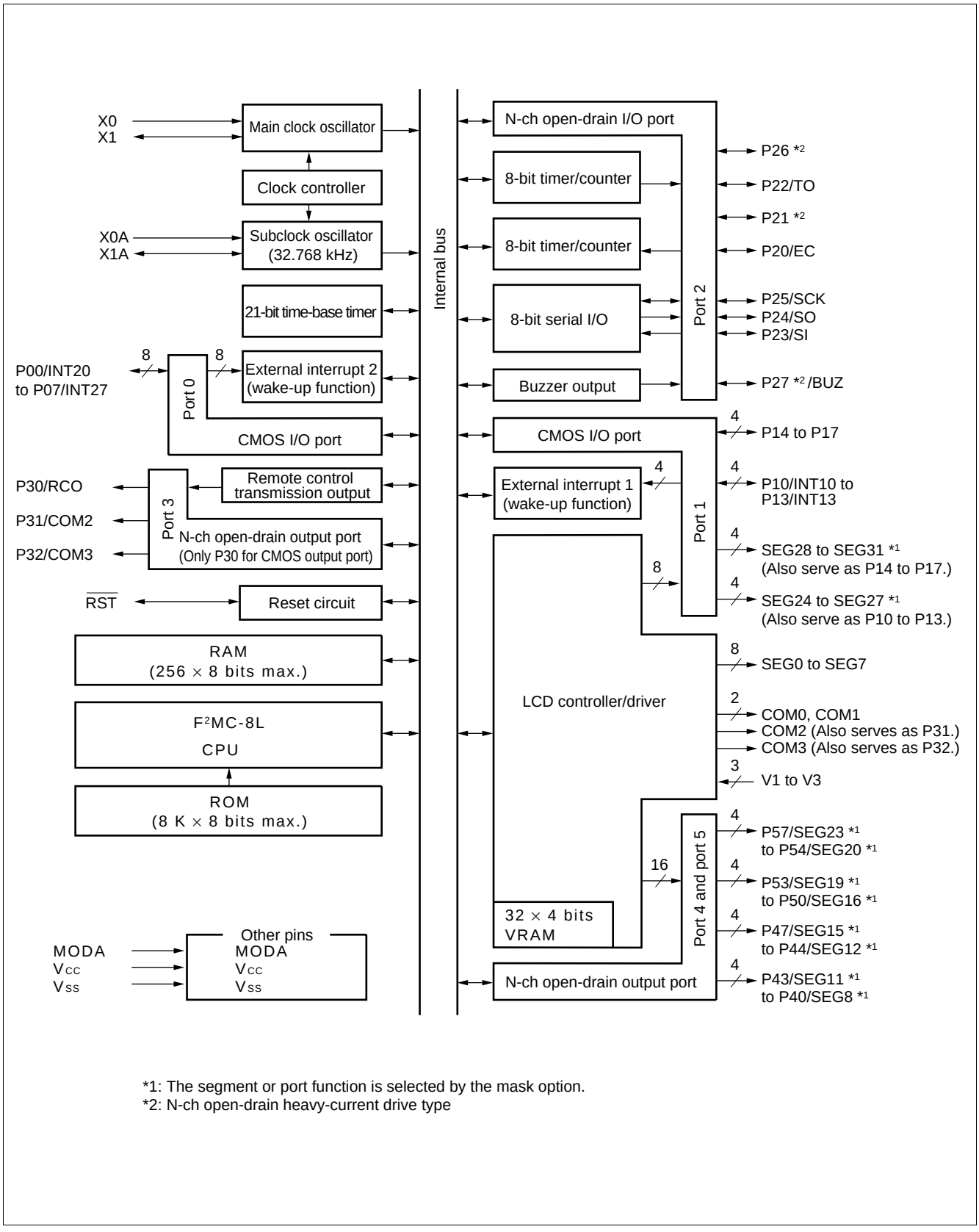
4. Programming to the EPROM

(1) Set the EPROM programmer to the MBM27C256A.

(2) Load program data into the EPROM programmer at 4000_H to $7FFF_H$.

(3) Program to 4000_H to $7FFF_H$ with the EPROM programmer.

■ BLOCK DIAGRAM



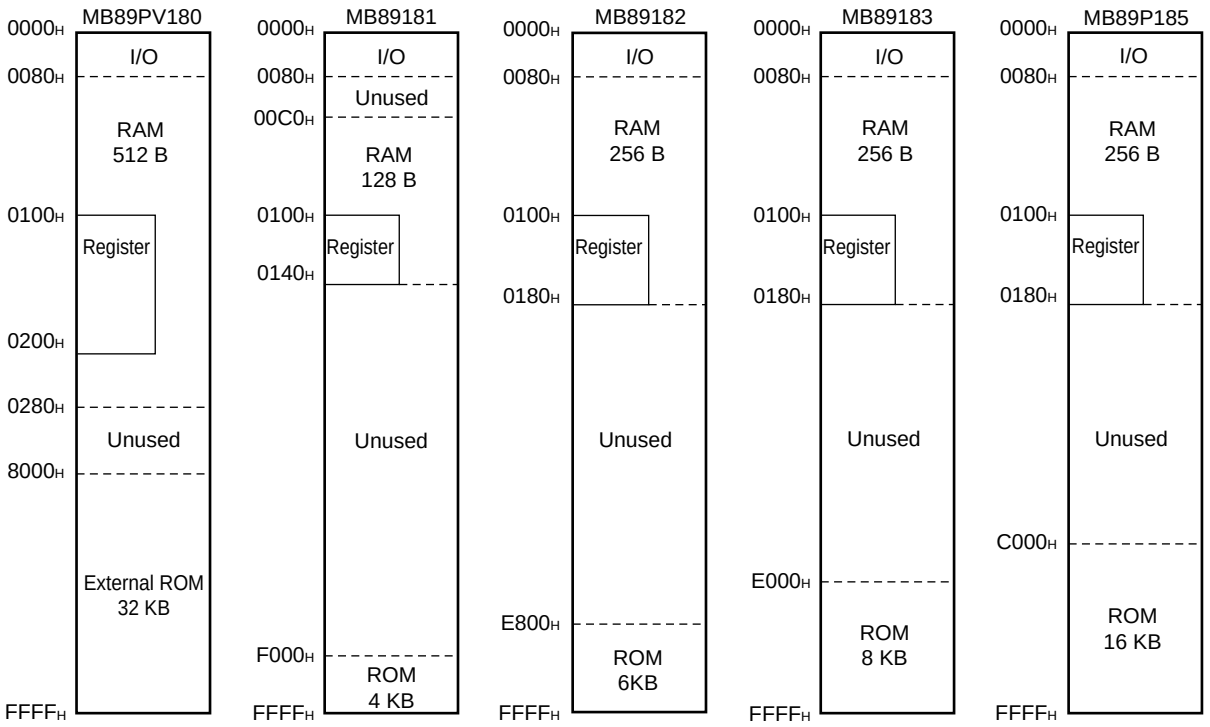
*1: The segment or port function is selected by the mask option.
*2: N-ch open-drain heavy-current drive type

■ CPU CORE

1. Memory Space

The microcontrollers of the MB89180 series offer a memory space of 64 Kbytes for storing all of I/O, data, and program areas. The I/O area is located at the lowest address. The data area is provided immediately above the I/O area. The data area can be divided into register, stack, and direct areas according to the application. The program area is located at exactly the opposite end, that is, near the highest address. Provide the tables of interrupt reset vectors and vector call instructions toward the highest address within the program area. The memory space of the MB89180 series is structured as illustrated below.

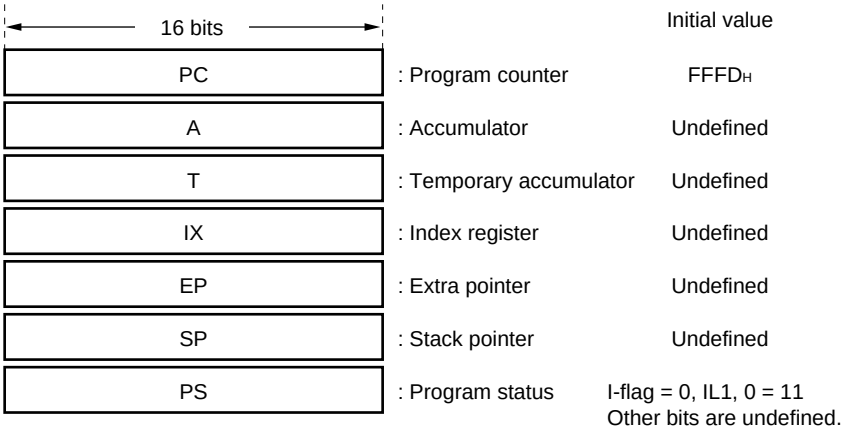
Memory Space



2. Registers

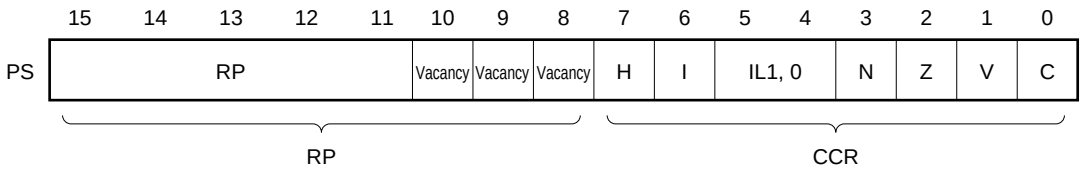
The F²MC-8L family has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The following dedicated registers are provided:

Program counter (PC):	A 16-bit register for indicating instruction storage positions
Accumulator (A):	A 16-bit temporary register for storing arithmetic operations, etc. When the instruction is an 8-bit data processing instruction, the lower byte is used.
Temporary accumulator (T):	A 16-bit register which performs arithmetic operations with the accumulator When the instruction is an 8-bit data processing instruction, the lower byte is used.
Index register (IX):	A 16-bit register for index modification
Extra pointer (EP):	A 16-bit pointer for indicating a memory address
Stack pointer (SP):	A 16-bit register for indicating a stack area
Program status (PS):	A 16-bit register for storing a register pointer, a condition code



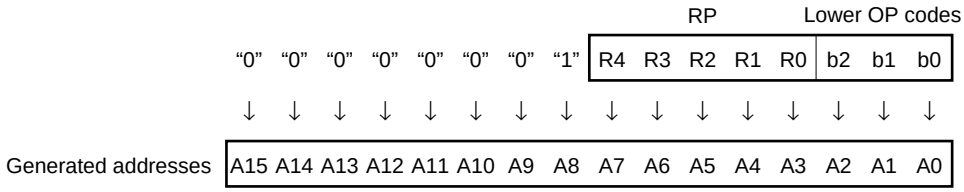
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

Structure of the Program Status Register



The RP indicates the address of the register bank currently in use. The relationship between the pointer contents and the actual address is based on the conversion rule illustrated below.

Rule for Conversion of Actual Addresses of the General-purpose Register Area



The CCR consists of bits indicating the results of arithmetic operations and the contents of transfer data and bits for control of CPU operations at the time of an interrupt.

H-flag: Set when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared otherwise. This flag is for decimal adjustment instructions.

I-flag: Interrupt is allowed when this flag is set to 1. Interrupt is prohibited when the flag is set to 0. Set to 0 when reset.

IL1, 0: Indicates the level of the interrupt currently allowed. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	High-low
0	0	1	High
0	1		
1	0	2	
1	1	3	Low = no interrupt

N-flag: Set if the MSB is set to 1 as the result of an arithmetic operation. Cleared when the bit is set to 0.

Z-flag: Set when an arithmetic operation results in 0. Cleared otherwise.

V-flag: Set if the complement on 2 overflows as a result of an arithmetic operation. Reset if the overflow does not occur.

C-flag: Set when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared otherwise. Set to the shift-out value in the case of a shift instruction.

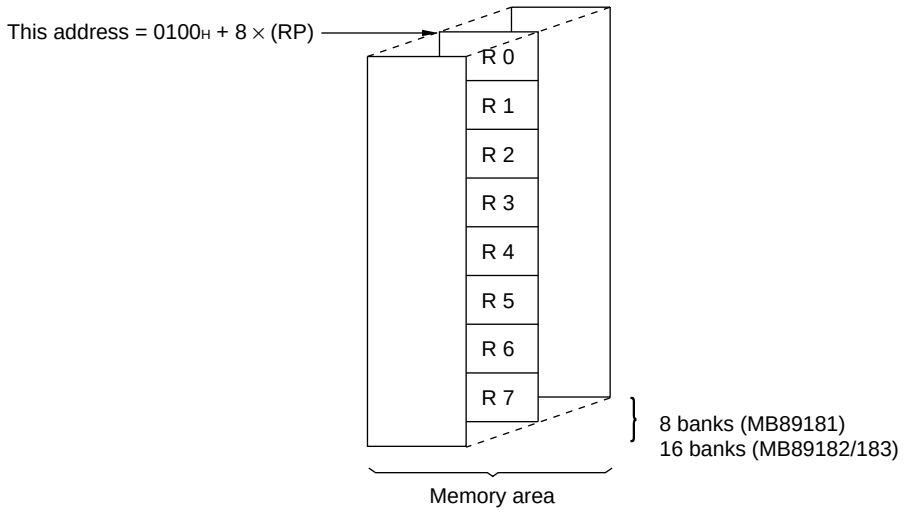
The following general-purpose registers are provided:

General-purpose registers: An 8-bit register for storing data

The general-purpose registers are 8 bits and located in the register banks of the memory. One bank contains eight registers. Up to a total of 8 banks can be used on the MB89181 (RAM 128 × 8 bits) and a total of 16 banks can be used on the MB89182/183 (RAM 256 × 8 bits). The bank currently in use is indicated by the register bank pointer (RP).

Note: The number of register banks that can be used varies with the RAM size.

Register Bank Configuration



■ I/O MAP

Address	Read/write	Register name	Register description
00_H	(R/W)	PDR0	Port 0 data register
01_H	(W)	DDR0	Port 0 data direction register
02_H	(R/W)	PDR1	Port 1 data register
03_H	(W)	DDR1	Port 1 data direction register
04_H	(R/W)	PDR2	Port 2 data register
05_H	(W)	DDR2	Port 2 data direction register
06_H			Vacancy
07_H	(R/W)	SYCC	System clock control register
08_H	(R/W)	STBC	Standby control register
09_H	(R/W)	WDTC	Watchdog timer control register
$0A_H$	(R/W)	TBTC	Time-base timer control register
$0B_H$	(R/W)	WPCR	Watch prescaler control register
$0C_H$	(R/W)	PDR3	Port 3 data register
$0D_H$			Vacancy
$0E_H$	(R/W)	PDR4	Port 4 data register
$0F_H$	(R/W)	PDR5	Port 5 data register
10_H	(R/W)	BZCR	Buzzer register
11_H			Vacancy
12_H			Vacancy
13_H			Vacancy
14_H	(R/W)	RCR1	Remote control transmission control register 1
15_H	(R/W)	RCR2	Remote control transmission control register 2
16_H			Vacancy
17_H			Vacancy
18_H	(R/W)	T2CR	Timer 2 control register
19_H	(R/W)	T1CR	Timer 1 control register
$1A_H$	(R/W)	T2DR	Timer 2 data register
$1B_H$	(R/W)	T1DR	Timer 1 data register
$1C_H$	(R/W)	SMR1	Serial mode register
$1D_H$	(R/W)	SDR1	Serial mode register
$1E_H$ to $2F_H$			Vacancy

(Continued)

(Continued)

Address	Read/write	Register name	Register description
30_H	(R/W)	EIE1	External interrupt 1 enable register
31_H	(R/W)	EIF1	External interrupt 1 flag register
32_H	(R/W)	EIE2	External interrupt 2 enable register
33_H	(R/W)	EIF2	External interrupt 2 flag register
34_H to $5F_H$			Vacancy
60_H to $6F_H$	(R/W)	VRAM	Display data RAM
70_H to 71_H			Vacancy
72_H	(R/W)	LCR1	LCD controller/driver control register 1
73_H to $7B_H$			Vacancy
$7C_H$	(W)	ILR1	Interrupt level setting register 1
$7D_H$	(W)	ILR2	Interrupt level setting register 2
$7E_H$	(W)	ILR3	Interrupt level setting register 3
$7F_H$			Vacancy

Note: Do not use vacancies.

■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 7.0	V	
LCD power supply voltage	V1 to V3	V_{SS} – 0.3	V_{SS} + 7.0	V	V1 to V3 must not exceed V_{CC}.
Input voltage	V_{I1}	V_{SS} – 0.3	V_{CC} + 0.3	V	V_{I1} must not exceed Vss + 7.0 V. Except P20 to P27 without a pull-up resistor
	V_{I2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P20 to P27 without a pull-up resistor
Output voltage	V_{O1}	V_{SS} – 0.3	V_{CC} + 0.3	V	V_{O1} must not exceed Vss + 7.0 V. Except P20 to P27, P40 to P47, and P50 to P57 without a pull-up resistor
	V_{O2}	V_{SS} – 0.3	V_{SS} + 7.0	V	P20 to P27, P40 to P47, and P50 to P57 without a pull-up resistor
“L” level output current	I_{OL1}	—	10	mA	Except P21, P26, P27, and power supply pins
	I_{OL2}	—	20	mA	P21, P26, and P27
“L” level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating rate) Except P21, P26, P27, and power supply pins
	I_{OLAV2}	—	8	mA	Average value (operating current × operating rate) P21, P26, and P27
“L” level total output current	$\sum I_{OL}$	—	80	mA	
“L” level total average output current	$\sum I_{OLAV}$	—	40	mA	Average value (operating current × operating rate)
“H” level output current	I_{OH1}	—	–5	mA	Except P30 and power supply pins
	I_{OH2}	—	–10	mA	P30

(Continued)

(Continued)

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
"H" level average output current	I_{OHAV1}	—	–2	mA	Average value (operating current × operating rate) Except P30 and power supply pins
	I_{OHAV2}	—	–4	mA	Average value (operating current × operating rate) P30
"H" level total output current	$\sum I_{OH}$	—	–20	mA	
"H" level total average output current	$\sum I_{OHAV}$	—	–10	mA	Average value (operating current × operating rate)
Power consumption	P_D	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

Precautions: Permanent device damage may occur if the above "Absolute Maximum Ratings" are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. Recommended Operating Conditions

(V_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	2.2*1	6.0	V	Guaranteed normal operation range, applicable to the mask ROM products
		2.7*1	6.0	V	MB89P185/PV180
		1.5	6.0	V	RAM data holding assurance range in stop mode
Power supply voltage for LCD	V1 to V3	V_{SS}	V_{CC}*2	V	V1 to V3 pins
Operating temperature	T_A	–40	+85	°C	

*1: The minimum operating power supply voltage varies with the operating frequency and execution time (instruction cycle).

*2: The liquid-crystal power supply range and optimum value vary depending on the characteristics of the liquid-crystal display element used.

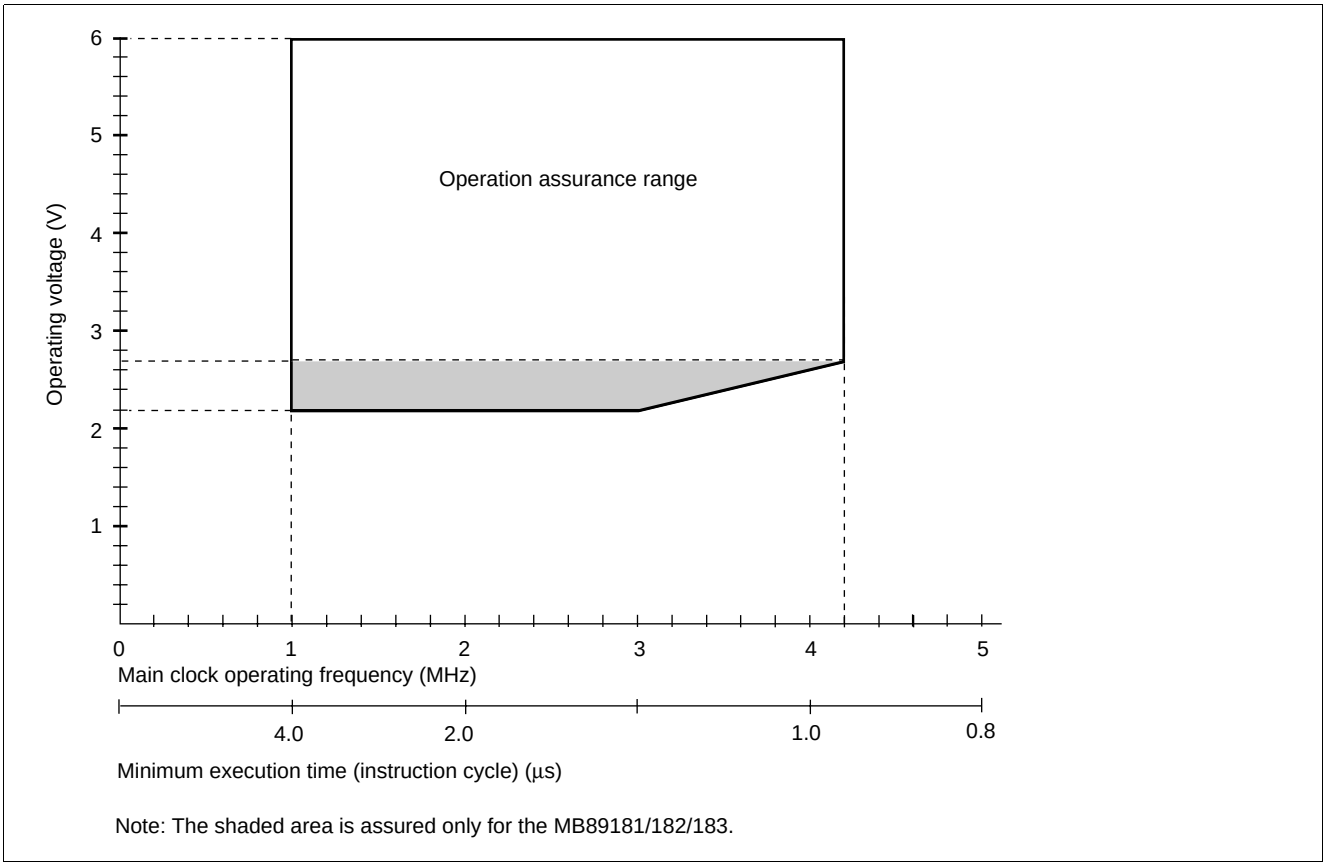


Figure 1 Operating Voltage vs. Main Clock Operating Frequency

3. DC Characteristics

(V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
"H" level input voltage	V_{IH}	P00 to P07, P10 to P17, P20 to P27	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	CMOS input
	V_{IHS}	$\overline{RST}$, MODA, EC, SI, SCK, INT10 to INT13, INT20 to INT27		0.8 V_{CC}	—	V_{CC} + 0.3	V	Hysteresis input
"L" level input voltage	V_{IL}	P00 to P07, P10 to P17, P20 to P27		V_{SS} – 0.3	—	0.3 V_{CC}	V	CMOS input
	V_{ILS}	$\overline{RST}$, MODA, EC, SI, SCK, INT10 to INT13, INT20 to INT27		V_{SS} – 0.3	—	0.2 V_{CC}	V	Hysteresis input
Open-drain output pin application voltage	V_D	P20 to P27, P40 to P47, P50 to P57		V_{SS} – 0.3	—	V_{SS} + 6.0	V	Without pull-up resistor
"H" level output voltage	V_{OH1}	P00 to P07, P10 to P17	I_{OH} = –2.0 mA	2.4	—	—	V	
	V_{OH2}	P30	I_{OH} = –6.0 mA	4.0	—	—	V	
"L" level output voltage	V_{OL}	P00 to P07, P10 to P17, P20, P22 to P25, P30 to P32, P40 to P47, P50 to P57	I_{OL} = +1.8 mA	—	—	0.4	V	
	V_{OL2}	P21, P26, P27	I_{OL} = +8.0 mA	—	—	0.4	V	
	V_{OL3}	$\overline{RST}$	I_{OL} = +4.0 mA	—	—	0.4	V	
Input leakage current (Hi-z output leakagecurrent)	I_{LI1}	MODA, P00to P07, P10 to P17, P30 to P32	0.0 V < V_I < V_{CC}	—	—	±5	µA	Without pull-up resistor
	I_{LI2}	P20 to P27, P40 to P47, P50 to P57	0.0 V < V_I < 6 V	—	—	±1	µA	Without pull-up resistor
Pull-up resistance	R_{PULL}	P00 to P07, P10 to P17, P20 to P27, P40 to P47, P50 to P57, $\overline{RST}$	V_I = 0.0 V	25	50	100	kΩ	Without pull-up resistor
Common output impedance	R_{VCOM}	COM0 to COM3	V1 to V3 = 5.0 V	—	—	2.5	kΩ	
Segment output impedance	R_{VSEG}	SEG0 to SEG31	V1 to V3 = 5.0 V	—	—	15	kΩ	

(Continued)

(Continued)

(V_{CC} = +5.0 V, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
LCD divided resistor value	R_{LCD}	—	Between V_{CC} and V_{SS}	300	500	750	kΩ	
LCD controller/ driver leakage current	I_{LCDL}	V1 to V3, COM0 to COM3, SEG0 to SEG31	—	—	—	±1	µA	
Power supply current*2	I_{CC1}	V_{CC}	F_{CH} = 4.2 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.95 µs, • Main clock operation mode	—	3.0	4.5	mA	MB89181/ 182/183/ PV180
				—	3.8	6.0	mA	MB89P185
	I_{CC2}		F_{CH} = 4.2 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 15.2 µs, • Main clock operation mode	—	0.25	0.4	mA	MB89181/ 182/183/ PV180
				—	0.85	1.4	mA	MB89P185
	I_{CCL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, t_{inst}*2 = 61 µs, • Subclock operation mode	—	0.05	0.1	mA	MB89181/ 182/183/ PV180
				—	0.65	1.1	mA	MB89P185
	I_{CCS1}		F_{CH} = 4.2 MHz, V_{CC} = 5.0 V, t_{inst}*2 = 0.95 µs, • Main clock sleep mode	—	0.8	1.2	mA	
	I_{CCS2}		F_{CH} = 4.2 MHz, V_{CC} = 3.0 V, t_{inst}*2 = 15.2 µs, • Main clock sleep mode	—	0.2	0.3	mA	
	I_{CCSL}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, t_{inst}*2 = 61 µs, • Subclock mode	—	25	50	µA	
	I_{CCT}		F_{CL} = 32.768 kHz, V_{CC} = 3.0 V, • Watch mode	—	10	15	µA	
	I_{CCH}		T_A = +25°C, V_{CC} = 5.0 V, • Stop mode	—	0.1	1	µA	MB89181/ 182/183
				—	0.1	10	µA	MB89PV18 0/P185
Input capacitance	C_{IN}	Other V_{CC} and V_{SS}	f = 1 MHz	—	10	—	pF	

*1: The measurement conditions of power supply current are as follows: the external clock, open output pins, and the external LCD dividing resistor. In the case of the MB89PV180, the current consumed by the connected EPROM and ICE is not included.

*2: For information on t_{inst}, see “(4) Instruction Cycle” in “4. AC Characteristics.”

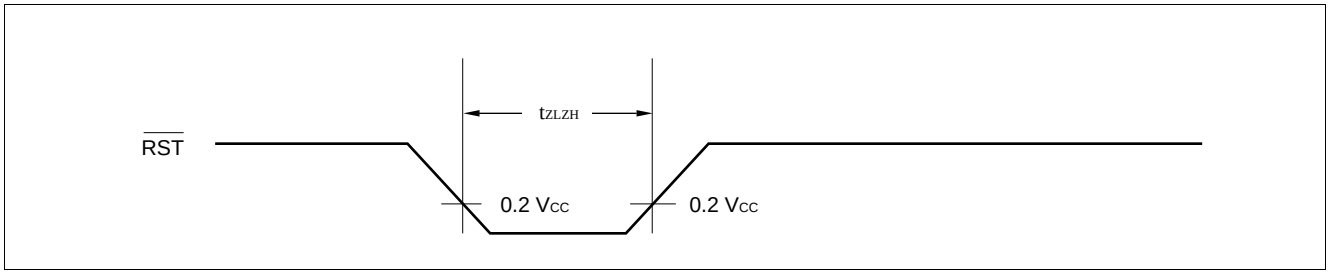
Note: For pins which serve as the segment (SEG8 to SEG31) and ports (P10 to P17, P40 to P47, and P50 to P57), see the port parameter when these pins are used as ports and the segment parameter when they are used as segment pins.

4. AC Characteristics

(1) Reset Timing

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
$\overline{RST}$ "L" pulse width	t_{ZLZH}	—	48 t_{HCYL}	—	ns	

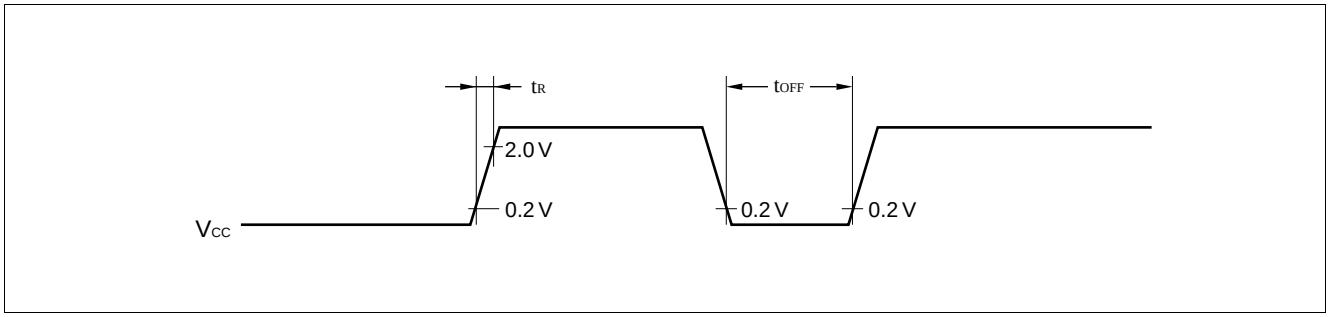


(2) Power-on Reset

(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Condition	Value		Unit	Remarks
			Min.	Max.		
Power supply rising time	t_R	—	—	50	ms	Power-on reset function only
Power supply cut-off time	t_{OFF}		1	—	ms	Due to repeated operations

Note: Make sure that power supply rises within the selected oscillation stabilization time.
If power supply voltage needs to be varied in the course of operation, a smooth voltage rise is recommended.

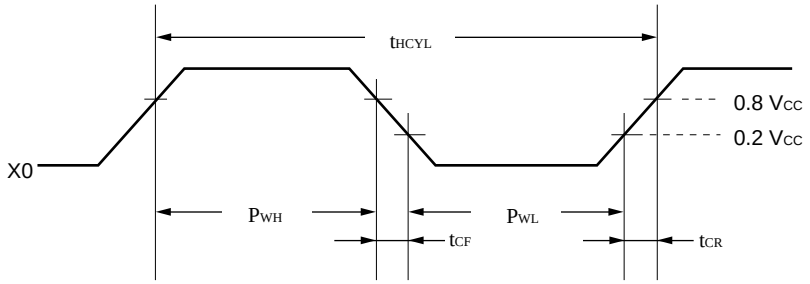


(3) Clock Timing

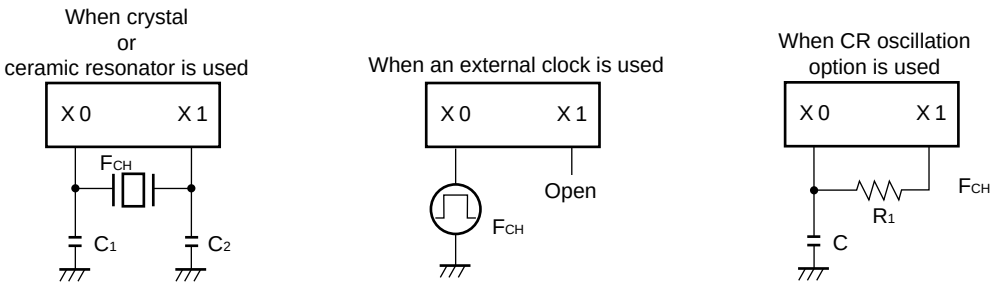
(V_{SS} = 0.0 V, T_A = –40°C to +85°C)

Parameter	Symbol	Pin	Value			Unit	Remarks
			Min.	Typ.	Max.		
Clock frequency	F_{CH}	X0, X1	1	—	4.2	MHz	Main clock
	F_{CL}	X0A, X1A	—	32.768	—	kHz	Subclock
Clock cycle time	t_{HCYL}	X0, X1	238	—	1000	ns	Main clock
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	Subclock
Input clock pulse width	P_{WH} P_{WL}	X0	20	—	—	ns	External clock
	P_{WHL} P_{WLL}	X0A	—	15.2	—	µs	
Input clock pulse rising/ falling time	t_{CR} t_{CF}	X0, X0A	—	—	10	ns	

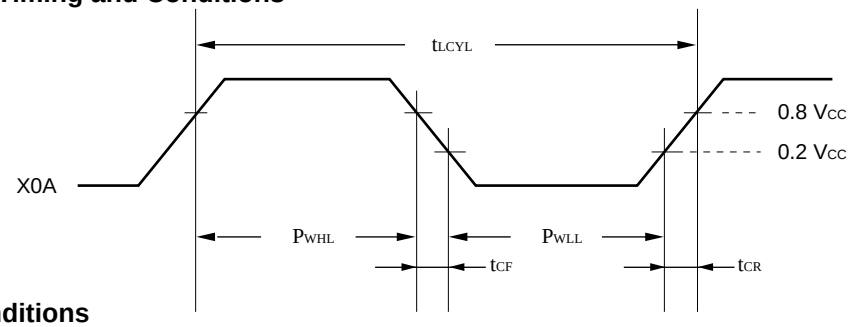
X0 and X1 Timing and Conditions



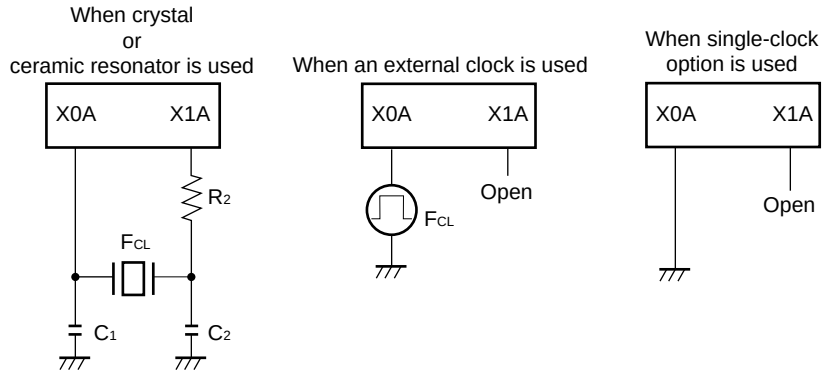
Main clock Conditions



X0A and X1A Timing and Conditions



Subclock Conditions



(4) Instruction Cycle

Parameter	Symbol	Value (typical)	Unit	Remarks
Instruction cycle (minimum execution time)	t_{inst}	$4/F_{CH}$, $8/F_{CH}$, $16/F_{CH}$, $64/F_{CH}$	µs	$(4/F_{CH})$ t_{inst} = 0.95 µs when operating at F_{CH} = 4.2 MHz
		$2/F_{CL}$	µs	t_{inst} = 61.036 µs when operating at F_{CL} = 32.768 kHz

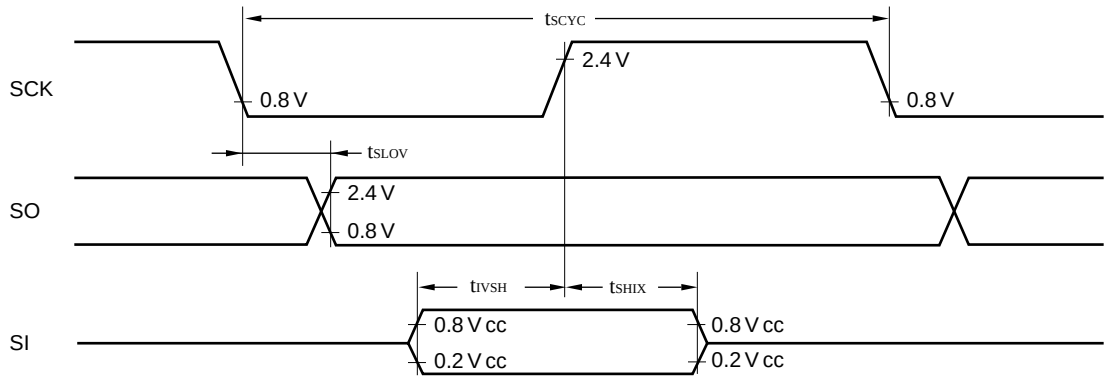
(5) Serial I/O Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

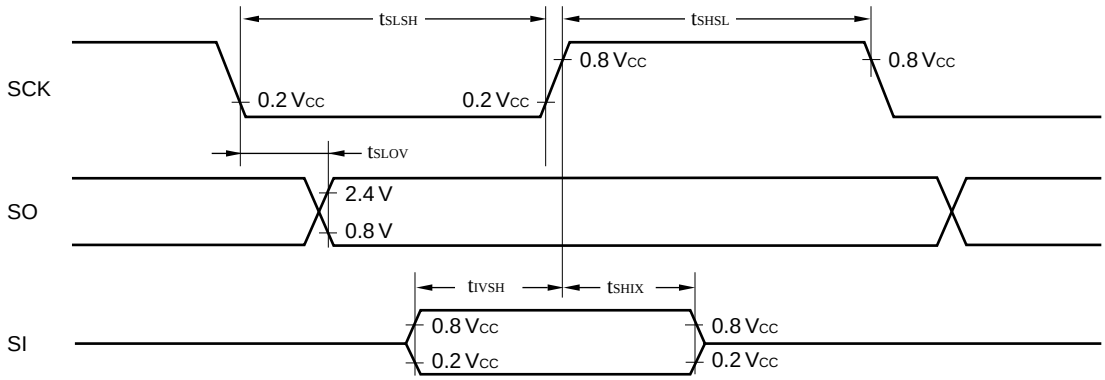
Parameter	Symbol	Pin	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK	Internal shift clock mode	2 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		–200	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	
Serial clock “H” pulse width	t_{SHSL}	SCK	External shift clock mode	1 t_{inst}*	—	µs	
Serial clock “L” pulse width	t_{SLSH}	SCK		1 t_{inst}*	—	µs	
SCK ↓ → SO time	t_{SLOV}	SCK, SO		0	200	ns	
Valid SI → SCK ↑	t_{IVSH}	SI, SCK		0.5 t_{inst}*	—	µs	
SCK ↑ → valid SI hold time	t_{SHIX}	SCK, SI		0.5 t_{inst}*	—	µs	

* : For information on t_{inst}, see “(4) Instruction Cycle.”

Internal Shift Clock Mode



External Shift Clock Mode

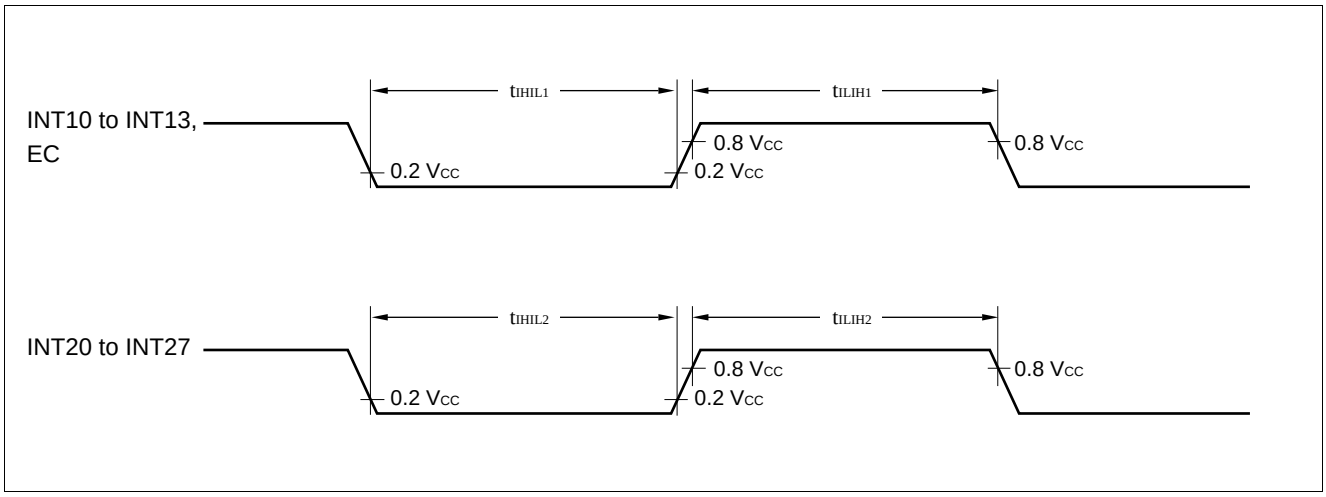


(6) Peripheral Input Timing

(V_{CC} = +5.0 V±10%, AV_{SS} = V_{SS} = 0.0 V, T_A = –40°C to +85°C)

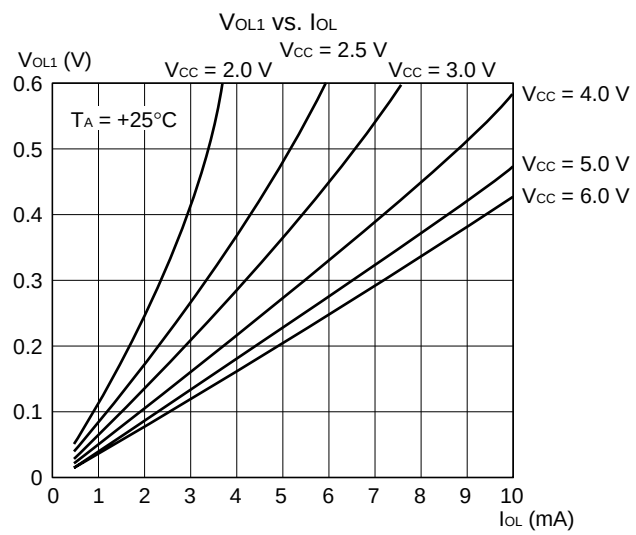
Parameter	Symbol	Pin	Value		Unit	Remarks
			Min.	Max.		
Peripheral input “H” pulse width 1	t_{ILIH1}	INT10 to INT13, EC	1 t_{inst}*	—	µs	
Peripheral input “L” pulse width 1	t_{IHIL1}	INT10 to INT13, EC	1 t_{inst}*	—	µs	
Peripheral input “H” pulse width 2	t_{ILIH2}	INT20 to INT27	2 t_{inst}*	—	µs	
Peripheral input “L” pulse width 2	t_{IHIL2}	INT20 to INT27	2 t_{inst}*	—	µs	

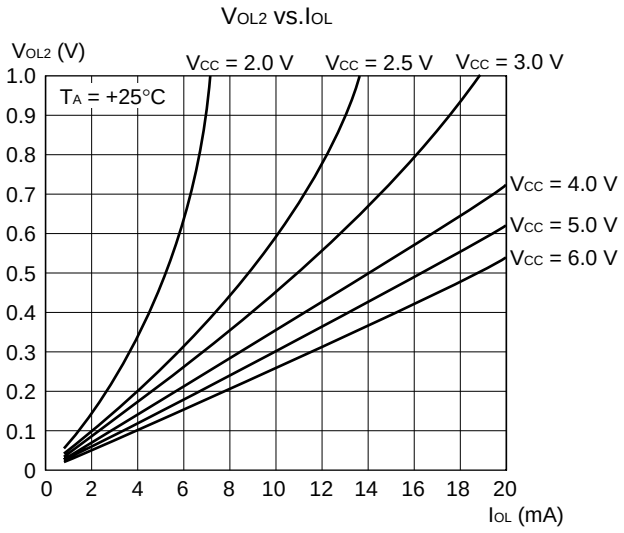
* : For information on t_{inst}, see “(4) Instruction Cycle.”



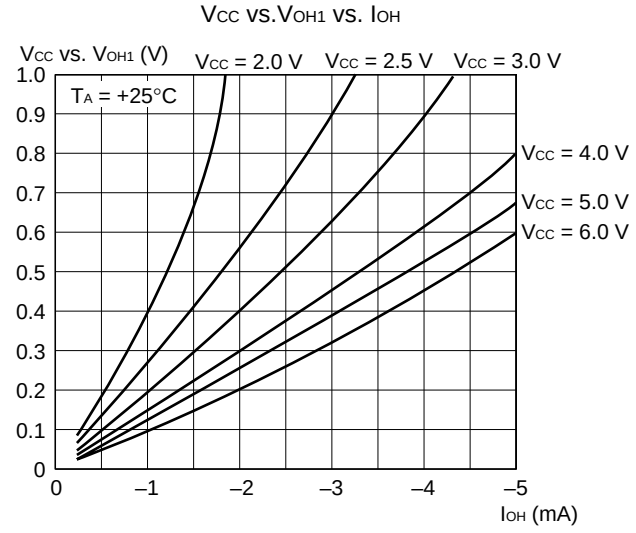
■ EXAMPLE CHARACTERISTICS

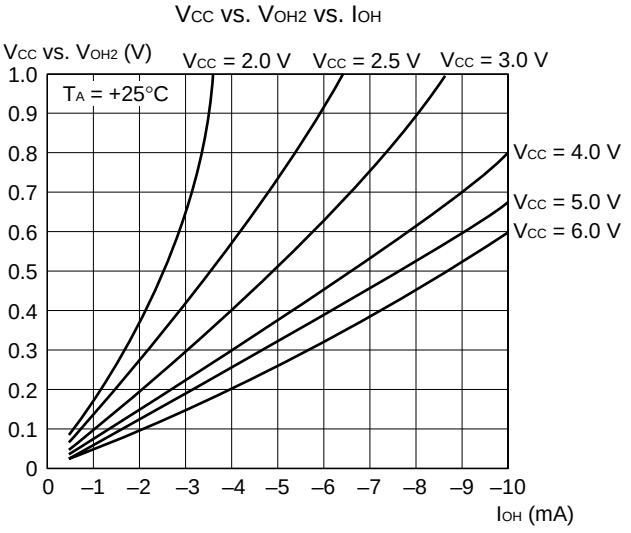
(1) “L” level Output Voltage



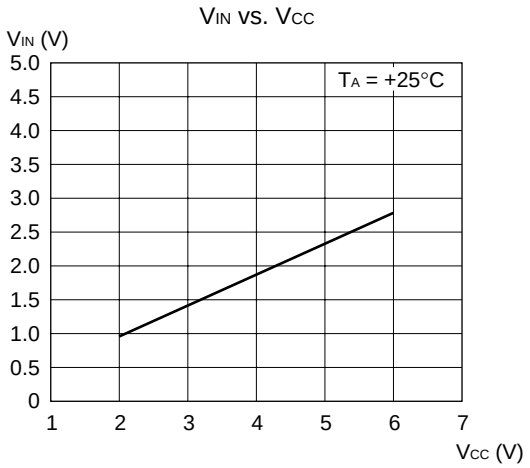


(2) “H” level Output Voltage

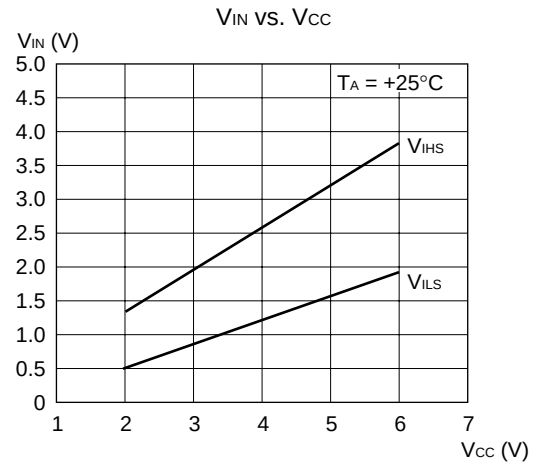




(3) "H" Level Input Voltage/"L" Level Input Voltage (CMOS Input)



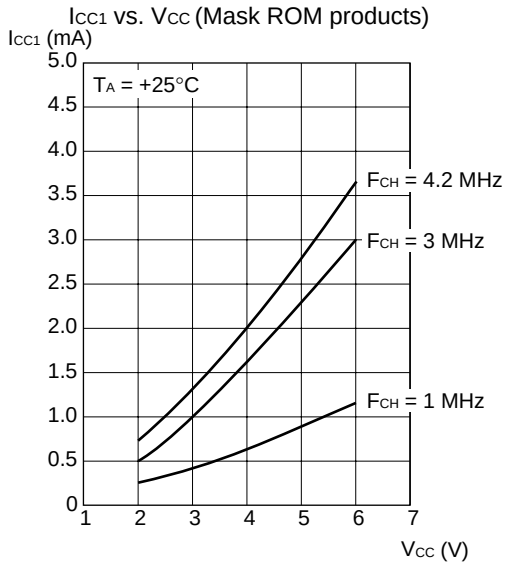
(4) "H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

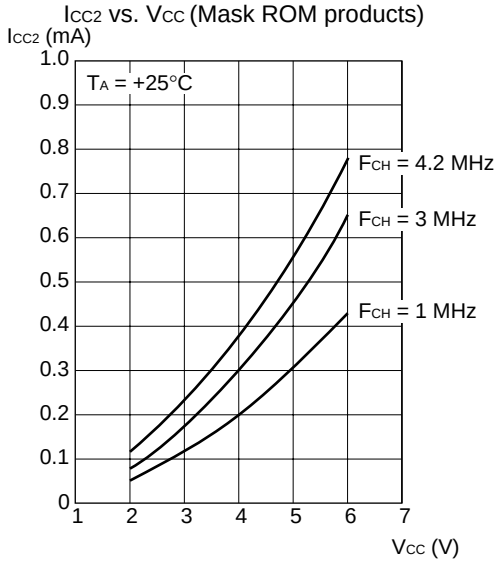


V_{IHS}: Threshold when input voltage in hysteresis characteristics is set to "H" level

V_{ILS}: Threshold when input voltage in hysteresis characteristics is set to "L" level

(5) Power Supply Current (External Clock)





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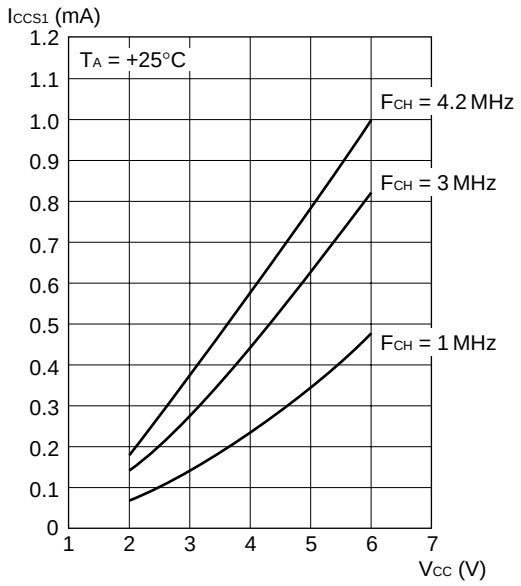
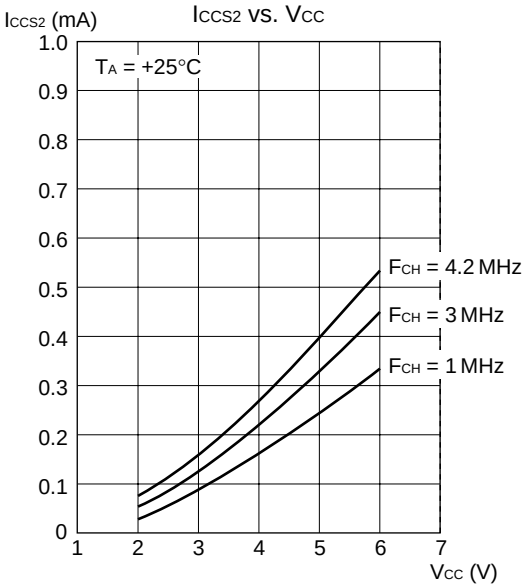
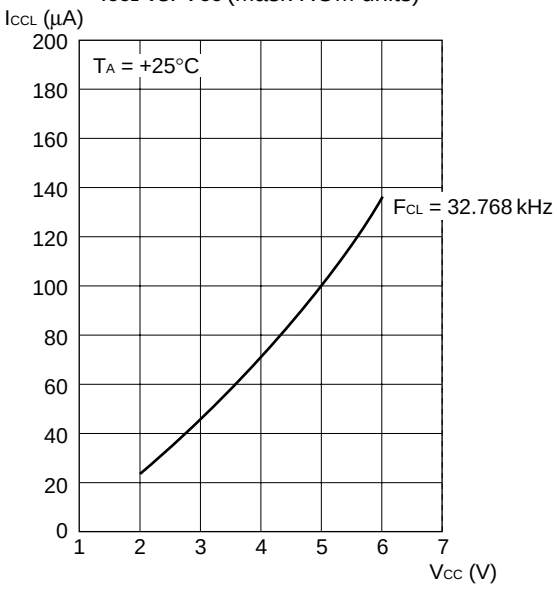
I_{CCS1} vs. V_{CC}



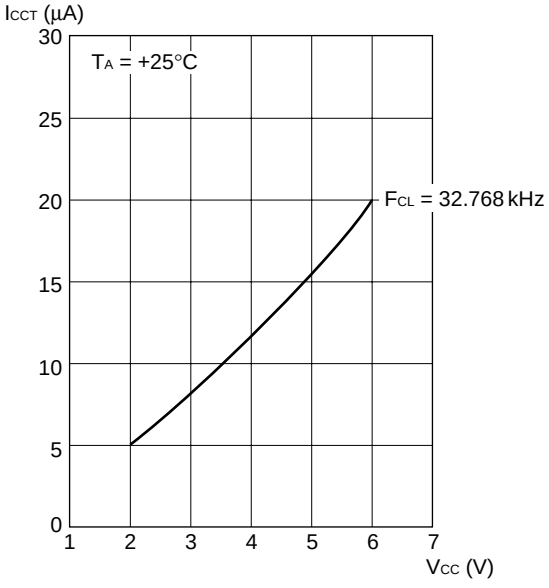
I_{CCS2} vs. V_{CC}



I_{CCL} vs. V_{CC} (Mask ROM units)



I_{CCT} vs. V_{CC}



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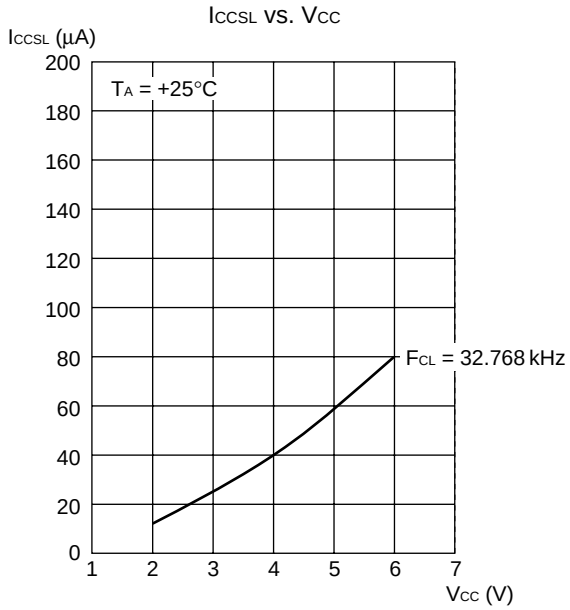
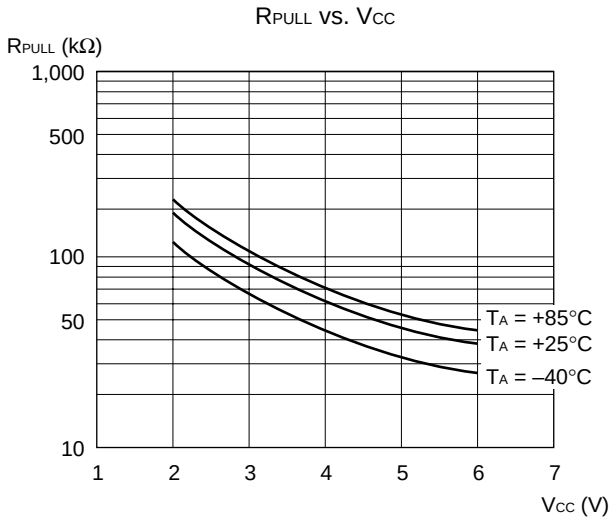


(6) Pull-up Resistance Value



■ INSTRUCTIONS

Execution instructions can be divided into the following four groups:

- Transfer
- Arithmetic operation
- Branch
- Others

Table 1 lists symbols used for notation of instructions.

Table 1 Instruction Symbols

Symbol	Meaning
dir	Direct address (8 bits)
off	Offset (8 bits)
ext	Extended address (16 bits)
#vct	Vector table number (3 bits)
#d8	Immediate data (8 bits)
#d16	Immediate data (16 bits)
dir: b	Bit direct address (8:3 bits)
rel	Branch relative address (8 bits)
@	Register indirect (Example: @A, @IX, @EP)
A	Accumulator A (Whether its length is 8 or 16 bits is determined by the instruction in use.)
AH	Upper 8 bits of accumulator A (8 bits)
AL	Lower 8 bits of accumulator A (8 bits)
T	Temporary accumulator T (Whether its length is 8 or 16 bits is determined by the instruction in use.)
TH	Upper 8 bits of temporary accumulator T (8 bits)
TL	Lower 8 bits of temporary accumulator T (8 bits)
IX	Index register IX (16 bits)

(Continued)

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Symbol	Meaning
EP	Extra pointer EP (16 bits)
PC	Program counter PC (16 bits)
SP	Stack pointer SP (16 bits)
PS	Program status PS (16 bits)
dr	Accumulator A or index register IX (16 bits)
CCR	Condition code register CCR (8 bits)
RP	Register bank pointer RP (5 bits)
Ri	General-purpose register Ri (8 bits, i = 0 to 7)
×	Indicates that the very × is the immediate data. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
(×)	Indicates that the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)
((×))	The address indicated by the contents of × is the target of accessing. (Whether its length is 8 or 16 bits is determined by the instruction in use.)

Columns indicate the following:

Mnemonic: Assembler notation of an instruction

~: Number of instructions

#: Number of bytes

Operation: Operation of an instruction

TL, TH, AH: A content change when each of the TL, TH, and AH instructions is executed. Symbols in the column indicate the following:

- "–" indicates no change.
- dH is the 8 upper bits of operation description data.
- AL and AH must become the contents of AL and AH immediately before the instruction is executed.
- 00 becomes 00.

N, Z, V, C: An instruction of which the corresponding flag will change. If + is written in this column, the relevant instruction will change its corresponding flag.

OP code: Code of an instruction. If an instruction is more than one code, it is written according to the following rule:

Example: 48 to 4F ← This indicates 48, 49, ... 4F.

Table 2 Transfer Instructions (48 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
MOV dir,A	3	2	(dir) ← (A)	–	–	–	– – – –	45
MOV @IX +off,A	4	2	((IX) +off) ← (A)	–	–	–	– – – –	46
MOV ext,A	4	3	(ext) ← (A)	–	–	–	– – – –	61
MOV @EP,A	3	1	((EP)) ← (A)	–	–	–	– – – –	47
MOV Ri,A	3	1	(Ri) ← (A)	–	–	–	– – – –	48 to 4F
MOV A,#d8	2	2	(A) ← d8	AL	–	–	+ + – –	04
MOV A,dir	3	2	(A) ← (dir)	AL	–	–	+ + – –	05
MOV A,@IX +off	4	2	(A) ← ((IX) +off)	AL	–	–	+ + – –	06
MOV A,ext	4	3	(A) ← (ext)	AL	–	–	+ + – –	60
MOV A,@A	3	1	(A) ← ((A))	AL	–	–	+ + – –	92
MOV A,@EP	3	1	(A) ← ((EP))	AL	–	–	+ + – –	07
MOV A,Ri	3	1	(A) ← (Ri)	AL	–	–	+ + – –	08 to 0F
MOV dir,#d8	4	3	(dir) ← d8	–	–	–	– – – –	85
MOV @IX +off,#d8	5	3	((IX) +off) ← d8	–	–	–	– – – –	86
MOV @EP,#d8	4	2	((EP)) ← d8	–	–	–	– – – –	87
MOV Ri,#d8	4	2	(Ri) ← d8	–	–	–	– – – –	88 to 8F
MOVW dir,A	4	2	(dir) ← (AH),(dir + 1) ← (AL)	–	–	–	– – – –	D5
MOVW @IX +off,A	5	2	((IX) +off) ← (AH), ((IX) +off + 1) ← (AL)	–	–	–	– – – –	D6
MOVW ext,A	5	3	(ext) ← (AH), (ext + 1) ← (AL)	–	–	–	– – – –	D4
MOVW @EP,A	4	1	((EP)) ← (AH),((EP) + 1) ← (AL)	–	–	–	– – – –	D7
MOVW EP,A	2	1	(EP) ← (A)	–	–	–	– – – –	E3
MOVW A,#d16	3	3	(A) ← d16	AL	AH	dH	+ + – –	E4
MOVW A,dir	4	2	(AH) ← (dir), (AL) ← (dir + 1)	AL	AH	dH	+ + – –	C5
MOVW A,@IX +off	5	2	(AH) ← ((IX) +off), (AL) ← ((IX) +off + 1)	AL	AH	dH	+ + – –	C6
MOVW A,ext	5	3	(AH) ← (ext), (AL) ← (ext + 1)	AL	AH	dH	+ + – –	C4
MOVW A,@A	4	1	(AH) ← ((A)), (AL) ← ((A)) + 1)	AL	AH	dH	+ + – –	93
MOVW A,@EP	4	1	(AH) ← ((EP)), (AL) ← ((EP) + 1)	AL	AH	dH	+ + – –	C7
MOVW A,EP	2	1	(A) ← (EP)	–	–	dH	– – – –	F3
MOVW EP,#d16	3	3	(EP) ← d16	–	–	–	– – – –	E7
MOVW IX,A	2	1	(IX) ← (A)	–	–	–	– – – –	E2
MOVW A,IX	2	1	(A) ← (IX)	–	–	dH	– – – –	F2
MOVW SP,A	2	1	(SP) ← (A)	–	–	–	– – – –	E1
MOVW A,SP	2	1	(A) ← (SP)	–	–	dH	– – – –	F1
MOV @A,T	3	1	((A)) ← (T)	–	–	–	– – – –	82
MOVW @A,T	4	1	((A)) ← (TH),((A) + 1) ← (TL)	–	–	–	– – – –	83
MOVW IX,#d16	3	3	(IX) ← d16	–	–	–	– – – –	E6
MOVW A,PS	2	1	(A) ← (PS)	–	–	dH	– – – –	70
MOVW PS,A	2	1	(PS) ← (A)	–	–	–	+ + + +	71
MOVW SP,#d16	3	3	(SP) ← d16	–	–	–	– – – –	E5
SWAP	2	1	(AH) ↔ (AL)	–	–	AL	– – – –	10
SETB dir: b	4	2	(dir): b ← 1	–	–	–	– – – –	A8 to AF
CLRB dir: b	4	2	(dir): b ← 0	–	–	–	– – – –	A0 to A7
XCH A,T	2	1	(AL) ↔ (TL)	AL	–	–	– – – –	42
XCHW A,T	3	1	(A) ↔ (T)	AL	AH	dH	– – – –	43
XCHW A,EP	3	1	(A) ↔ (EP)	–	–	dH	– – – –	F7
XCHW A,IX	3	1	(A) ↔ (IX)	–	–	dH	– – – –	F6
XCHW A,SP	3	1	(A) ↔ (SP)	–	–	dH	– – – –	F5
MOVW A,PC	2	1	(A) ← (PC)	–	–	dH	– – – –	F0

Notes: • During byte transfer to A, T ← A is restricted to low bytes.
• Operands in more than one operand instruction must be stored in the order in which their mnemonics are written. (Reverse arrangement of F²MC-8 family)

Table 3 Arithmetic Operation Instructions (62 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
ADDC A,Ri	3	1	(A) ← (A) + (Ri) + C	–	–	–	+ + + +	28 to 2F
ADDC A,#d8	2	2	(A) ← (A) + d8 + C	–	–	–	+ + + +	24
ADDC A,dir	3	2	(A) ← (A) + (dir) + C	–	–	–	+ + + +	25
ADDC A,@IX +off	4	2	(A) ← (A) + ((IX) +off) + C	–	–	–	+ + + +	26
ADDC A,@EP	3	1	(A) ← (A) + ((EP)) + C	–	–	–	+ + + +	27
ADDCW A	3	1	(A) ← (A) + (T) + C	–	–	dH	+ + + +	23
ADDC A	2	1	(AL) ← (AL) + (TL) + C	–	–	–	+ + + +	22
SUBC A,Ri	3	1	(A) ← (A) – (Ri) – C	–	–	–	+ + + +	38 to 3F
SUBC A,#d8	2	2	(A) ← (A) – d8 – C	–	–	–	+ + + +	34
SUBC A,dir	3	2	(A) ← (A) – (dir) – C	–	–	–	+ + + +	35
SUBC A,@IX +off	4	2	(A) ← (A) – ((IX) +off) – C	–	–	–	+ + + +	36
SUBC A,@EP	3	1	(A) ← (A) – ((EP)) – C	–	–	–	+ + + +	37
SUBCW A	3	1	(A) ← (T) – (A) – C	–	–	dH	+ + + +	33
SUBC A	2	1	(AL) ← (TL) – (AL) – C	–	–	–	+ + + +	32
INC Ri	4	1	(Ri) ← (Ri) + 1	–	–	–	+ + + –	C8 to CF
INCW EP	3	1	(EP) ← (EP) + 1	–	–	–	– – – –	C3
INCW IX	3	1	(IX) ← (IX) + 1	–	–	–	– – – –	C2
INCW A	3	1	(A) ← (A) + 1	–	–	dH	+ + – –	C0
DEC Ri	4	1	(Ri) ← (Ri) – 1	–	–	–	+ + + –	D8 to DF
DECW EP	3	1	(EP) ← (EP) – 1	–	–	–	– – – –	D3
DECW IX	3	1	(IX) ← (IX) – 1	–	–	–	– – – –	D2
DECW A	3	1	(A) ← (A) – 1	–	–	dH	+ + – –	D0
MULU A	19	1	(A) ← (AL) × (TL)	–	–	dH	– – – –	01
DIVU A	21	1	(A) ← (T) / (AL),MOD → (T)	dL	00	00	– – – –	11
ANDW A	3	1	(A) ← (A) ∧ (T)	–	–	dH	+ + R –	63
ORW A	3	1	(A) ← (A) ∨ (T)	–	–	dH	+ + R –	73
XORW A	3	1	(A) ← (A) ∀ (T)	–	–	dH	+ + R –	53
CMP A	2	1	(TL) – (AL)	–	–	–	+ + + +	12
CMPW A	3	1	(T) – (A)	–	–	–	+ + + +	13
RORC A	2	1	→ C → A	–	–	–	+ + – +	03
ROLC A	2	1	C ← A ←	–	–	–	+ + – +	02
CMP A,#d8	2	2	(A) – d8	–	–	–	+ + + +	14
CMP A,dir	3	2	(A) – (dir)	–	–	–	+ + + +	15
CMP A,@EP	3	1	(A) – ((EP))	–	–	–	+ + + +	17
CMP A,@IX +off	4	2	(A) – ((IX) +off)	–	–	–	+ + + +	16
CMP A,Ri	3	1	(A) – (Ri)	–	–	–	+ + + +	18 to 1F
DAA	2	1	Decimal adjust for addition	–	–	–	+ + + +	84
DAS	2	1	Decimal adjust for subtraction	–	–	–	+ + + +	94
XOR A	2	1	(A) ← (AL) ∀ (TL)	–	–	–	+ + R –	52
XOR A,#d8	2	2	(A) ← (AL) ∀ d8	–	–	–	+ + R –	54
XOR A,dir	3	2	(A) ← (AL) ∀ (dir)	–	–	–	+ + R –	55
XOR A,@EP	3	1	(A) ← (AL) ∀ ((EP))	–	–	–	+ + R –	57
XOR A,@IX +off	4	2	(A) ← (AL) ∀ ((IX) +off)	–	–	–	+ + R –	56
XOR A,Ri	3	1	(A) ← (AL) ∀ (Ri)	–	–	–	+ + R –	58 to 5F
AND A	2	1	(A) ← (AL) ∧ (TL)	–	–	–	+ + R –	62
AND A,#d8	2	2	(A) ← (AL) ∧ d8	–	–	–	+ + R –	64
AND A,dir	3	2	(A) ← (AL) ∧ (dir)	–	–	–	+ + R –	65

(Continued)

(Continued)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
AND A,@EP	3	1	(A) ← (AL) ∧ ((EP))	–	–	–	+ + R –	67
AND A,@IX +off	4	2	(A) ← (AL) ∧ ((IX) +off)	–	–	–	+ + R –	66
AND A,Ri	3	1	(A) ← (AL) ∧ (Ri)	–	–	–	+ + R –	68 to 6F
OR A	2	1	(A) ← (AL) ∨ (TL)	–	–	–	+ + R –	72
OR A,#d8	2	2	(A) ← (AL) ∨ d8	–	–	–	+ + R –	74
OR A,dir	3	2	(A) ← (AL) ∨ (dir)	–	–	–	+ + R –	75
OR A,@EP	3	1	(A) ← (AL) ∨ ((EP))	–	–	–	+ + R –	77
OR A,@IX +off	4	2	(A) ← (AL) ∨ ((IX) +off)	–	–	–	+ + R –	76
OR A,Ri	3	1	(A) ← (AL) ∨ (Ri)	–	–	–	+ + R –	78 to 7F
CMP dir,#d8	5	3	(dir) – d8	–	–	–	+ + + +	95
CMP @EP,#d8	4	2	((EP)) – d8	–	–	–	+ + + +	97
CMP @IX +off,#d8	5	3	((IX) + off) – d8	–	–	–	+ + + +	96
CMP Ri,#d8	4	2	(Ri) – d8	–	–	–	+ + + +	98 to 9F
INCW SP	3	1	(SP) ← (SP) + 1	–	–	–	– – – –	C1
DECW SP	3	1	(SP) ← (SP) – 1	–	–	–	– – – –	D1

Table 4 Branch Instructions (17 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
BZ/BEQ rel	3	2	If Z = 1 then PC ← PC + rel	–	–	–	– – – –	FD
BNZ/BNE rel	3	2	If Z = 0 then PC ← PC + rel	–	–	–	– – – –	FC
BC/BLO rel	3	2	If C = 1 then PC ← PC + rel	–	–	–	– – – –	F9
BNC/BHS rel	3	2	If C = 0 then PC ← PC + rel	–	–	–	– – – –	F8
BN rel	3	2	If N = 1 then PC ← PC + rel	–	–	–	– – – –	FB
BP rel	3	2	If N = 0 then PC ← PC + rel	–	–	–	– – – –	FA
BLT rel	3	2	If V ∀ N = 1 then PC ← PC + rel	–	–	–	– – – –	FF
BGE rel	3	2	If V ∀ N = 0 then PC ← PC + rel	–	–	–	– – – –	FE
BBC dir: b,rel	5	3	If (dir: b) = 0 then PC ← PC + rel	–	–	–	– + – –	B0 to B7
BBS dir: b,rel	5	3	If (dir: b) = 1 then PC ← PC + rel	–	–	–	– + – –	B8 to BF
JMP @A	2	1	(PC) ← (A)	–	–	–	– – – –	E0
JMP ext	3	3	(PC) ← ext	–	–	–	– – – –	21
CALLV #vct	6	1	Vector call	–	–	–	– – – –	E8 to EF
CALL ext	6	3	Subroutine call	–	–	–	– – – –	31
XCHW A,PC	3	1	(PC) ← (A),(A) ← (PC) + 1	–	–	dH	– – – –	F4
RET	4	1	Return from subrountine	–	–	–	– – – –	20
RETI	6	1	Return form interrupt	–	–	–	Restore	30

Table 5 Other Instructions (9 instructions)

Mnemonic	~	#	Operation	TL	TH	AH	N Z V C	OP code
PUSHW A	4	1		–	–	–	– – – –	40
POPW A	4	1		–	–	dH	– – – –	50
PUSHW IX	4	1		–	–	–	– – – –	41
POPW IX	4	1		–	–	–	– – – –	51
NOP	1	1		–	–	–	– – – –	00
CLRC	1	1		–	–	–	– – – R	81
SETC	1	1		–	–	–	– – – S	91
CLRI	1	1		–	–	–	– – – –	80
SETI	1	1		–	–	–	– – – –	90

■ INSTRUCTION MAP

L \ H	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	NOP	SWAP	RET	RETI	PUSHW A	POPW A	MOV A,ext	MOVW A,PS	CLRI	SETI	CLRB dir: 0	BBC dir: 0,rel	INCW A	DECW A	JMP @A	MOVW A,PC
1	MULU A	DIVU A	JMP addr16	CALL addr16	PUSHW IX	POPW IX	MOV ext,A	MOVW PS,A	CLRC	SETC	CLRB dir: 1	BBC dir: 1,rel	INCW SP	DECW SP	MOVW SP,A	MOVW A,SP
2	ROLC A	CMP A	ADDC A	SUBC A	XCH A, T	XOR A	AND A	OR A	MOV @A,T	MOV A,@A	CLRB dir: 2	BBC dir: 2,rel	INCW IX	DECW IX	MOVW IX,A	MOVW A,IX
3	RORC A	CMPW A	ADDCW A	SUBCW A	XCHW A, T	XORW A	ANDW A	ORW A	MOVW @A,T	MOVW A,@A	CLRB dir: 3	BBC dir: 3,rel	INCW EP	DECW EP	MOVW EP,A	MOVW A,EP
4	MOV A,#d8	CMP A,#d8	ADDC A,#d8	SUBC A,#d8		XOR A,#d8	AND A,#d8	OR A,#d8	DAA	DAS	CLRB dir: 4	BBC dir: 4,rel	MOVW A,ext	MOVW ext,A	MOVW A,#d16	XCHW A,PC
5	MOV A,dir	CMP A,dir	ADDC A,dir	SUBC A,dir	MOV dir,A	XOR A,dir	AND A,dir	OR A,dir	MOV dir,#d8	CMP dir,#d8	CLRB dir: 5	BBC dir: 5,rel	MOVW A,dir	MOVW dir,A	MOVW SP,#d16	XCHW A,SP
6	MOV A,@IX +d	CMP A,@IX +d	ADDC A,@IX +d	SUBC A,@IX +d	MOV @IX +d,A	XOR A,@IX +d	AND A,@IX +d	OR A,@IX +d	MOV @IX +d,#d8	CMP @IX +d,#d8	CLRB dir: 6	BBC dir: 6,rel	MOVW A,@IX +d	MOVW @IX +d,A	MOVW IX,#d16	XCHW A,IX
7	MOV A,@EP	CMP A,@EP	ADDC A,@EP	SUBC A,@EP	MOV @EP,A	XOR A,@EP	AND A,@EP	OR A,@EP	MOV @EP,#d8	CMP @EP,#d8	CLRB dir: 7	BBC dir: 7,rel	MOVW A,@EP	MOVW @EP,A	MOVW EP,#d16	XCHW A,EP
8	MOV A,R0	CMP A,R0	ADDC A,R0	SUBC A,R0	MOV R0,A	XOR A,R0	AND A,R0	OR A,R0	MOV R0,#d8	CMP R0,#d8	SETB dir: 0	BBS dir: 0,rel	INC R0	DEC R0	CALLV #0	BNC rel
9	MOV A,R1	CMP A,R1	ADDC A,R1	SUBC A,R1	MOV R1,A	XOR A,R1	AND A,R1	OR A,R1	MOV R1,#d8	CMP R1,#d8	SETB dir: 1	BBS dir: 1,rel	INC R1	DEC R1	CALLV #1	BC rel
A	MOV A,R2	CMP A,R2	ADDC A,R2	SUBC A,R2	MOV R2,A	XOR A,R2	AND A,R2	OR A,R2	MOV R2,#d8	CMP R2,#d8	SETB dir: 2	BBS dir: 2,rel	INC R2	DEC R2	CALLV #2	BP rel
B	MOV A,R3	CMP A,R3	ADDC A,R3	SUBC A,R3	MOV R3,A	XOR A,R3	AND A,R3	OR A,R3	MOV R3,#d8	CMP R3,#d8	SETB dir: 3	BBS dir: 3,rel	INC R3	DEC R3	CALLV #3	BN rel
C	MOV A,R4	CMP A,R4	ADDC A,R4	SUBC A,R4	MOV R4,A	XOR A,R4	AND A,R4	OR A,R4	MOV R4,#d8	CMP R4,#d8	SETB dir: 4	BBS dir: 4,rel	INC R4	DEC R4	CALLV #4	BNZ rel
D	MOV A A,R5	CMP A,R5	ADDC A,R5	SUBC A,R5	MOV R5,A	XOR A,R5	AND A,R5	OR A,R5	MOV R5,#d8	CMP R5,#d8	SETB dir: 5	BBS dir: 5,rel	INC R5	DEC R5	CALLV #5	BZ rel
E	MOV A,R6	CMP A,R6	ADDC A,R6	SUBC A,R6	MOV R6,A	XOR A,R6	AND A,R6	OR A,R6	MOV R6,#d8	CMP R6,#d8	SETB dir: 6	BBS dir: 6,rel	INC R6	DEC R6	CALLV #6	BGE rel
F	MOV A,R7	CMP A,R7	ADDC A,R7	SUBC A,R7	MOV R7,A	XOR A,R7	AND A,R7	OR A,R7	MOV R7,#d8	CMP R7,#d8	SETB dir: 7	BBS dir: 7,rel	INC R7	DEC R7	CALLV #7	BLT rel

■ MASK OPTIONS

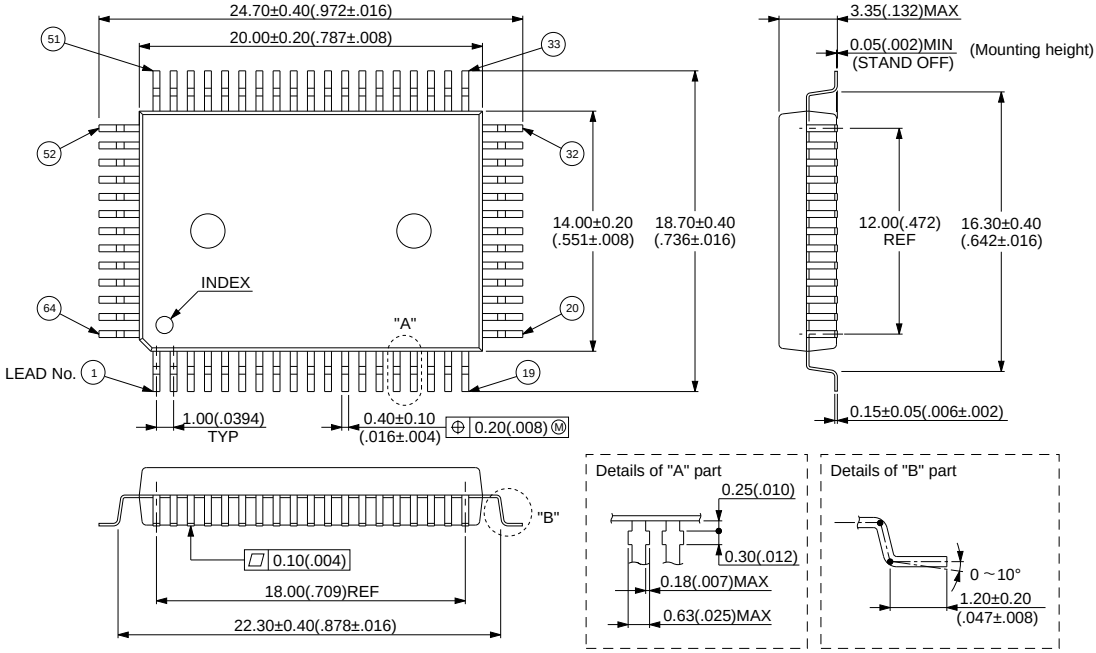
No.	Part number	MB89181/182/183	MB89P185	MB89PV180
	Specifying procedure	Specify when ordering masking	Set with EPROM programmer	Setting not possible
1	Pull-up resistors P00 to P07, P10 to P17	Can be set per pin (P10 to P17 are available only when segment output is not selected.)	Can be set per pin (P10 to P17 are available only when segment output is not selected.)	Fixed to without pull-up resistor
2	Pull-up resistors P40 to P47, P50 to P57	Can be set per pin (Available only when segment output is not selected.)	Fixed to without pull-up resistor	
3	Pull-up resistors P20 to P27	Can be set per pin	Fixed to without pull-up resistor	
4	Power-on reset 〈 With power-on reset Without power-on reset	Selectable	Selectable	Fixed to with power-on reset
5	Selection of oscillation stabilization delay time The initial value of the main clock oscillation stabilization time is selectable by bit value of WTM1 and WTM0.	Selectable WTM1 WTM0 0 0: $2^2/F_{CH}$ 0 1: $2^{12}/F_{CH}$ 1 0: $2^{16}/F_{CH}$ 1 1: $2^{18}/F_{CH}$	Selectable WTM1 WTM0 0 0: $2^2/F_{CH}$ 0 1: $2^{12}/F_{CH}$ 1 0: $2^{16}/F_{CH}$ 1 1: $2^{18}/F_{CH}$	Fixed to oscillation stabilization time of $2^{16}/F_{CH}$
6	Main clock oscillation type 〈 Crystal or ceramic oscillator CR	Selectable	Crystal or ceramic oscillator	Crystal or ceramic oscillator
7	Reset pin output 〈 With reset output Without reset output	Selectable	Selectable	With reset output
8	Clock mode selection 〈 Dual-clock mode Single-clock mode	Selectable	Selectable	Fixed to dual-clock mode
9	Segment output selection 32 segments:No port selection 28 segments:Selection of P17 to P14 24 segments: Selection of P17 to P10 20 segments:Selection of P17 to P10,and P57 to P54 16 segments:Selection of P17 to P10,and P57 to P50 12 segments:Selection of P17 to P10,P57 to P50, and P47 to P44 8 segments: Selection of P17 to P10,P57 to P50, and P47 to P40	Selectable Selects the number of segments.	-101: 32 segments -102: 28 segments -103: 24 segments -104: 20 segments -105: 16 segments -106: 12 segments -107: 8 segments	

■ ORDERING INFORMATION

Part number	Package	Remarks
MB89181PF MB89182PF MB89183PF MB89P185PF-101 MB89P185PF-102 MB89P185PF-103 MB89P185PF-104 MB89P185PF-105 MB89P185PF-106 MB89P185PF-107	64-pin Plastic QFP (FPT-64P-M06)	
MB89181FM MB89182FM MB89183FM MB89P185PFM-101 MB89P185PFM-102 MB89P185PFM-103 MB89P185PFM-104 MB89P185PFM-105 MB89P185PFM-106 MB89P185PFM-107	64-pin Plastic QFP (FPT-64P-M09)	
MB89181PFV MB89182PFV MB89183PFV	64-pin Plastic SQFP (FPT-64P-M03)	
MB89PV180CF-101 MB89PV180CF-102 MB89PV180CF-103 MB89PV180CF-104 MB89PV180CF-105 MB89PV180CF-106 MB89PV180CF-107	64-pin Ceramic MQFP (MQP-64C-P01)	

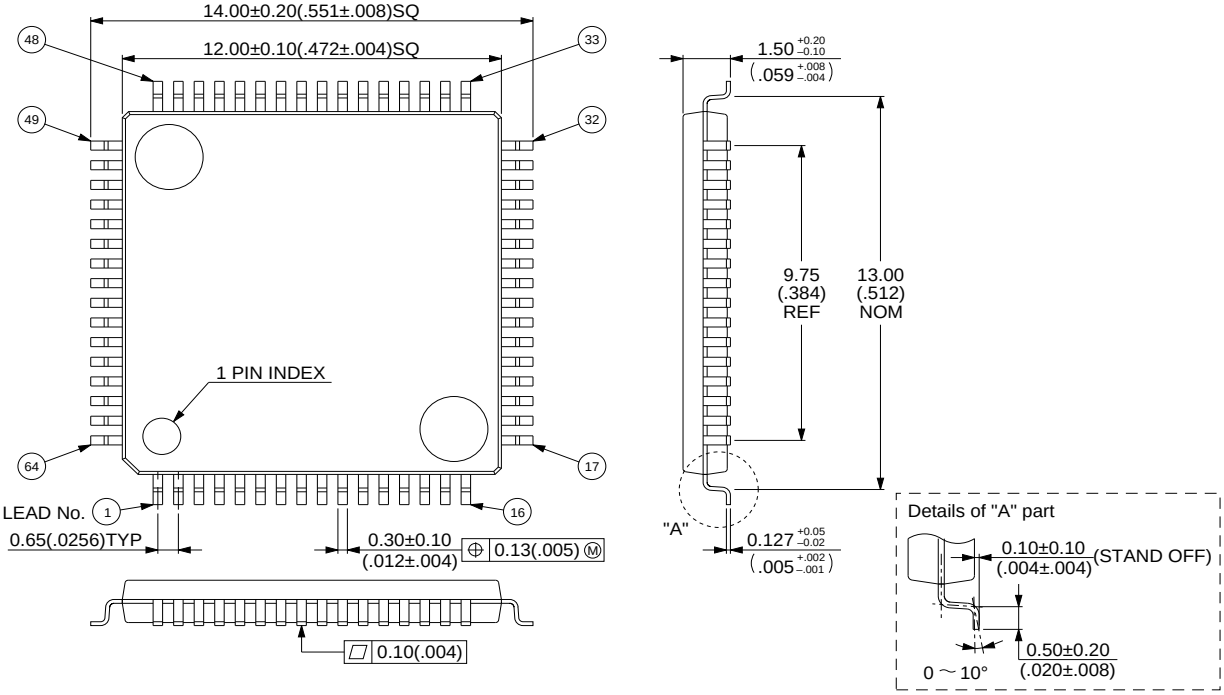
■ PACKAGE DIMENSIONS

64-pin Plastic QFP
(FPT-64P-M06)



Dimensions in mm (inches)

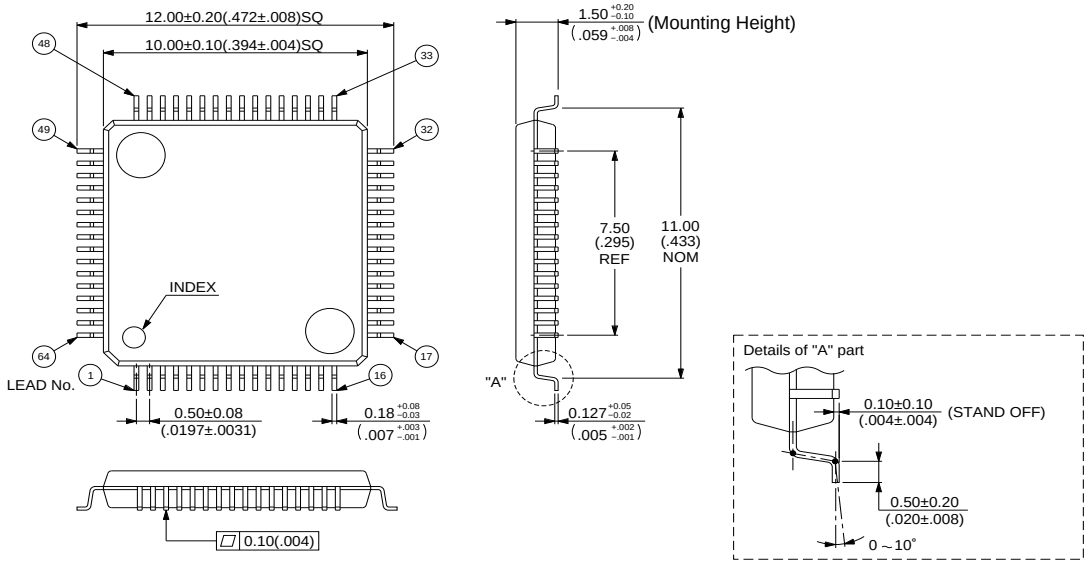
64 pin, Plastic QFP
(FPT-64P-M09)



Dimensions in mm (inches).

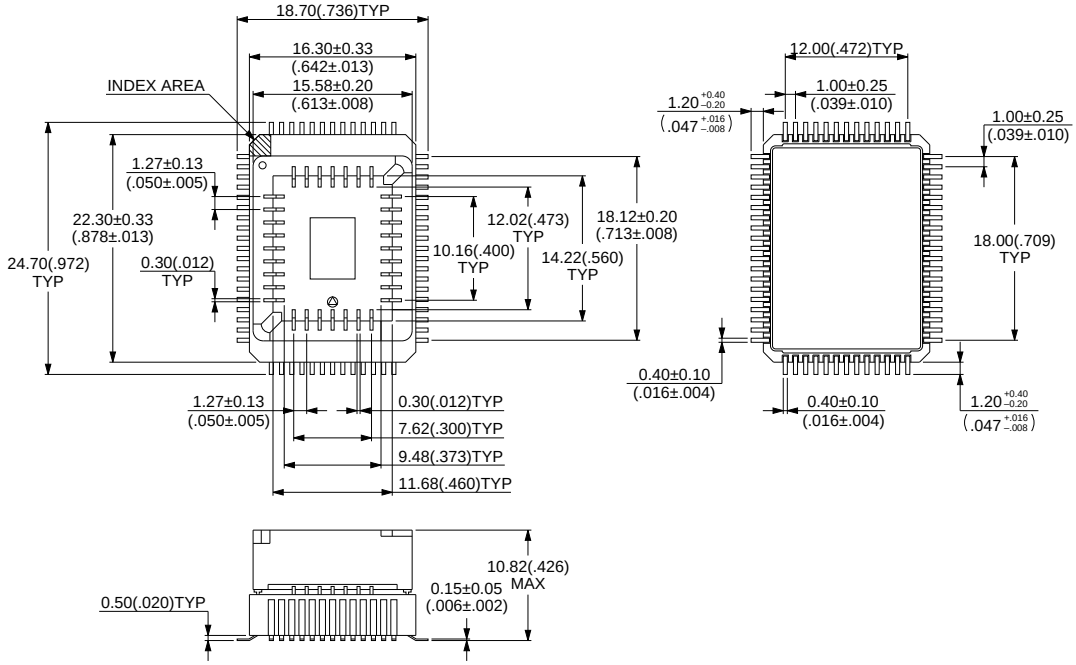
(Continued)

64 pin, PlasticLQFP
(FPT-64P-M03)



Dimensions in mm (inches).

64-pin Ceramic MQFP
(MQP-64C-P01)



Dimensions in mm (inches)

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