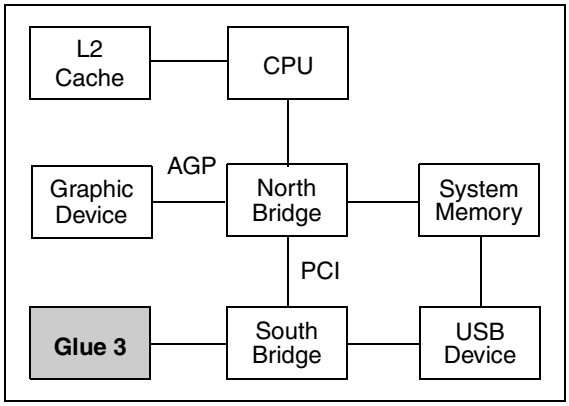
MB87B301BPD-G-ER

Glue 3 Logic Chip for Intel® 810 and 820 Chipsets

Description

Glue 3 is a third generation glue logic device for Intel® desktop boards using the Intel 810 chipset with Celeron™ processor or the Intel 820 chipset with Pentium® III processors. The Intel 820 chipset is targeted for desktop applications and it replaces the Intel BX chipset. The Intel 810 chipset is targeted for mobile applications.

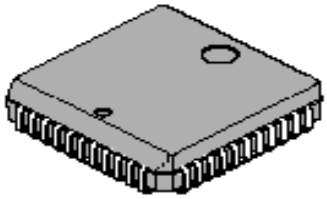


Intel® 820 Desktop Board Application

Features

Glue 3 replaces approximately 32 discrete logic components, saving significant space on the desktop board. It provides power management, LED, and fan control functions. The following functions are supported by this glue chip:

- Audio-disable circuit
- 5V reference generation
- FLUSH_OUT/INIT_OUT circuit
- CLK_IN (33 MHz or 66 MHz) input
- HD single color LED driver
- IDE reset signal generation/PCIRST# buffers
- PWROK signal generation
- Control circuitry for suspend to RAM
- Power supply power up circuitry
- RSMRST# generation
- Backfeed cutoff circuit for suspend to RAM
- Tri-state buffers for test
- Voltage translation for Audio MIDI signal
- Voltage translation for DDC for monitor
- Intel Part No. A05770-002
- 44-pin PLCC package in tape and reel only



Package Outline

- 44-pin Plastic QFJ (PLCC)
- LCC-44P-M02

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Pin Assignment

Pin	Signal	Type	Description	Pin	Signal	Type	Description
1	VREF3IN	3I	3.3V input	23	FLUSH_OUT*	5V OD	Open drain signal, goes to the CPU and FWH
2	5VSB	P (I)	5V system standby power supply	24	SEL_33_66*	3IU	Strapping option for 33 MHz or 66 MHz CLK_IN
3	3VSB	P (I)	3V system standby power supply	25	5V_DDCSDA	5IOD	DDCSDA input/output 5V side
4	GPO_FLUSH_CACHE*	3I	GPO from SIO/ICH	26	BACKFEED_CUT	5V OD	Signal used for STR circuitry
5	INIT*	3IU	Signal from the ICH	27	INIT_OUT*	5V OD	Delayed INIT* signal into the CPU
6	PCIRST*	3I	PCI reset signal	28	IDE_RSTDRV*	5O	IDE reset output, 5V push/pull
7	3V_DDCSCL	3IOD	DDCSCL input/output 3.3V side	29	LOGIC_OUTX	5V OD	NAND gate output
8	SLOTOCC*/CPU_PRESENT*	3IU	Slot occupied or CPU present signal from the processor	30	LOGIC_INA	5I	NAND gate input
9	HD_LED*	5V OD	Hard drive front panel LED output	31	H_PWRGD	5V OD	Open drain, power good output
10	CLK_IN	3I	Either 33 MHz or 66 MHz clock, based on SEL_33_66* pin	32	PWRGD_3V	3O	3.3V power good output
11	PCIRST_OUT*	3O	Copy of PCIRST*, increased drive-strength	33	SLP_S3A/PS_ON*	5V OD	Inverted copy of SLP_S3*, signal goes to power connector
12	PRIMARY_HD*	5IU	IDE primary drive active output	34	PWRGD_PS	5IU	Power good signal from power supply
13	SCSI*	5IU	SCSI drive active output	35	3V_DDCSDA	3IOD	DDCSDA input/output 3.3V side
14	SECONDARY_HD*	5IU	IDE secondary drive active output	36	FPRST*	5IU	Reset signal from the front panel
15	SLP_S5A	5O	Inverted copy of SLP_S5*	37	LOGIC_INB	5I	NAND gate input
16	AUD_RST*	3O	Audio reset output	38	5V_DDCSCL	5IOD	DDCSCL input/output 5V side
17	GND	G	Ground	39	SLP_S5*	3I	Signal from the ICH for transitioning to the S5 power state
18	AUD_MIDI_OUT	5O	5V audio MIDI signal to MIDI port	40	SLP_S3*	3I	Signal from the ICH for transitioning to the S3 power state
19	SCK_BJT_GATE	5V OD	Gate signal for the SCK BJT in suspend to RAM	41	RSMRST*	3O	Reset for the ICH resume well
20	AUD_DIS*	3I	Audio enable input	42	GND	G	Ground
21	AUD_MIDI_IN	5I	5V tolerant signal from the audio digital controller	43	REF5V	AO	Highest system supply reference voltage
22	TEST_EN	5ID	Test enable, 100K internal pull-down to GND	44	VREF5IN	5I	5V system primary supply input

Pin Type Legend

Type	Description
3I	3.3V input signal
3IU	3.3V input signal with internal pull-up
5I	5V input signal
5IU	5V input signal with internal pull-up
5ID	5V input signal with internal pull-down
P	Power (input)
G	Ground (input)
3O	3.3V output signal
5O	5V output signal
3V OD	3.3V open-drain output signal
5V OD	5V open-drain output signal
AO	Analog output
3IOD	3.3V input/output open drain
5IOD	5V input/output open drain

Absolute Maximum Ratings

Parameter	Symbol	Requirements	Rating		Unit
			Minimum	Maximum	
Supply voltage	V_{DD5}	5.0V power supply pins	V_{ss}*-0.5	6.0	V
	V_{DD3}	3.3V power supply pins	V_{ss}*-0.5	6.0	V
Input voltage	V_I		V_{ss}*-0.5	V_{DD}*+0.5	V
Output voltage	V_O		V_{ss}*-0.5	V_{DD}*+0.5	V
Storage ambient temperature	T_{ST}	Plastic package	-55	+125	°C
Supply pin current	I_D	For one V_{DD} pin	90		mA
		For one V_{ss} pin	90		mA
Output current	I_O	Low power-type output buffer I_{OL} = 2 mA	+14		mA
		Normal-type output buffer I_{OL} = 4 mA	±14		mA
		Power-type output buffer I_{OL} = 8 mA	±14		mA
		High-power type output buffer I_{OL} = 12 mA	±28		mA
		Double high-power type output buffer I_{OL} = 24 mA	±58		mA
Overshoot		For 50 ns maximum	V_{DD}+1.0V		
Undershoot		For 50 ns maximum	V_{ss}-1.0V		

Note: V_{SS} = 0, V_{DD} = 3 or 5V depending on the buffer

Recommended Operating Conditions (V_{DD3} = 3.3V ± 0.30V, V_{DD5} = 5.0V ± 0.25V)

Parameter		Symbol	Requirements			Unit
			Minimum	Typical	Maximum	
Supply voltage		V_{DD3}	3	3.3	3.6	V
		V_{DD5}	4.75	5	5.25	V
High-level input voltage	3.3V CMOS I/O	V_{IH1}	V_{DD3} x 0.7	-	V_{DD3}	V
	5.0V CMOS I/O	V_{IH2}	V_{DD5} x 0.7	-	V_{DD5}	V
	TTL I/O	V_{IH3}	2.2	-	V_{DD5}	V
Low-level input voltage	3.3V CMOS I/O	V_{IL1}	V_{ss}	-	V_{DD3} x 0.2	V
	5.0V CMOS I/O	V_{IL2}	V_{ss}	-	V_{DD5} x 0.3	V
	TTL I/O	V_{IL3}	V_{ss}	-	0.8	V
Ambient temperature		T_a	0	-	70	°C

Note: V_{SS} = 0

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PACKAGE

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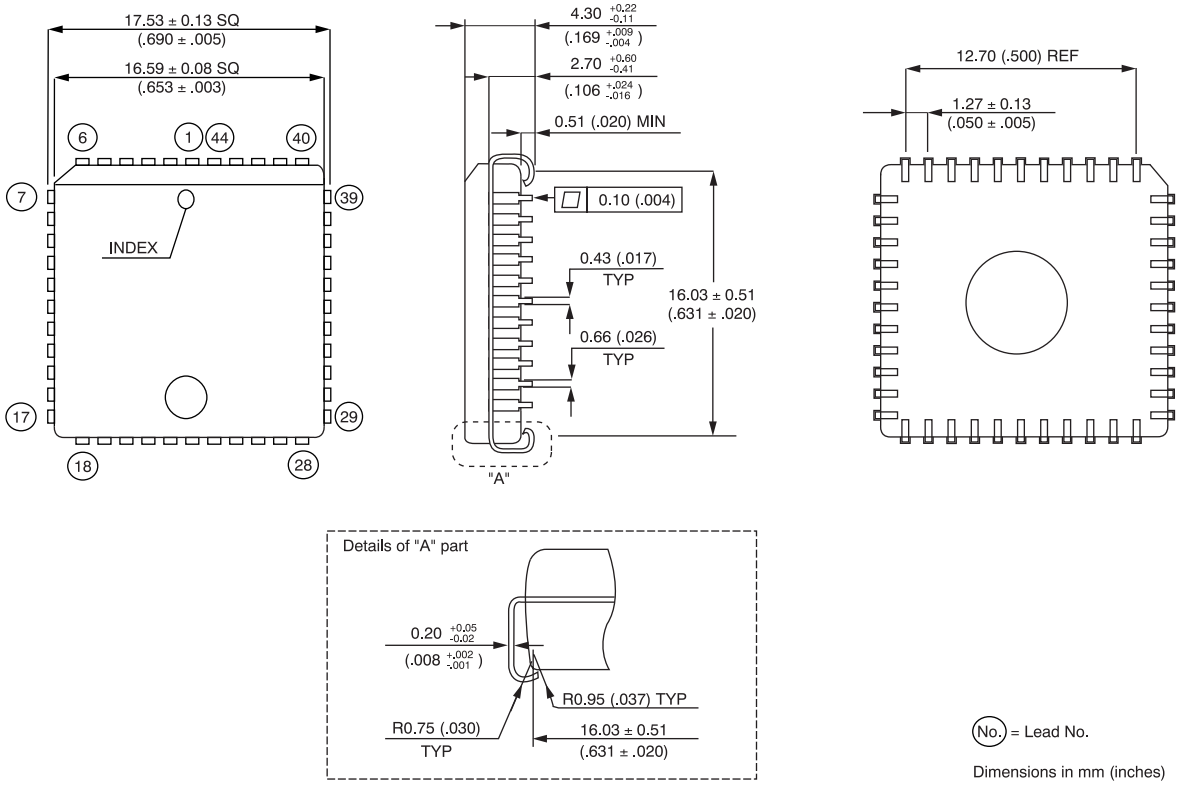

Specifications	
Lead Pitch	1.27 mm
Package Width x Package Length	16.59 ± 0.08 mm
Package Height (including standoff)	4.30 + 0.22 - 0.11 mm
Standoff Height	0.51 mm minimum
Lead Shape	J bend
Sealing Method	Plastic mold

Glue 3 is an application-specific glue logic device. It is designed specifically for Intel reference design desktop boards using the Intel 810 chipset with Celeron processor or the Intel 820 chipset with Pentium III processors (the “Target Application”).

Glue 3 has neither been designed nor tested for any other application. It is not intended for use with any other application. Buyers assume all risks and liabilities that occur from the use of Glue 3 for any purpose other than the Target Application.

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