MEMORY Mobile FCRAM™

CMOS

16M Bit (1M word x 16 bit)

Mobile Phone Application Specific Memory

MB82D01161-85/-85L/-90/90L

CMOS 1,048,576-WORD x 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

The Fujitsu MB82D01161 is a CMOS Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. This MB82D01161 is suited for low power applications such as Cellular Handset and PDA.

■ FEATURES

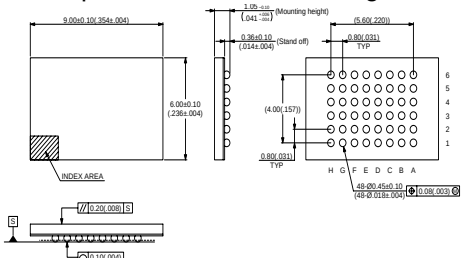
- Asynchronous SRAM Interface
- 1M word ×16bit Organization
- Fast Random Cycle Time:
  t_{RC} = 90ns
- Fast Random Access Time
  t_{AA} = t_{CE} = 85ns (-85), 90ns (-90)
- Low Power Consumption:
  I_{DDS1} = 200µA, 100µA (L version)
- Wide Operating Conditions:
  V_{DD} = +2.3V to +2.7V
  +2.7V to +3.1V
  +3.1V to +3.5V
  T_A = -30ºC to +85ºC
- Byte Write Control
- Power Down Control by CE2

■ PRODUCT LINE

	MB82D01161			
	85	**85L**	**90**	**90L**
Access Time (t_{AA} Max. & t_{CE} Max.)	85ns		90ns	
Active Current (I_{DDA1} Max.)	20mA			
Stabdby Current (I_{DDS1} Max.)	200µA	100µA	200µA	100µA
Power Down Current (I_{DDP} Max.)	10µA			

■ PACKAGE

48-pin Plastic FBGA Package



(BGA-48P-M16) (BGA-48P-M18)

Notice: FCRAM is a trademark of Fujitsu Limited, Japan.

■ PIN ASSIGNMENT

(TOP VIEW)

Flash Compatible FBGA
(suffix PBT)

	1	2	3	4	5	6
A	A4	A17	$\overline{UB}$	CE2	A8	A12
B	A3	A7	$\overline{LB}$	$\overline{WE}$	A9	A13
C	A2	A6	A18	NC	A10	A14
D	A1	A5	NC	A19	A11	A15
E	A0	DQ1	DQ3	DQ6	DQ8	A16
F	$\overline{CE1}$	DQ9	DQ11	DQ13	DQ15	NC
G	$\overline{OE}$	DQ10	DQ12	V_{DD}	DQ14	DQ16
H	V_{SS}	DQ2	DQ4	DQ5	DQ7	V_{SS}

(BGA-48P-M16)

SRAM Compatible FBGA
(suffix PBN)

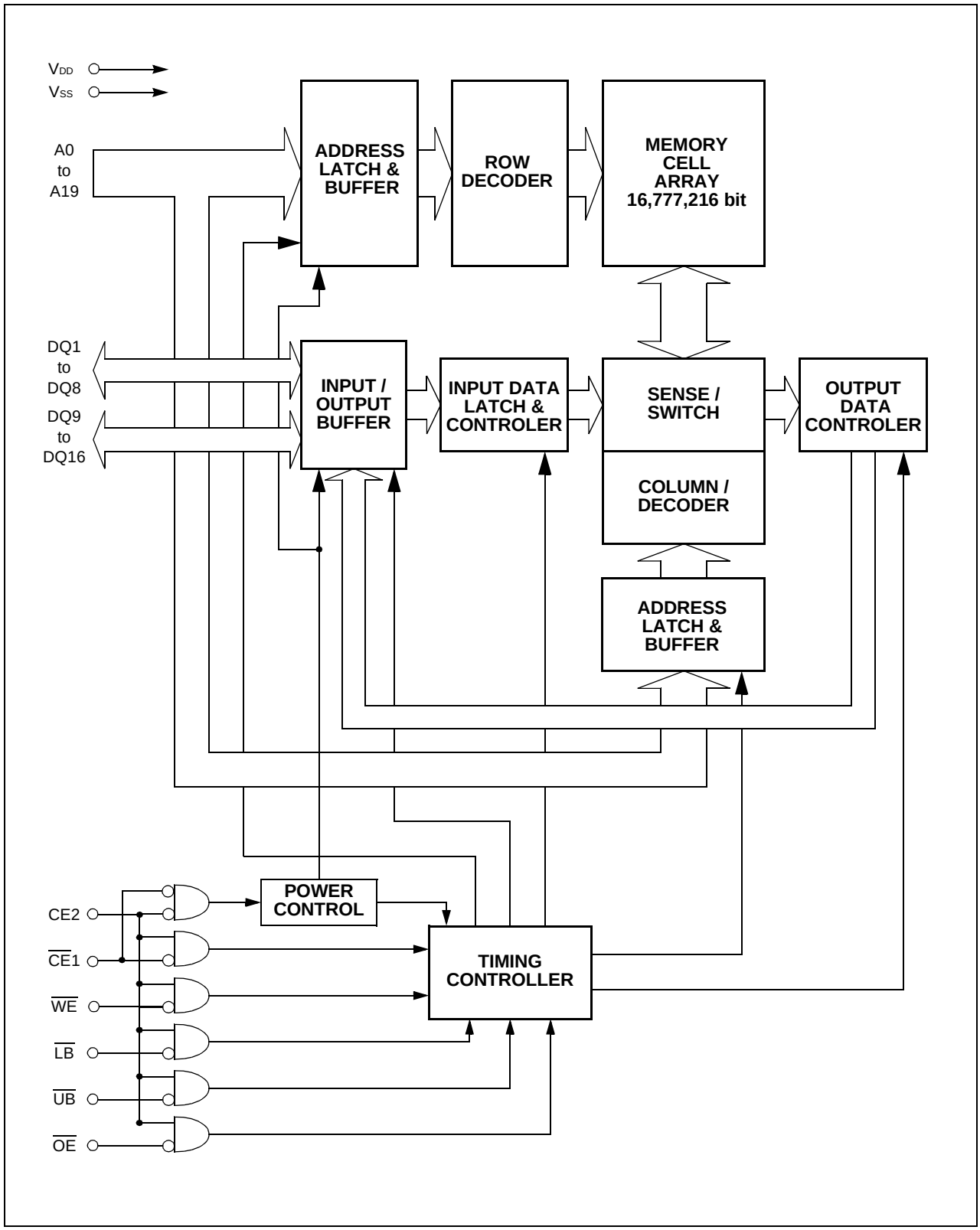
	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	DQ9	$\overline{UB}$	A3	A4	$\overline{CE1}$	DQ1
C	DQ10	DQ11	A5	A6	DQ2	DQ3
D	V_{SS}	DQ12	A17	A7	DQ4	V_{DD}
E	V_{DD}	DQ13	NC	A16	DQ5	V_{SS}
F	DQ15	DQ14	A14	A15	DQ6	DQ7
G	DQ16	A19	A12	A13	$\overline{WE}$	DQ8
H	A18	A8	A9	A10	A11	NC

(BGA-48P-M18)

■ PIN DESCRIPTION

Pin Name	Description
A_0 to A_{19}	Address Input
$\overline{CE1}$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Write Control (Low Active)
$\overline{UB}$	Upper Byte Write Control (Low Active)
DQ_{1-8}	Lower Byte Data Input/Output
DQ_{9-16}	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE *1

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ1-8	DQ9-16	I_{DD}	Data Retention
Power Down	L	L	X	X	X	X	High-Z	High-Z	I_{DDP}	No
Standby (Deselect)	H	L	X	X	X	X	High-Z	High-Z	I_{DDS}	No
		H	X	X	X	X				Yes
Output Disable *2	L	H	H	H	X	X	High-Z	High-Z	I_{DDA}	Yes
Read *3	L	H	H	L	X	X	Output Valid	Output Valid	I_{DDA}	Yes
Write	L	H	L	H	L	L	Input Valid	Input Valid	I_{DDA}	Yes
Write (Upper Byte)	L	H	L	H	L	H	Input Valid	Invalid	I_{DDA}	Yes
Write (Lower Byte)	L	H	L	H	H	L	Invalid	Input Valid	I_{DDA}	Yes

*1: L = VIL, H = VIH, X can be either VIL or VIH, High-Z = High Impedance

*2: Output Disable condition should not be kept longer than 1μs.

*3: Byte control at Read operation is not supported.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.6	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +3.6	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Max.	Unit
Supply Voltage	*1	$V_{DD\ (31)}$	3.1	3.5	V
		$V_{DD\ (27)}$	2.7	3.1	V
		$V_{DD\ (23)}$	2.3	2.7	V
		V_{SS}	0	0	V
High Level Input Voltage	*1,*2	$V_{IH\ (31)}$	2.6	V_{DD}+0.3 and ≤ 3.6V	V
		$V_{IH\ (27)}$	2.3	V_{DD}+0.3	V
		$V_{IH\ (23)}$	2.0	V_{DD}+0.3	V
Low Level Input Voltage	*1,*2	V_{IL}	-0.3	0.4	V
Ambient Temperature		T_A	-30	85	°C

Notes: *1: All voltages are referenced to V_{SS}.
*2: Minimum DC voltage on input or I/O pins are -0.3V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0V for periods of up to 5ns. Maximum DC voltage on input and I/O pins are V_{DD}+0.3V. During voltage transitions, outputs may positive overshoot to V_{DD}+1.0V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PACKAGE PIN CAPACITANCE

Symbol	Description	Test Setup	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0V	—	5	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics *1,*2,*3

Parameter		Symbol	Test Conditions		Min.	Max.	Unit
Input Leakage Current		I_{LI}	V_{IN} = V_{SS} to V_{DD}		-1.0	+1.0	µA
Output Leakage Current		I_{LO}	V_{OUT} = V_{SS} to V_{DD}, Output Disable		-1.0	+1.0	µA
Output High Voltage Level		V_{OH}	I_{OH} = –0.5mA		1.8	—	V
Output Low Voltage Level		V_{OL}	I_{OL} = 1mA		—	0.4	V
V_{DD} Power Down Current		I_{DDP}	V_{DD} = $V_{DD(31)}$ max., V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DD} – 0.2V, $\overline{CE1}$ = CE2 ≤ 0.2V, I_{OUT}=0mA		—	20	µA
			V_{DD} = $V_{DD(27, 23)}$ max., V_{IN} ≤ 0.2V or V_{IN} ≥ V_{DD} – 0.2V, $\overline{CE1}$ = CE2 ≤ 0.2V, I_{OUT}=0mA		—	10	µA
V_{DD} Standby Current		I_{DDS}	V_{DD} = $V_{DD(31)}$ max., V_{IN} = V_{IH} or V_{IL} CE2 = V_{IL} or $\overline{CE1}$ = CE2 = V_{IH}, I_{OUT}=0mA		—	2.5	mA
	L version				—	2.0	
			V_{DD} = $V_{DD(27, 23)}$ max., V_{IN} = V_{IH} or V_{IL} CE2 = V_{IL} or $\overline{CE1}$ = CE2 = V_{IH}, I_{OUT}=0mA		—	2.0	mA
	L version				—	1.5	
		I_{DDS1}	V_{DD} = $V_{DD(31)}$ max., V_{IN} ≤ 0.2V or $\overline{V_{IN}}$ ≥ V_{DD} – 0.2V, CE2 ≤ 0.2V or, $\overline{CE1}$ = CE2 ≥ V_{DD} – 0.2V, I_{OUT}=0mA		—	250	µA
	L version				—	150	
			V_{DD} = $V_{DD(27, 23)}$ max., V_{IN} ≤ 0.2V or $\overline{V_{IN}}$ ≥ V_{DD} – 0.2V, CE2 ≤ 0.2V or, $\overline{CE1}$ = CE2 ≥ V_{DD} – 0.2V, I_{OUT}=0mA		—	200	µA
	L version				—	100	
V_{DD} Active Current		I_{DDA1}	V_{DD} = $V_{DD(31)}$ max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	25	mA
		I_{DDA2}		t_{RC} / t_{WC} = maximum	—	4.0	mA
		I_{DDA1}	V_{DD} = $V_{DD(27, 23)}$ max., V_{IN} = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	20	mA
		I_{DDA2}		t_{RC} / t_{WC} = maximum	—	3.0	mA

Notes: *1: All voltages are referenced to Vss.

*2: DC Characteristics are measured after following POWER-UP timing.

*3: I_{DDA} depends on the output load conditions.

2. AC Characteristics

(1) Read Operation

Parameter	Symbol	-85/-85L		-90/-90L		Unit	Notes
		Min.	Max.	Min.	Max.		
Read Cycle Time	t_{RC}	90	1000	90	1000	ns	*1
Address Setup Time at $\overline{CE}$1 High to Low Transition	t_{ASC}	–5	—	–5	—	ns	
Address Hold Time during $\overline{CE}$1 Low	t_{AHC}	90	—	90	—	ns	*2
Address Access Time	t_{AA}	—	85	—	90	ns	*3
Chip Enable Access Time	t_{CE}	—	85	—	90	ns	*3
Output Enable Access Time	t_{OE}	—	60	—	60	ns	*3
Output Data Hold Time	t_{OH}	5	—	5	—	ns	*3
$\overline{CE}$1 Low to Output Low-Z	t_{CLZ}	10	—	10	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	0	—	ns	*4
$\overline{CE}$1 High to Output High-Z	t_{CHZ}	—	25	—	25	ns	*4
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	15	—	15	ns	*4
$\overline{CE}$1 High Pulse Width	t_{CP}	10	—	10	—	ns	
$\overline{CE}$1 High to Address Hold Time	t_{CHAH}	–5	—	–5	—	ns	*5
Address Invalid Time during Read ($\overline{CE}$1=Low)	t_{AX}	—	10	—	10	ns	

Notes: *1: Maximum value is a reference and is applied to Output Disable condition.

*2: t_{AHC} must be satisfied every address valid state after t_{AX} during $\overline{CE}$1=Low.

*3: The output load is 30pF.

*4: The output load is 5pF.

*5: If actual address change before $\overline{CE}$1 High transition is earlier than t_{CHAH} (min), t_{CP} ($\overline{CE}$1 High period) should be kept at least t_{RC} (min) period.

2. AC Characteristics (Continued)

(2) Write Operation

Parameter	Symbol	-85/-85L		-90/-90L		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Cycle Time	t_{WC}	90	1000	90	1000	ns	*1
Address Setup Time	t_{AS}	0	—	0	—	ns	
Address Hold Time	t_{AH}	40	—	40	—	ns	
$\overline{CE}1$ Write Setup Time	t_{CS}	0	1000	0	1000	ns	*2
$\overline{CE}1$ Write Hold Time	t_{CH}	0	1000	0	1000	ns	*2
$\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	0	—	0	—	ns	
$\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Hold Time	t_{BH}	0	—	0	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	0	—	0	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	15	—	15	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time	t_{OHCL}	–5	—	–5	—	ns	*3
$\overline{OE}$ High to Address Hold Time	t_{OHAH}	0	—	0	—	ns	*4
$\overline{CE}1$ Write Pulse Width	t_{CW}	60	—	60	—	ns	*5, *6
$\overline{WE}$ Write Pulse Width	t_{WP}	60	—	60	—	ns	*5, *6
$\overline{CE}1$ Write Recovery Time	t_{WRC}	15	—	15	—	ns	*7
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	15	1000	ns	*2, *7
Data Setup Time	t_{DS}	20	—	20	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	ns	
$\overline{CE}1$ Low to Output in Low-Z	t_{CLZ}	10	—	10	—	ns	*8
$\overline{OE}$ Low to Output in Low-Z	t_{OLZ}	0	—	0	—	ns	*8

Notes: *1: Minimum value must be equal or greater than the sum of actual write pulse width (t_{CW} or t_{WP}) and write recovery time (t_{WRC} or t_{WR}).
Maximum value is a reference and applied to Output Disable condition.

*2: Maximum value is applied to Output Disable condition.

*3: t_{OHCL} (min) must be satisfied if read operation is not performed prior to write operation.
In case $\overline{OE}$ is disabled after t_{OHCL} (min), $\overline{WE}$ Low must be asserted after t_{RC} (min) from $\overline{CE}1$ Low.

*4: Applicable if $\overline{CE}1$ stays Low after read operation.

*5: t_{WHP} (max) must be satisfied for the high pulse noise.

*6: t_{CW} and t_{WP} are applied if write operation is initiated by $\overline{CE}1$ and $\overline{WE}$, respectively.

*7: t_{WRC} and t_{WR} are applied if write pulse is terminated by $\overline{CE}1$ and $\overline{WE}$, respectively.

*8: The output load is 5pF.

2. AC Characteristics (Continued)

(3) Power Down Parameter

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
CE2 Low Setup Time for Power Down Entry	t_{CSP}	100	—	ns	
$\overline{CE}$1 Low Pulse Width during Power Down mode	t_{CPP}	100	—	ns	
CE2 Low Hold Time after Power Down Exit ($\overline{CE}$1 = High)	t_{C2LP}	350	—	µs	*1
$\overline{CE}$1 High Hold Time following CE2 High after Power Down Exit	t_{C1HP}	300	—	µs	*2

Notes: *1: Requires at least two dummy read cycles.
*2: Required when dummy read cycles are not performed.

(4) Other Timing Parameter

Parameter	Symbol	Value		Unit	Note
		Min.	Max.		
$\overline{CE}$1 High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}$1 High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	20	—	ns	
$\overline{CE}$1 and CE2 Active Glitch Pulse Width	t_{CAP}	—	5	ns	*1
$\overline{CE}$1 or $\overline{WE}$ High Glitch Pulse Width during Write Cycle	t_{WHP}	—	5	ns	*2
CE2 Low Hold Time after Power-up	t_{C2LP}	350	—	µs	*3
$\overline{CE}$1 High Hold Time following CE2 High after Power-up	t_{C1HP}	300	—	µs	*4

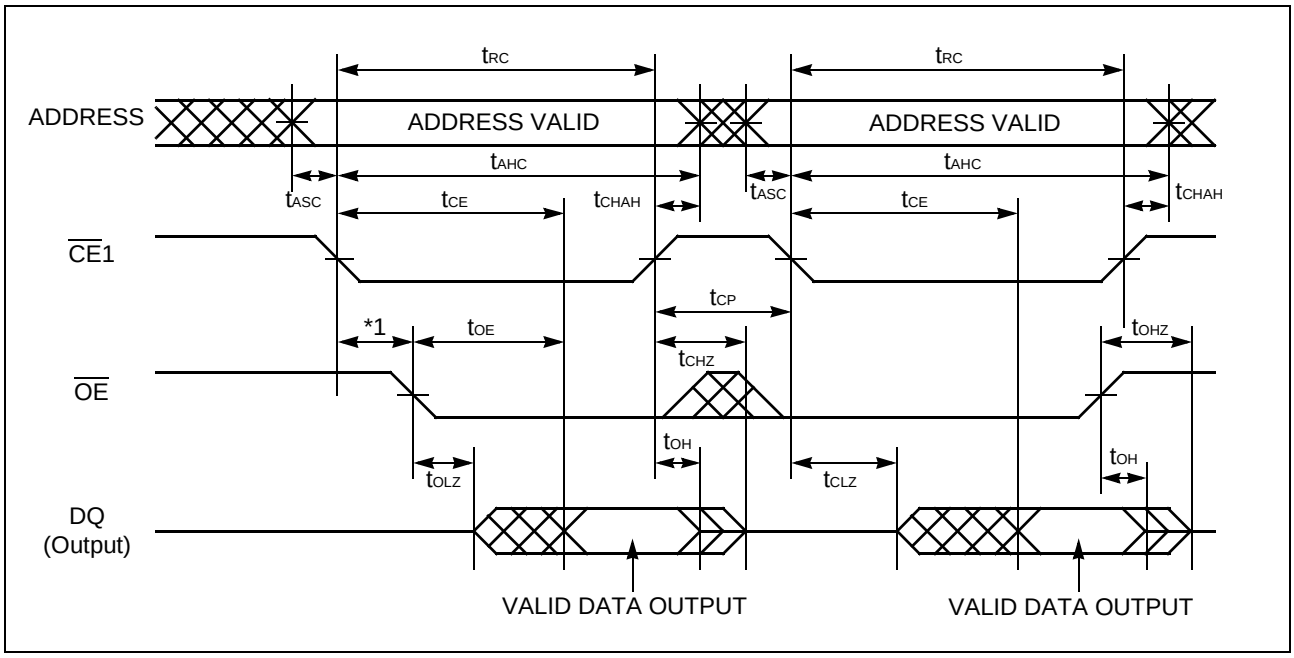
Notes: *1: Active means a condition where $\overline{CE}$1 = V_{IL} and CE2 =V_{IH}.
*2: Specified to the one time high pulse width during t_{CW} or t_{WP} and excluded 10ns from beginning and ending of the write cycle.
*3: Requires at least two dummy read cycles.
*4: Required when dummy read cycles are not performed.

(5) AC Test Conditions

Symbol	Description	Test Setup	Value	Unit
V_{IH}	Input High Level	V_{DD} = 3.1V to 3.5V	2.6	V
		V_{DD} = 2.7V to 3.1V	2.3	
		V_{DD} = 2.3V to 2.7V	2.0	
V_{IL}	Input Low Level	—	0.4	V
V_{REF}	Input Timing Measurement Level	V_{DD} = 3.1V to 3.5V	1.5	V
		V_{DD} = 2.7V to 3.1V	1.3	V
		V_{DD} = 2.3V to 2.7V	1.1	V
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns

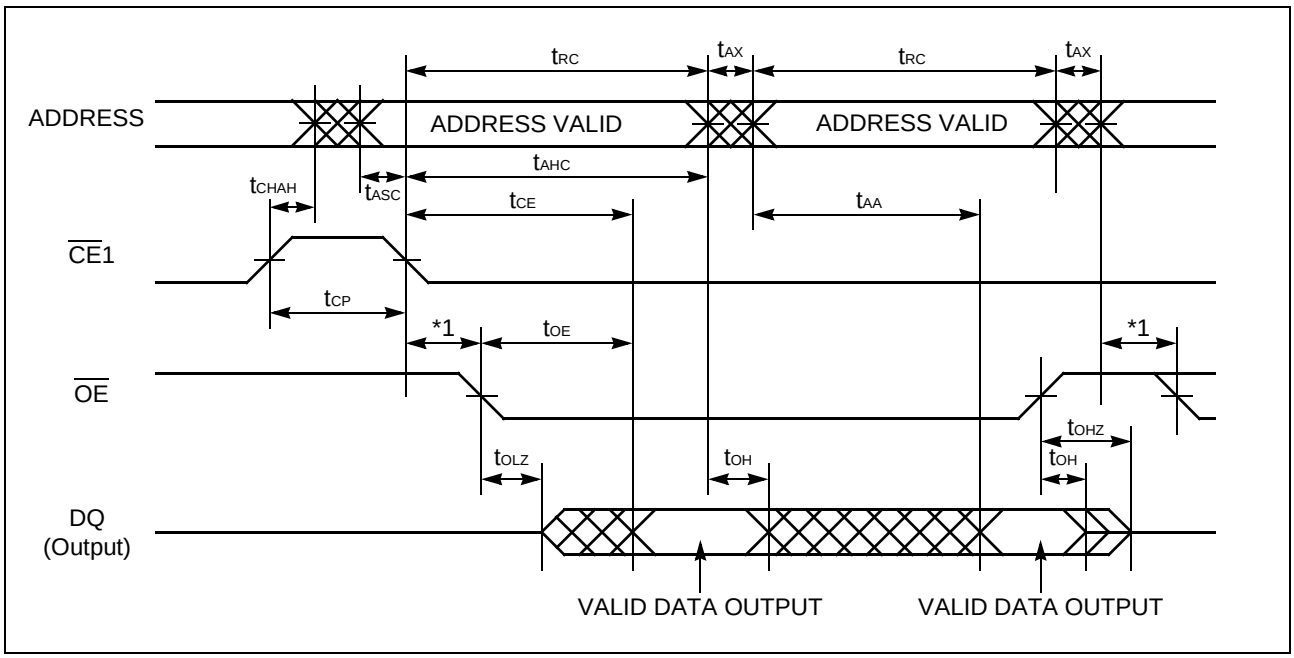
■ TIMING DIAGRAMS

1. READ Timing #1 ($\overline{CE}$1 Control)



Note: CE2 and $\overline{WE}$ must be HIGH for entire read cycle.
*1: Output Disable condition before new Read data valid should not be kept longer than 1µs.

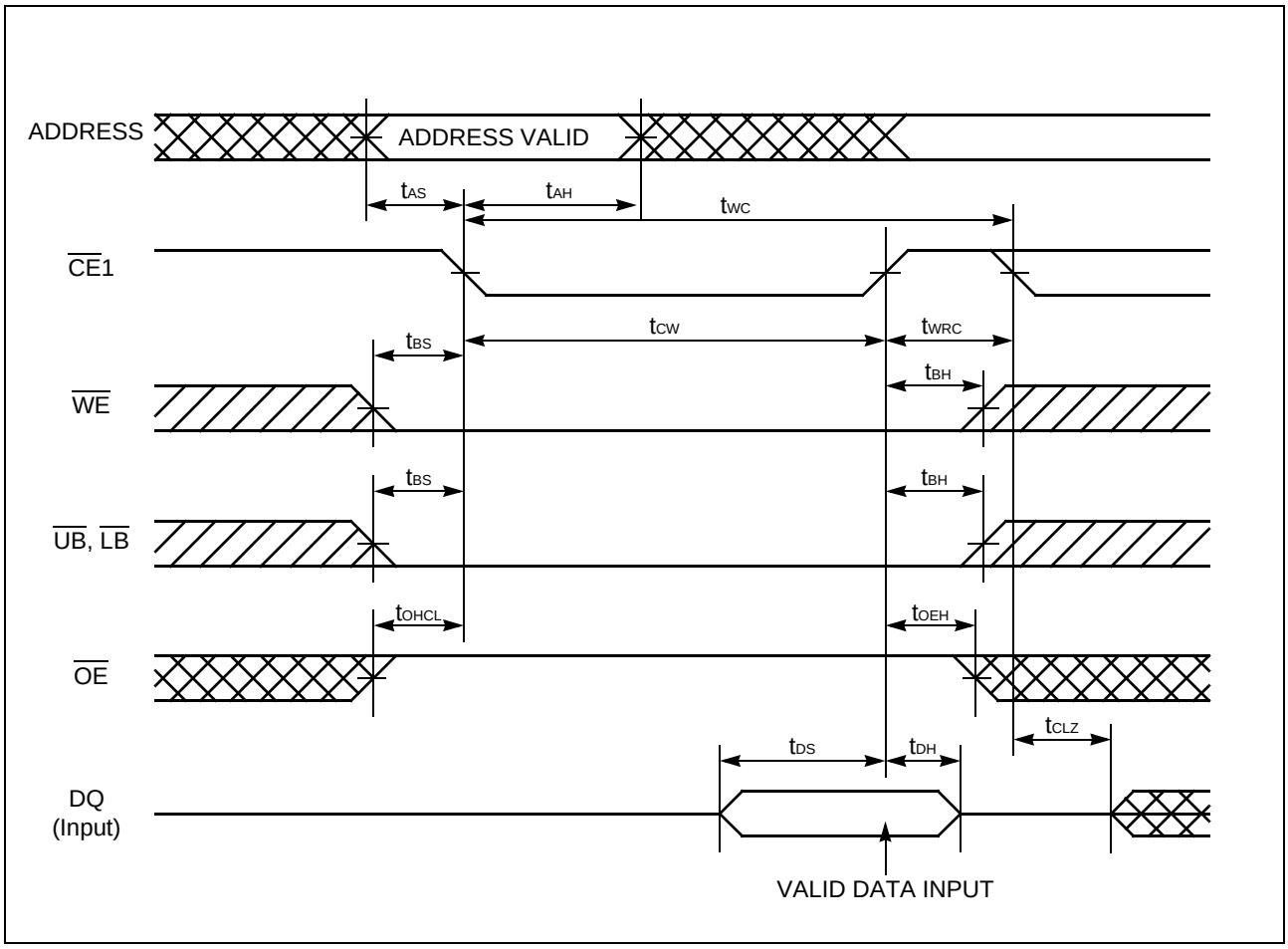
2. READ Timing #2 (Address Access)



Note: CE2 and $\overline{WE}$ must be HIGH for entire read cycle.
*1: Output Disable condition before new Read data valid should not be kept longer than 1µs.

■ TIMING DIAGRAMS (Continued)

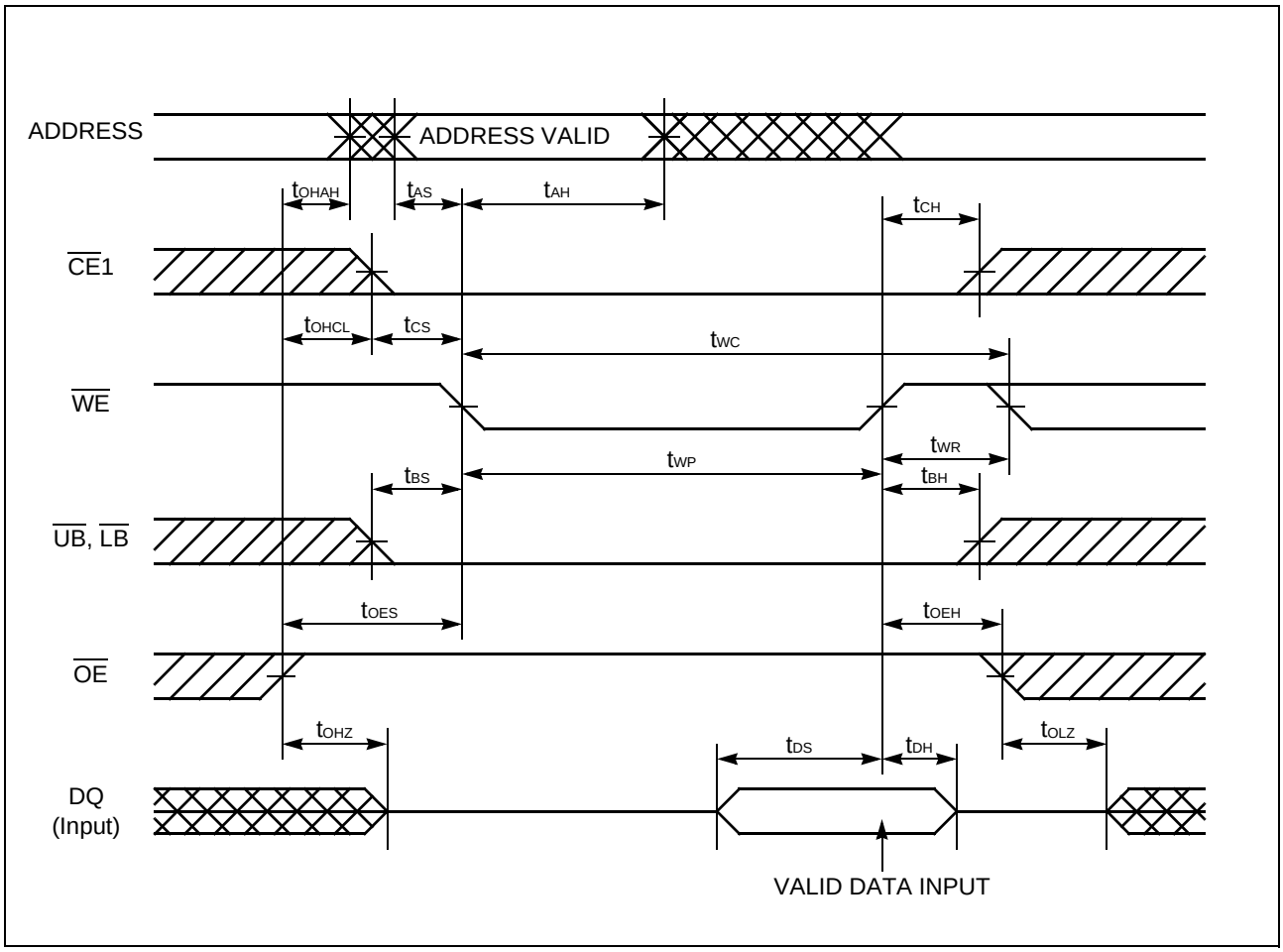
3. WRITE Timing #1 ($\overline{CE}$1 Control)



Note: CE2 must be HIGH for write cycle.

■ TIMING DIAGRAMS (Continued)

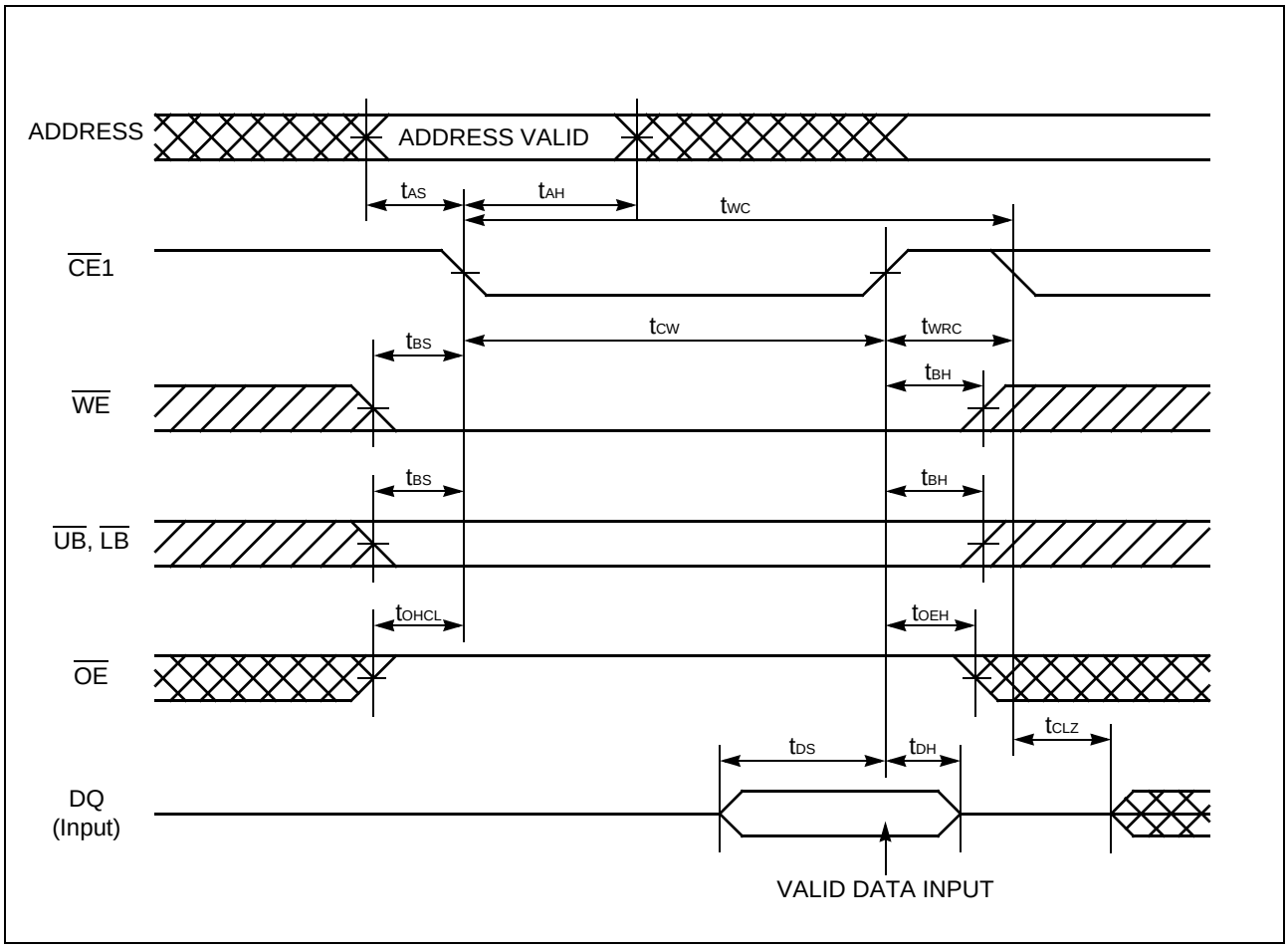
4. WRITE Timing #2 ($\overline{WE}$ Control)



Note: CE2 must be HIGH for write cycle.

■ TIMING DIAGRAMS (Continued)

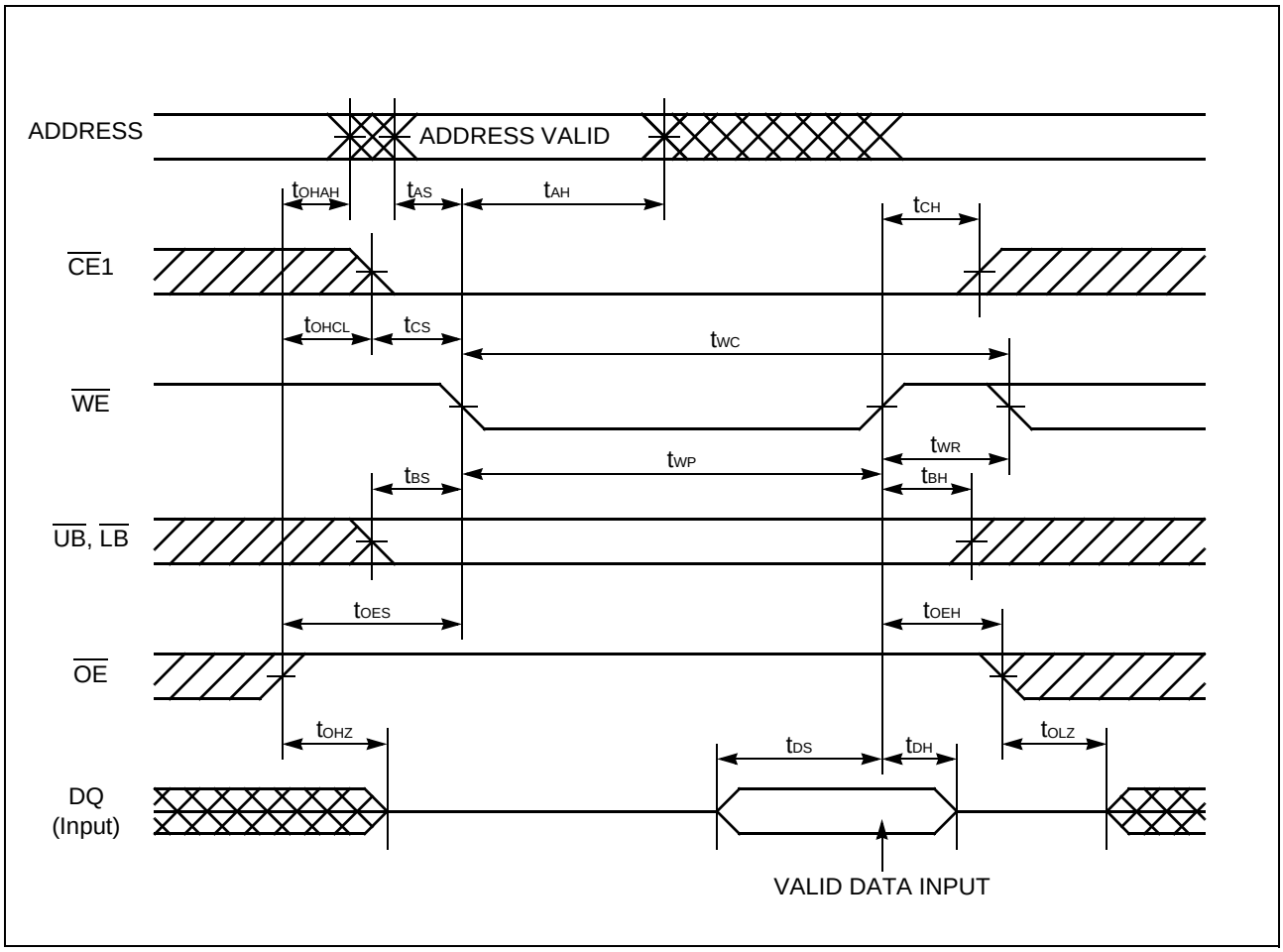
5. BYTE WRITE Timing #1 ($\overline{CE}$1 Control)



Note: CE2 must be HIGH and either $\overline{LB}$ or $\overline{UB}$ must be LOW for byte write cycle.

■ TIMING DIAGRAMS (Continued)

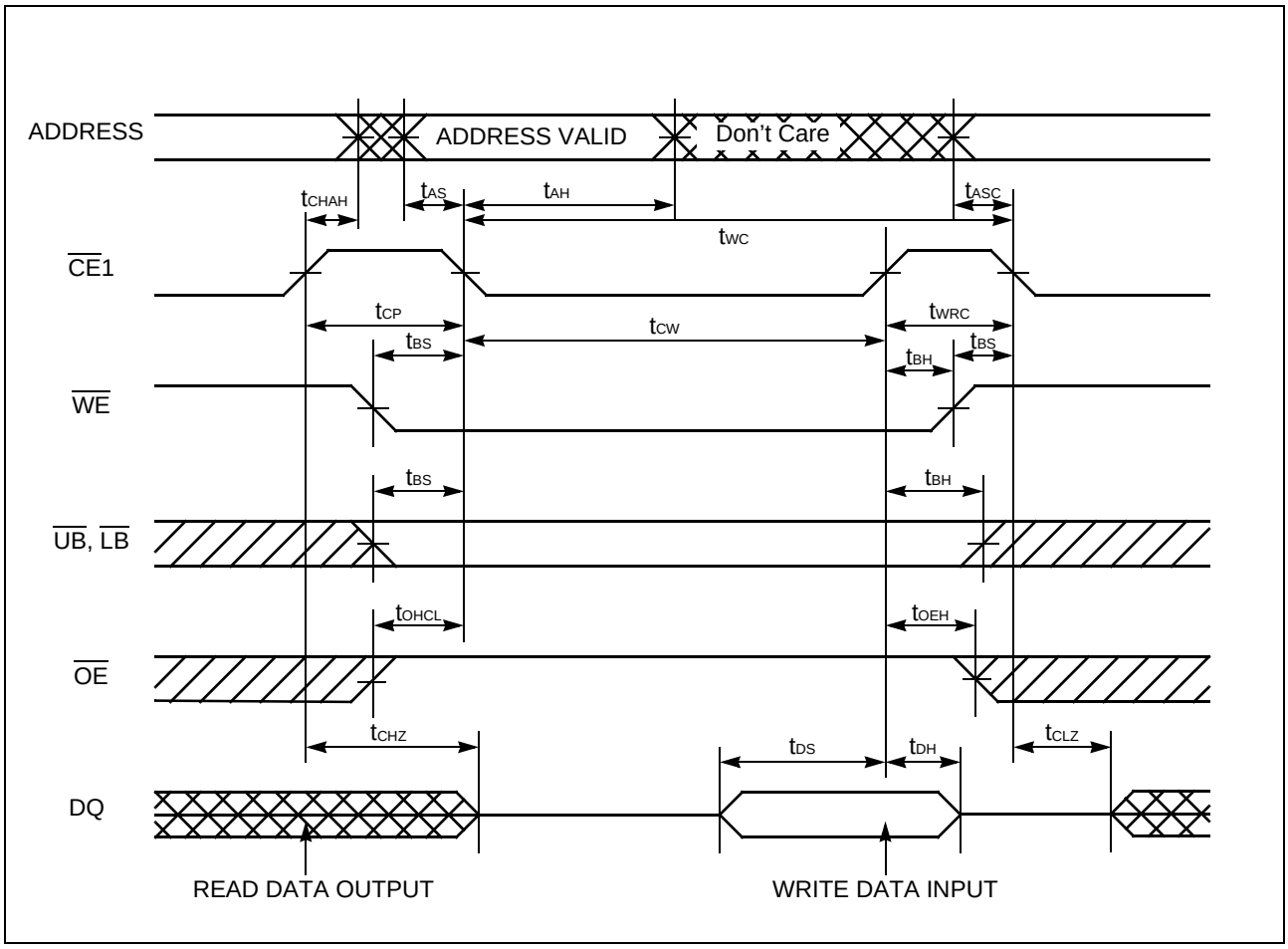
6. BYTE WRITE Timing #2 ($\overline{WE}$ Control)



Note: CE2 must be HIGH and either $\overline{LB}$ or $\overline{UB}$ must be LOW for byte write cycle.

■ TIMING DIAGRAMS (Continued)

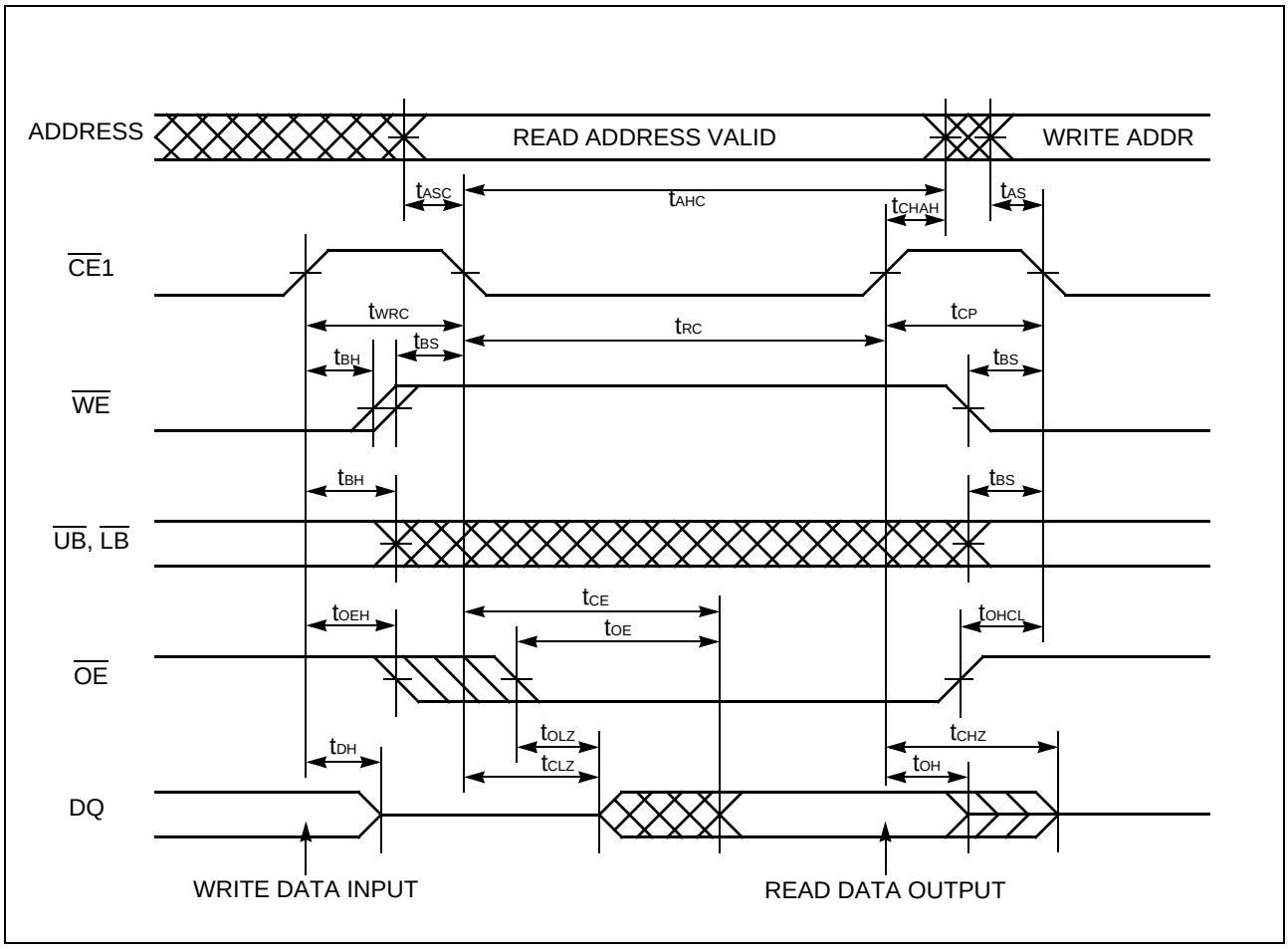
7. READ / WRITE Timing #1-1 ($\overline{CE}$ Control)



Note: Write address is edge trigger of either $\overline{CE}$1 or $\overline{WE}$ falling edge.

■ TIMING DIAGRAMS (Continued)

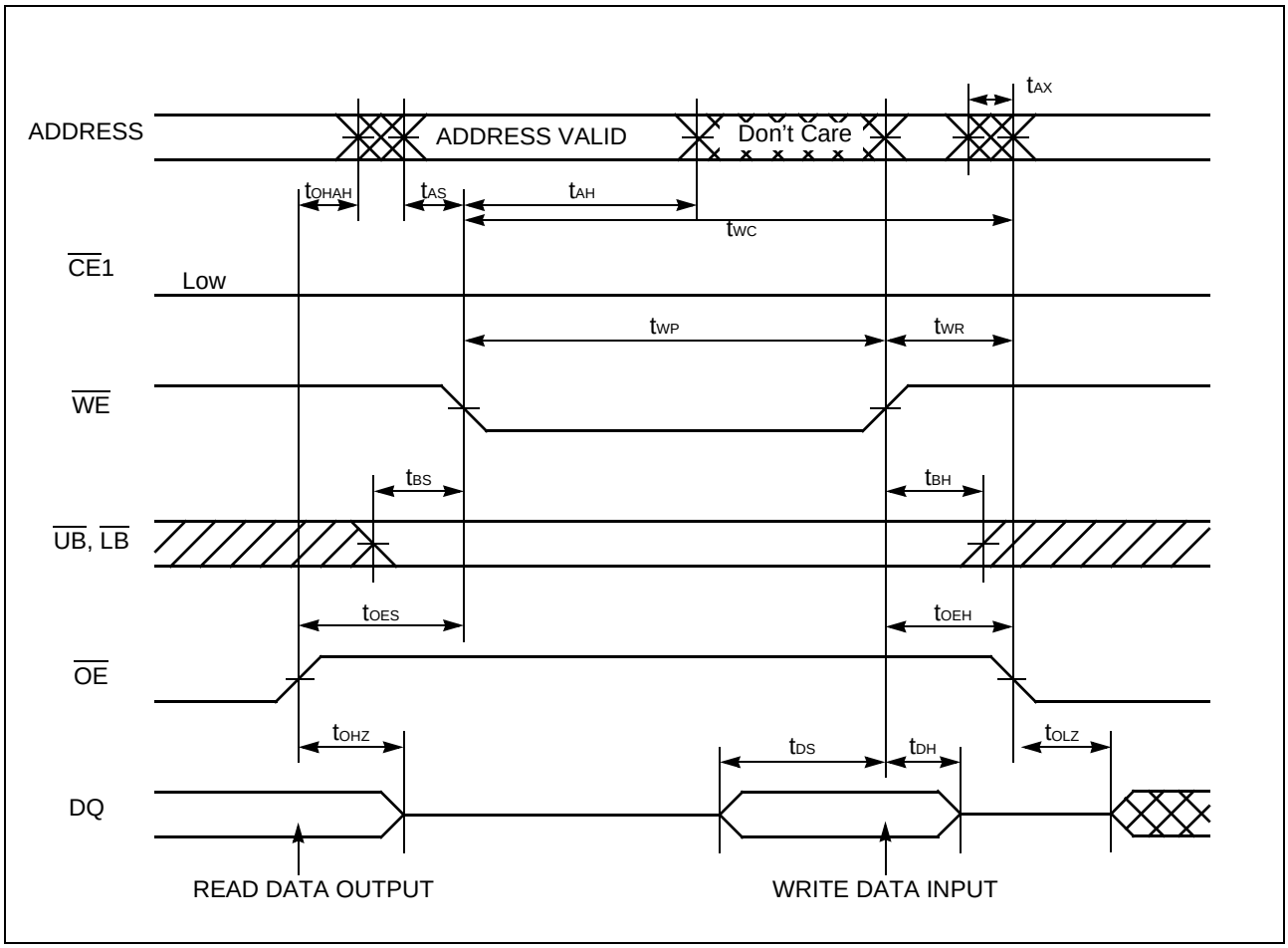
8. READ / WRITE Timing #1-2 ($\overline{CE}$ Control)



Note: $\overline{WE}$ must be HIGH for read cycle.

■ TIMING DIAGRAMS (Continued)

9. READ / WRITE Timing #2-1 ($\overline{OE}$ and $\overline{WE}$ Control)

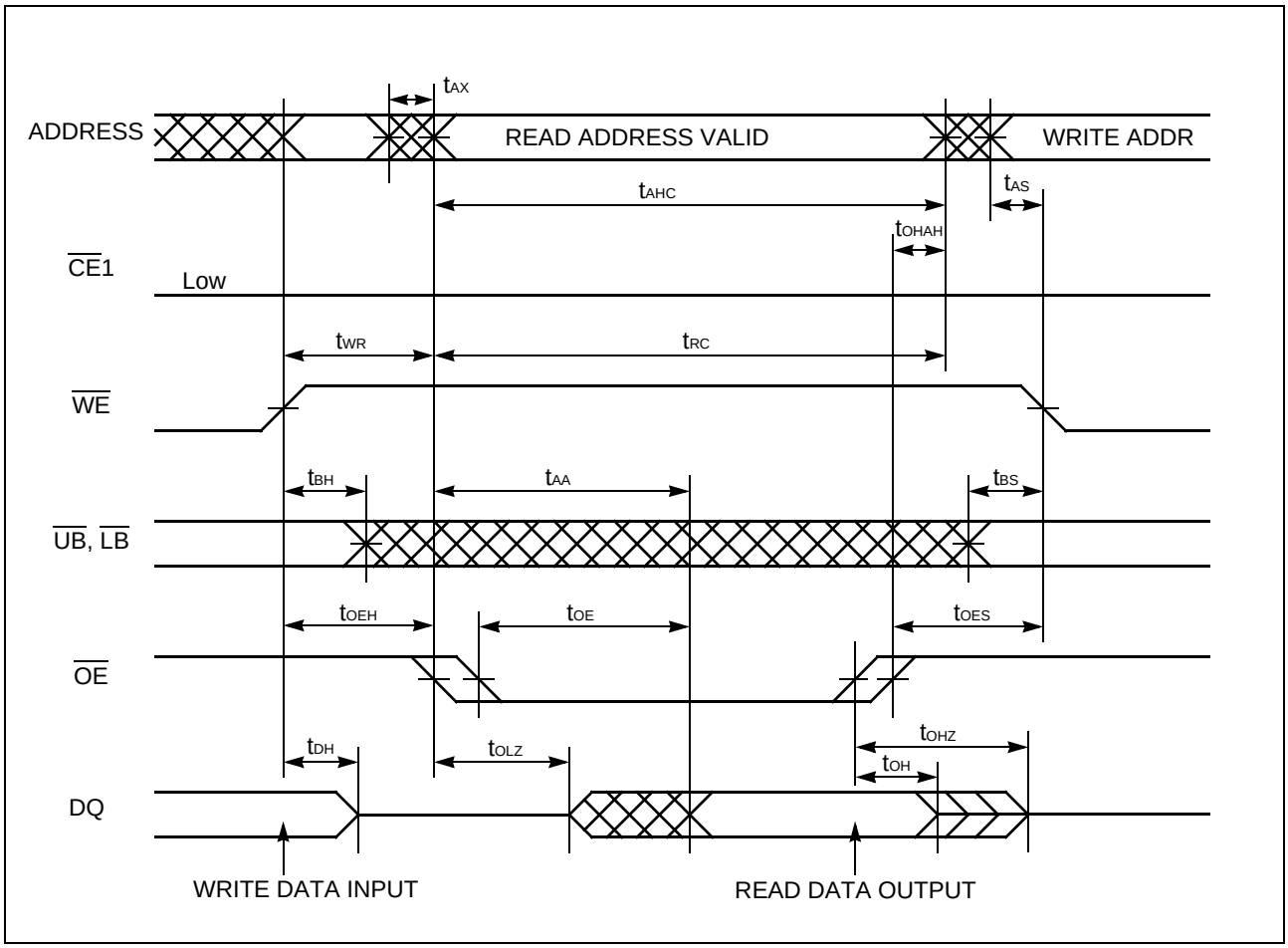


Note: $\overline{CE}1$ can be tied to LOW for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to LOW, output is exclusively controlled by $\overline{OE}$ and read address can be issued after $\overline{WE}$ is brought to High.

WARNING: The read address following write operation must be changed if $\overline{CE}1$ stays LOW.

■ TIMING DIAGRAMS (Continued)

10. READ / WRITE Timing #2-2 ($\overline{OE}$ and $\overline{WE}$ Control))

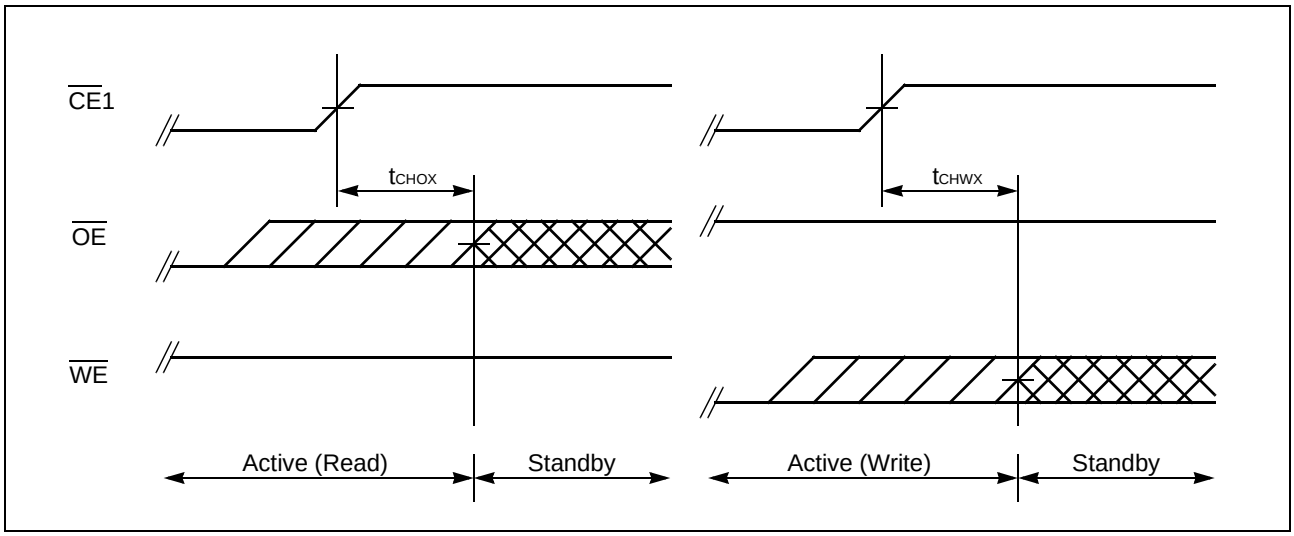


Note: $\overline{CE}1$ can be tied to LOW for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to LOW, output is exclusively controlled by $\overline{OE}$ and read address can be issued after $\overline{WE}$ is brought to High.

WARNING: The read address following write operation must be changed if $\overline{CE}1$ stays LOW.

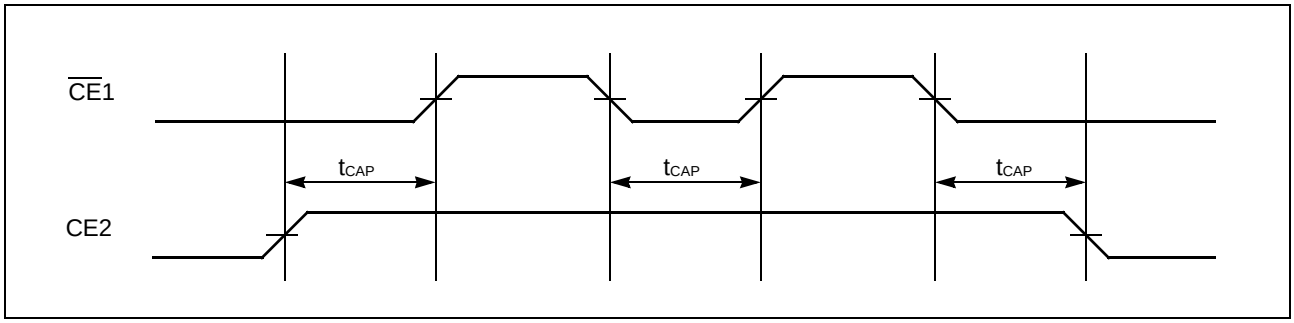
■ TIMING DIAGRAMS (Continued)

11. Standby Entry Timing after Read or Write



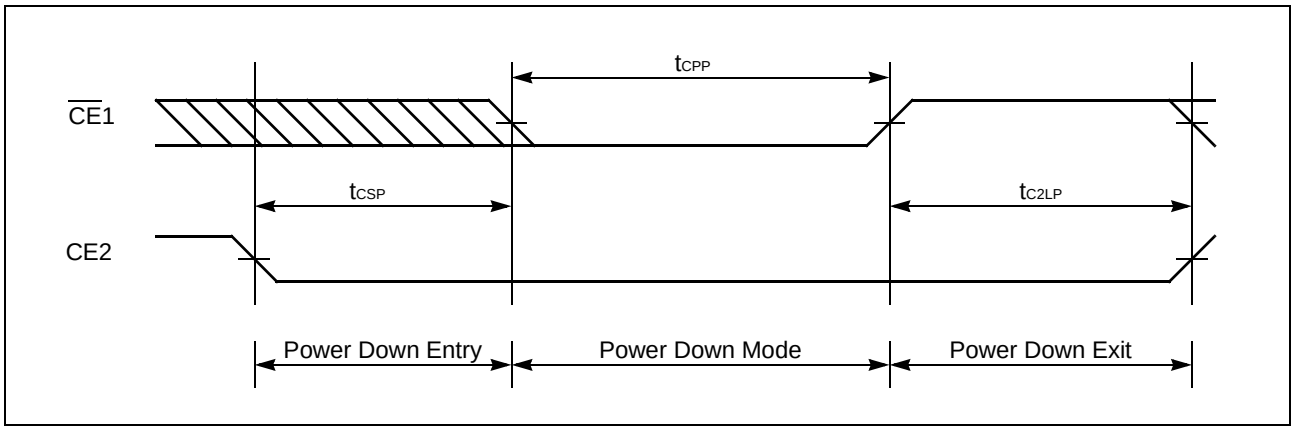
Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period from either last address transition or $\overline{CE}1$ Low to High transition.

12. Chip Enable Timing



Note: t_{CAP} is not applicable CE2 HIGH pulse width while $\overline{CE}1$ stays LOW and CE2 should not use as a read and write timing control signal in stead of $\overline{CE}1$.

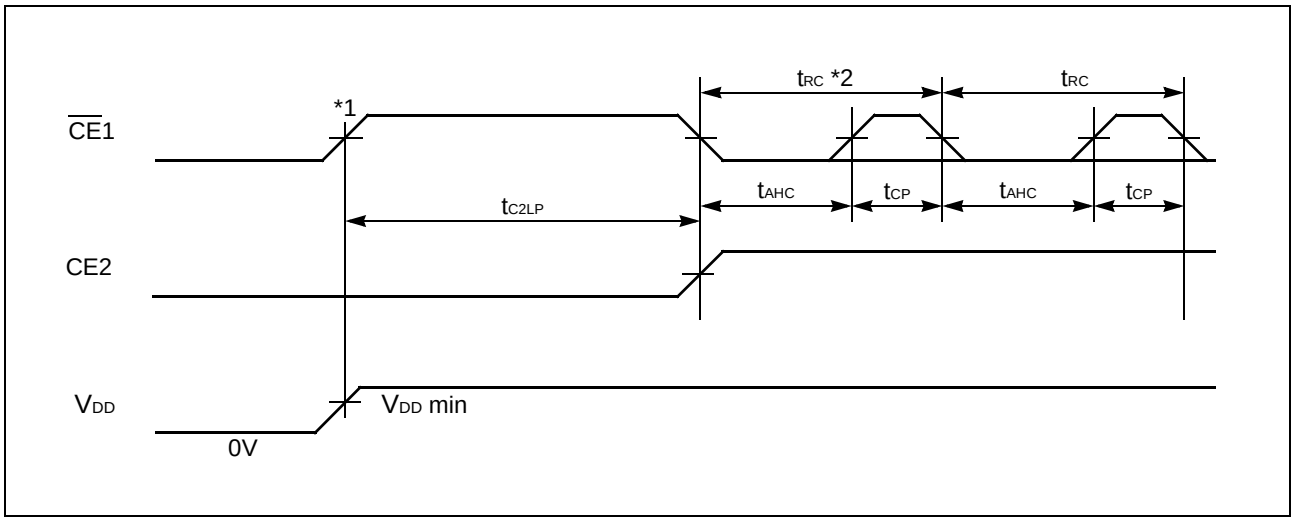
13. POWER DOWN Timing



Note: A minimum of two dummy read cycle must be performed prior to regular read and write operation after t_{C2LP}.
Otherwise $\overline{CE}1$ must kept High for t_{C1HP} period after t_{C2LP}.

■ TIMING DIAGRAMS (Continued)

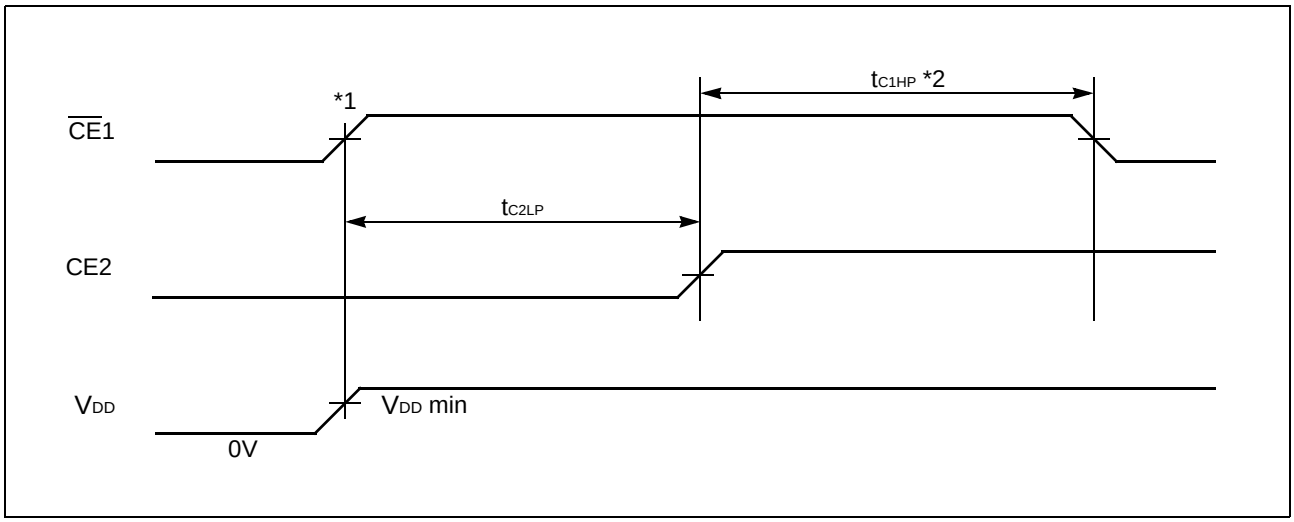
14. Power-Up Timing #1



Notes: *1. It is recommended $\overline{CE}1$ to track V_{DD}. The t_{C2LP} specifies from valid state of $\overline{CE}1$=High and CE2=Low after V_{DD} reaches specified minimum level.

*2. A minimum of two dummy read cycle must be performed prior to regular read and write operation after t_{C2LP}.

15. Power-Up Timing #2 (No dummy cycle)



Notes: *1. It is recommended $\overline{CE}1$ to track V_{DD}. The t_{C2LP} specifies from valid state of $\overline{CE}1$=High and CE2=Low after V_{DD} reaches specified minimum level.

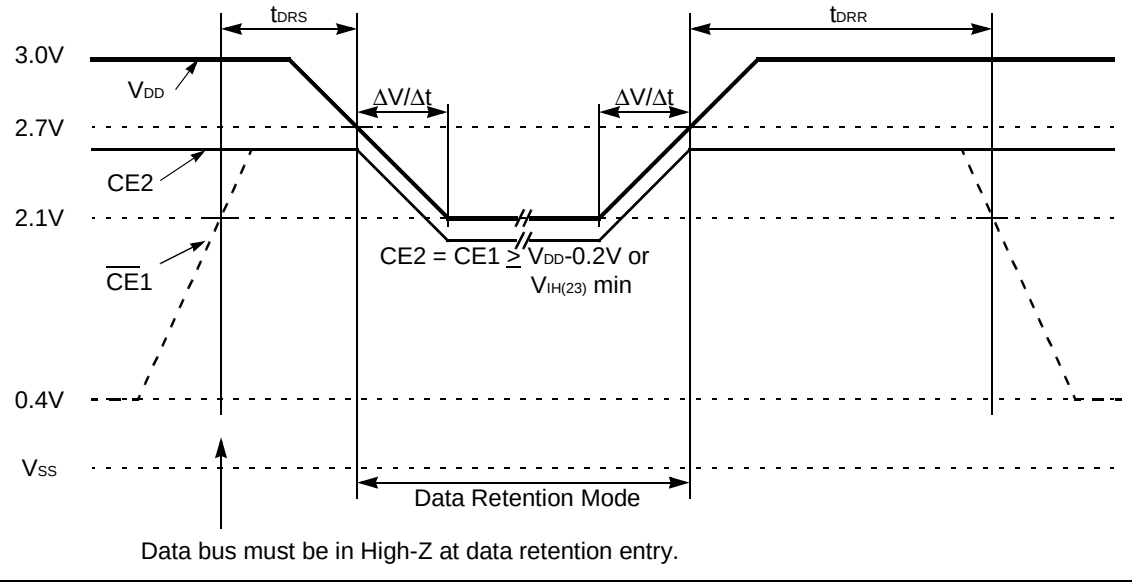
*2. No dummy read cycle is required if t_{C1HP} is satisfied.

■ DATA RETENTION

Low V_{DD} Characteristics

Parameter		Symbol	Test Conditions	Value		Unit
				Min.	Max.	
V_{DD} Data Retention Supply Voltage		V_{DR}	$\overline{CE}1 = CE2 \geq V_{DD} - 0.2V$ or, $\overline{CE}1 = CE2 = V_{IH}$,	2.1	3.5	V
V_{DD} Data Retention Supply Current	-85/-90	I_{DR}	$V_{DD} = V_{DR}$, $V_{IN} = V_{IH(23)}$ or V_{IL} $\overline{CE}1 = CE2 = V_{IH(23)}$	—	2	mA
	-85L/-90L			—	1.5	
	-85/-90	I_{DR1}	$V_{DD} = V_{DR}$ min, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{DD} - 0.2V$, $\overline{CE}1 = CE2 \geq V_{DD} - 0.2V$	—	200	µA
	-85L/-90L			—	100	
Data Retention Setup Time		t_{DRS}	$V_{DD} = V_{DD(27)}$ min at data retention entry	0	—	ns
Data Retention Recovery Time		t_{DRR}	$V_{DD} = V_{DD(27)}$ min after data retention	200	—	ns
V_{DD} Voltage Transition Time		$\Delta V/\Delta t$		0.2	—	V/µs

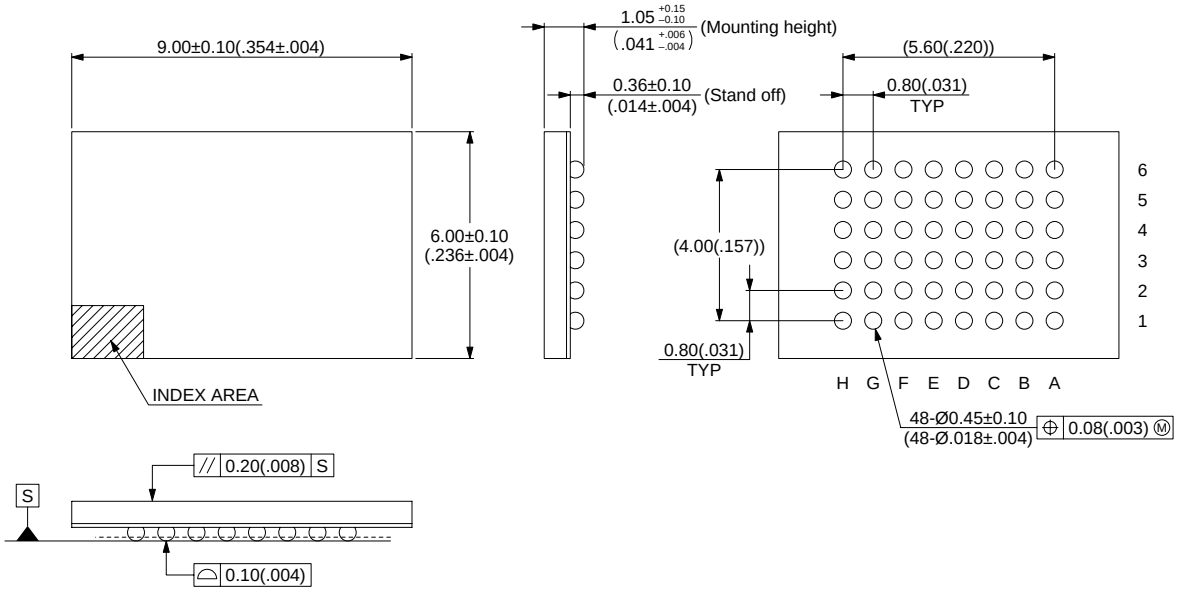
Data Retention Timing



Data bus must be in High-Z at data retention entry.

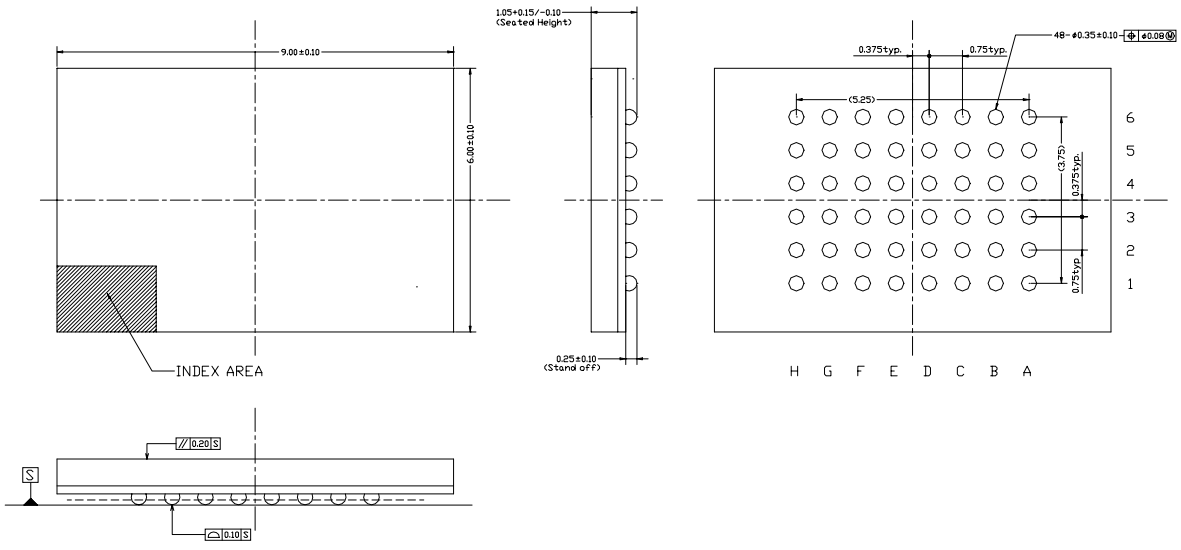
■ PACKAGE DIMENTIONS

48-pin plastic FBGA
(BGA-48P-M16)



Dimensions in mm (inches)

48-pin plastic FBGA
(BGA-48P-M18)



Dimensions in mm

■ ORDERING INFORMATION

Part Number	Package	Remarks
MB82D01161-85PBT	Plastic FBGA 48-ball 0.8mm pitch (BGA-48P-M16)	t_{CE} = 85ns max., I_{DDS1} = 200 µA max. Flash Compatibe Package
MB82D01161-85LPBT	Plastic FBGA 48-ball 0.8mm pitch (BGA-48P-M16)	t_{CE} = 85ns max., I_{DDS1} = 100 µA max. Flash Compatibe Package
MB82D01161-90PBT	Plastic FBGA 48-ball 0.8mm pitch (BGA-48P-M16)	t_{CE} = 90ns max., I_{DDS1} = 200 µA max. Flash Compatibe Package
MB82D01161-90LPBT	Plastic FBGA 48-ball 0.8mm pitch (BGA-48P-M16)	t_{CE} = 90ns max., I_{DDS1} = 100 µA max. Flash Compatibe Package
MB82D01161-85PBN	Plastic FBGA 48-ball 0.75mm pitch (BGA-48P-M18)	t_{CE} = 85ns max., I_{DDS1} = 200 µA max. SRAM Compatibe Package
MB82D01161-85LPBN	Plastic FBGA 48-ball 0.75mm pitch (BGA-48P-M18)	t_{CE} = 85ns max., I_{DDS1} = 100 µA max. SRAM Compatibe Package
MB82D01161-90PBN	Plastic FBGA 48-ball 0.75mm pitch (BGA-48P-M18)	t_{CE} = 90ns max., I_{DDS1} = 200 µA max. SRAM Compatibe Package
MB82D01161-90LPBN	Plastic FBGA 48-ball 0.75mm pitch (BGA-48P-M18)	t_{CE} = 90ns max., I_{DDS1} = 100 µA max. SRAM Compatibe Package

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