FUJITSU SEMICONDUCTOR
DATA SHEET

DS04-21330-1E

ASSP

Single Serial Input PLL Frequency Synthesizer

On-Chip 2.0GHz Prescaler

MB15E05

■ DESCRIPTION

The Fujitsu MB15E05 is serial input Phase Locked Loop (PLL) frequency synthesizers with a 2.0 GHz prescaler. A 64/65 or a 128/129 can be selected for the prescaler that enables pulse swallow operation.

The latest BiCMOS process technology is used, resultantly a supply current is limited as low as 6mA typ. This operates with a supply voltage of 3.0V (typ.).

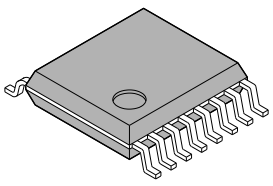
Furthermore, a super charger circuit is included to get a fast tuning as well as low noise performance. As a result of this, MB15E05 is ideally suitable for digital mobile communications, such as PCN (Personal Communication Network), PCS (Personal Communication Service), etc.

■ FEATURES

- High frequency operation: 2.0 GHz max
- Low power supply voltage: V_{CC} = 2.7 to 3.6V
- Very Low power supply current : I_{CC} = 6.0 mA typ. (Vcc = 3V)
- Power saving function : I_{PS} = 10 µA max.
- Pulse swallow function: 64/65 or 128/129
- Serial input 14-bit programmable reference divider: R = 5 to 16,383
- Serial input 18-bit programmable divider consisting of:
  - Binary 7-bit swallow counter: 0 to 127
  - Binary 11-bit programmable counter: 5 to 2,047
- Wide operating temperature: Ta = –40 to 85°C
- Plastic 16-pin SSOP package (FPT-16P-M05)

■ PACKAGE

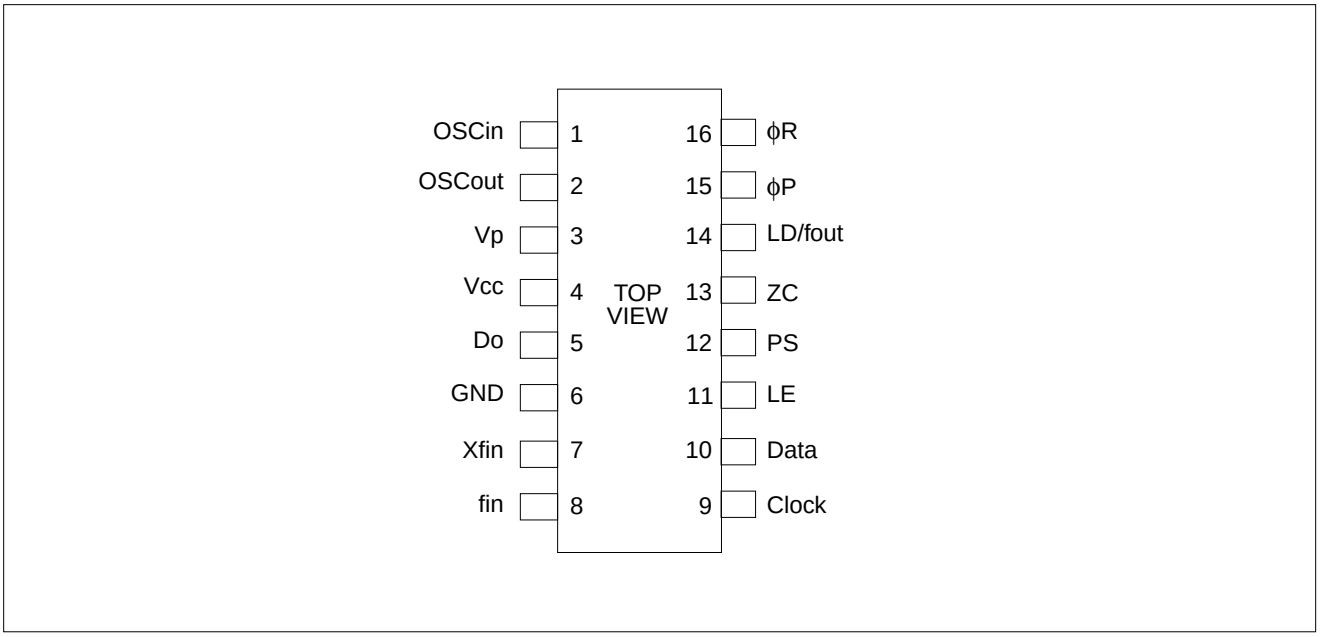
16-pin, Plastic SSOP



(FPT-16P-M05)

This device contains circuitry to protect the inputs against damage due to high static voltages or electroc fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

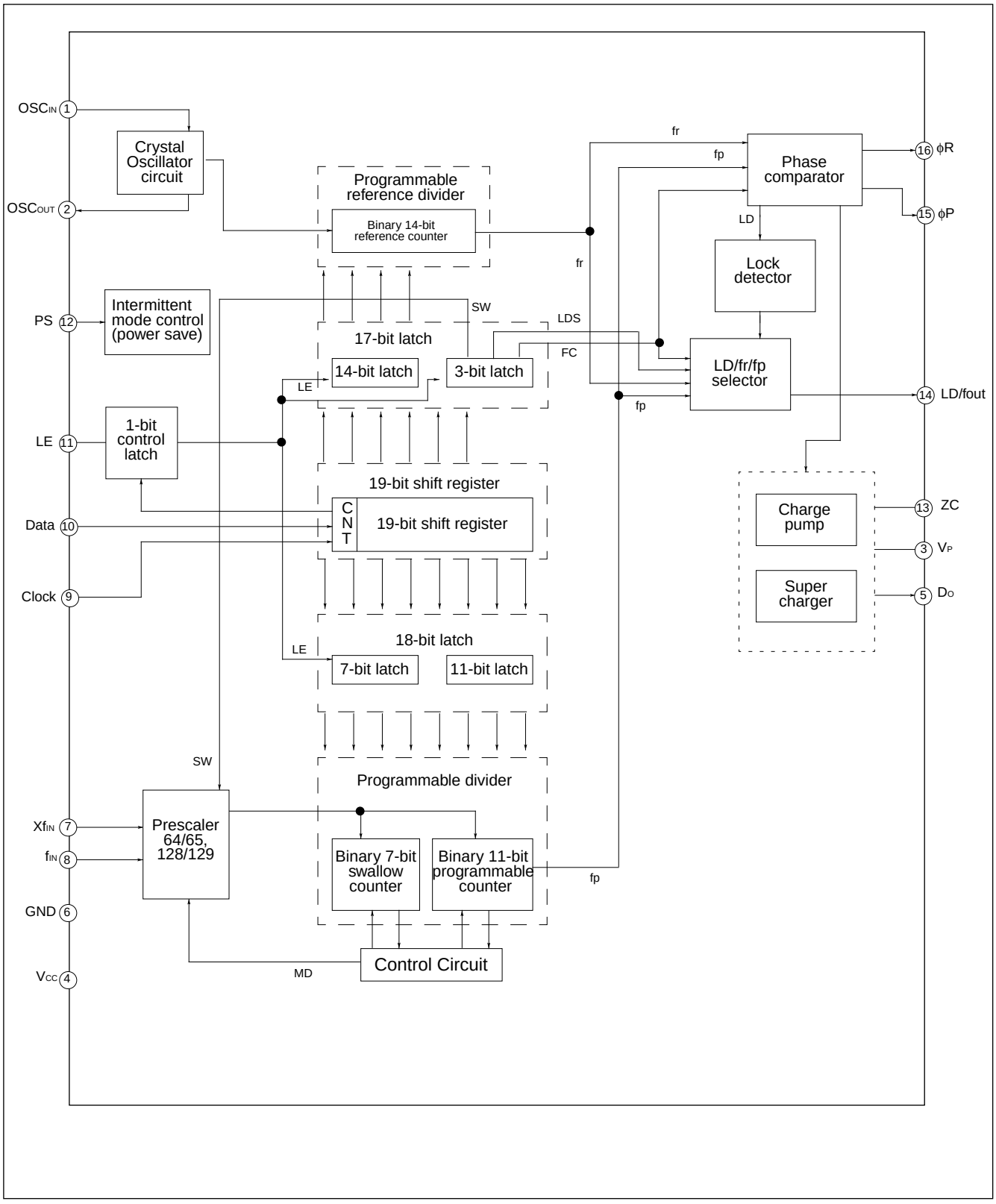
■ PIN ASSIGNMENT



■ PIN DESCRIPTIONS

Pin No.	Pin Name	I/O	Descriptions
1	OSC_{IN}	I	Programmable reference divider input. Oscillator input. Connection for an crystal or a TCXO. TCXO should be connected with a coupling capacitor.
2	OSC_{OUT}	O	Oscillator output. Connection for an external crystal.
3	V_P	–	Power supply voltage input for the charge pump.
4	V_{CC}	–	Power supply voltage input.
5	D_O	O	Charge pump output. Phase of the charge pump can be reversed by FC input.
6	GND	–	Ground.
7	Xfin	I	Prescaler complementary input, and should be grounded via a capacitor.
8	fin	I	Prescaler input. Connection with an external VCO should be done with AC coupling.
9	Clock	I	Clock input for the 19-bit shift register. Data is shifted into the shift register on the rising edge of the clock. *(Open is prohibited.)*
10	Data	I	Serial data input using binary code. The last bit of the data is a control bit. *(Open is prohibited.)* Control bit = ”H” ; Data is transmitted to the programmable reference counter. Control bit = ”L” ; Data is transmitted to the programmable counter.
11	LE	I	Load enable signal input *(Open is prohibited.)* When LE is high, the data in the shift register is transferred to a latch, according to the control bit in the serial data.
12	PS	I	Power saving control input. This pin should be set at ”L” at Power-ON. *(Open is prohibited.)* PS = ”H” ; Normal mode PS = ”L” ; Power saving mode
13	ZC	I	Forced high-impedance control for the charge pump (with internal pull up resistor.) ZC = ”H” ; Normal Do output. ZC = ”L” ; Do becomes high impedance.
14	LD/fout	O	Lock detect signal output(LD)/ phase comparator monitoring output (fout). The output signal is selected by LDS bit in the serial data. LDS = ”H” ; outputs fout (fr/fp monitoring output) LDS = ”L” ; outputs LD (”H” at locking, ”L” at unlocking.)
15	ϕP	O	Phase comparator output for an external charge pump.
16	ϕR	O	Phase comparator output for an external charge pump.

■ BLOCK DIAGRAM 1



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Remark
Power supply voltage	V_{CC}	–0.5 to +4.0	V	
	V_P	V_{CC} to +6.0	V	
Input voltage	V_I	–0.5 to V_{CC} +0.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Storage temperature	T_{stg}	–55 to +125	°C	

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Power supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_P	V_{CC}	–	6.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:
-Store and transport devices in conductive containers.
-Use properly grounded workstations, tools, and equipment.
-Turn off power before inserting or removing this device into or from a socket.
-Protect leads with conductive sheet, when transporting a board mounted device.

■ ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Unit
				Min	Typ	Max	
Power supply current*1		I_{CC}	fin_{IF} = 2000MHz, fosc = 12MHz	–	6.0	–	mA
Power saving current*2		Ips	Vcc current at PS ="L" and ZC = "H"	–	–	10	µA
Operating frequency		fin		100	–	2000	MHz
Crystal oscillator operating frequency		f_{OSC}	min. 500mVp-p	3	–	40	MHz
Input sensitivity	fin	$Vfin_{IF}$	50Ω termination (Refer to the test circuit.)	–10	–	+2	dBm
	OSCin	V_{OSC}		500	–	V_{CC}	mVp–p
Input voltage	Data, Clock, LE, PS, ZC	V_{IH}		Vccx0.7	–	–	V
		V_{IL}		–	–	Vccx0.3	
Input current	Data, Clock, LE, PS	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}		–1.0	–	+1.0	
	ZC	I_{IH}		–1.0	–	+1.0	µA
		I_{IL}	Pull up input	–100	–	0	
	OSCin	I_{IH}		0	–	+100	µA
		I_{IL}		–100	–	0	
Output voltage	ϕP	V_{OL}	Open drain output	–	–	0.4	V
	ϕR, LD/fout	V_{OH}		Vcc-0.4	–	–	V
		V_{OL}		–	–	0.4	
	Do	V_{DOH}		Vcc-0.4	–	–	V
		V_{DOL}		–	–	0.4	
High impedance cutoff current	Do	I_{OFF}		–	–	1.1	µA
Output current	ϕP	I_{OL}	Open drain output	1.0	–	–	mA
	ϕR, LD/fou	I_{OH}		–	–	–1.0	mA
		I_{OL}		1.0	–	–	
	Do	I_{DOH}	Vcc = 3.0V, Vp = 5V, V_{DOH} = 4.0V	–	–10.0*2	–	mA
		I_{DOL}	Vcc = 3.0V, Vp = 5V, V_{DOL} = 1.0V	–	10.0*2	–	

*1: Conditions ; Vcc = 3.0V, Ta = 25°C, in locking state.

*2: Conditions ; Ta = 25°C

■ FUNCTION DESCRIPTIONS

Pulse Swallow Function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \leq A \leq 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (5 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial Data Input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the programmable reference divider and the programmable divider separately.
Binary serial data is entered through the Data pin.
One bit of data is shifted into the shift register on the rising edge of the clock. When the load enable pin is high, stored data is latched according to the control bit data as follows:

Table.1 Control Bit

Control bit (CNT)	Destination of serial data
H	17 bit latch (for the programmable reference divider)
L	18 bit latch (for the programmable divider)

Shift Register Configuration

Programmable Reference Counter

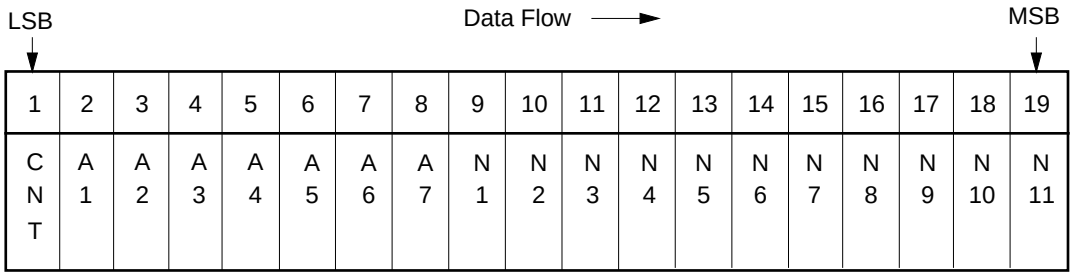
LSB ↓ Data Flow → MSB ↓

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
CNT	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	FC	LDS

CNT : Control bit [Table. 1]
R1 to R14 : Divide ratio setting bit for the programmable reference counter (5 to 16,383) [Table. 2]
SW : Divide ratio setting bit for the prescaler (64/65 or 128/129) [Table. 5]
FC : Phase control bit for the phase comparator [Table. 7]
LDS : LD/fout signal select bit [Table. 6]

Note: Start data input with MSB first

Programmable Reference Counter



CNT : Control bit [Table. 1]
N1 to N11 : Divide ratio setting bits for the programmable counter (5 to 2,047) [Table. 3]
A1 to A7 : Divide ratio setting bits for the swallow counter (0 to 127) [Table. 4]

Note: Start data input with MSB first

Table2. Binary 14-bit Programmable Reference Counter Data Setting

Divide ratio (R)	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
5	0	0	0	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.	.	.	.
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.

Table.3 Binary 11-bit Programmable Counter Data Setting

Divide ratio (N)	N 11	N 10	N 9	N 8	N 7	N 6	N 5	N 4	N 3	N 2	N 1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
.	.	.	.	.	.	.	.	.	.	.	.
2047	1	1	1	1	1	1	1	1	1	1	1

Note: • Divide ratio less than 5 is prohibited.
• Divide ratio (N) range = 5 to 2,047

Table.4 Binary 7-bit Swallow Counter Data Setting

Divide ratio (A)	A 7	A 6	A 5	A 4	A 3	A 2	A 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
.	.	.	.	.	.	.	.
127	1	1	1	1	1	1	1

Note: • Divide ratio (A) range = 0 to 127

Table. 5 Prescaler Data Setting

SW	Prescaler Divide ratio
H	64/65
L	128/129

Table. 6 LD/fout Output Select Data Setting

LDS	LD/fout output signal
H	fout signal
L	LD signal

Relation between the FC input and phase characteristics

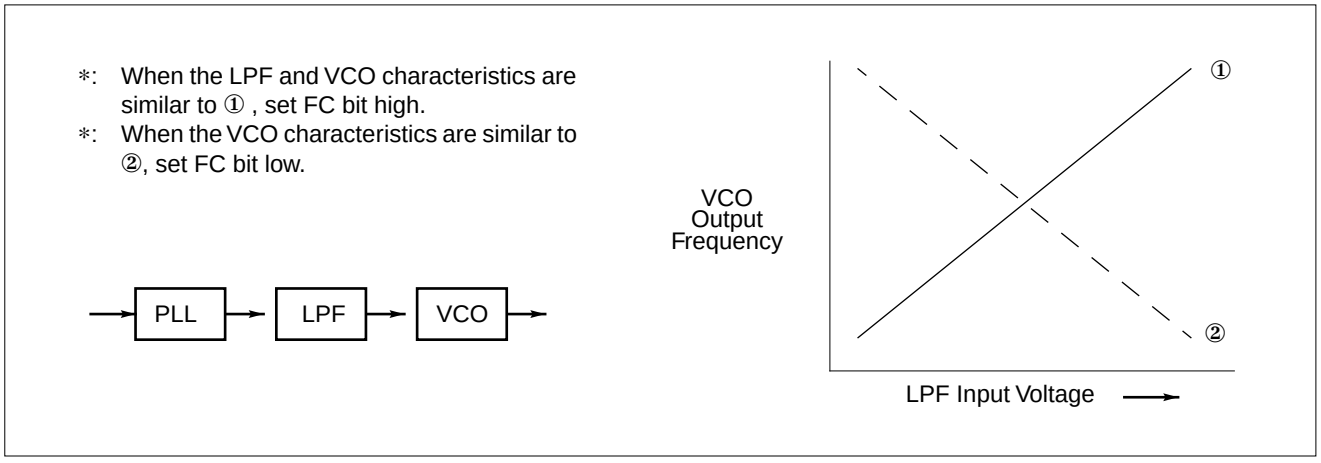
The FC bit changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ϕR, ϕP) are reversed according to the FC bit. Also, the monitor pin (f_{OUT}) output is controlled by the FC bit. The relationship between the FC bit and each of D_O, ϕR, and ϕP is shown below.

Table. 7 FC Bit Data Setting (LDS = "H")

	FC = High				FC = Low			
	Do	ϕR	ϕP	LD/fout	Do	ϕR	ϕP	LD/fout
$f_r > f_p$	H	L	L	(fr)	L	H	Z*	(fp)
$f_r < f_p$	L	H	Z*	(fr)	H	L	L	(fp)
$f_r = f_p$	Z*	L	Z*	(fr)	Z*	L	Z*	(fp)

* : High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.



Power Saving Mode (Intermittent Mode Control Circuit)

Setting a PS pin to Low, the IC enters into power saving mode resultatly current sonsumption can be limited to 10μA (max.). Setting PS pin to High, power saving mode is released so that the IC works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from the power saving mode. In general, the power consumption can be saved by the intermittent operation that powering down or waking up the synthesizer. Such case, if the PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_r) and comparison frequency (f_p) and may in the worst case take longer time for lock up of the loop.
To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.
During the power saving mode, the corresponding section except for indispensable circuit for the power saving function stops working, then current consumption is reduced to 10μA per one PLL section.
At that time, the Do and LD become the same state as when a loop is locking. That is, the Do becomes high impedance.
A VCO control voltage is naturally kept at the locking voltage which defined by a LPF"s time constant. As a result of this, VCO's frequency is kept at the locking frequency.

Note:
- *While the power saving mode is executed, ZC pin should be set at "H" or open. If ZC is set at "L" during power saving mode, approximately 10 μA current flows.*
- *PS pin must be set "L" at Power-ON.*
- *The power saving mode can be released (PS : L → H) 1μs later after power supply remains stable.*
- *During the power saving mode, it is possible to input the serial data.*

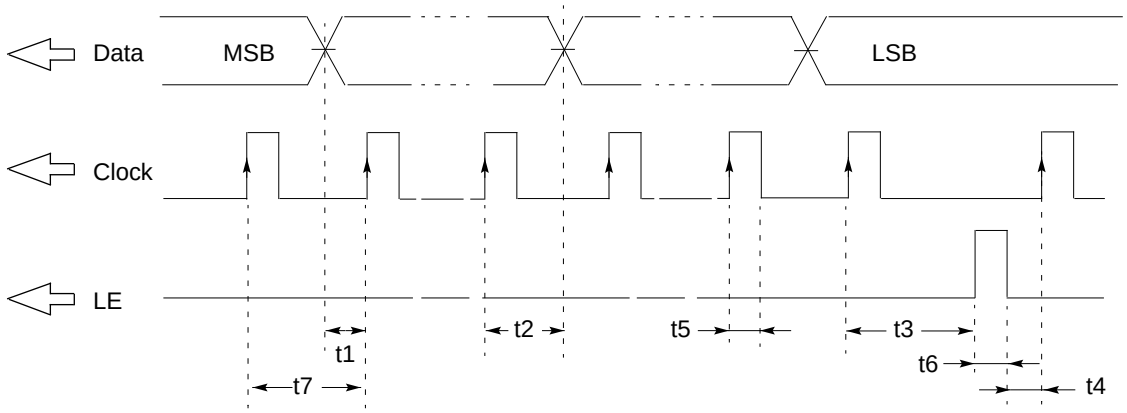
Table.8 PS Pin Setting

PS pin	Status
H	Normal mode
L	Power saving mode

Table.9 ZC Pin Setting

ZC pin	Do output
H	Normal output
L	High impedance

■ SERIAL DATA INPUT TIMING

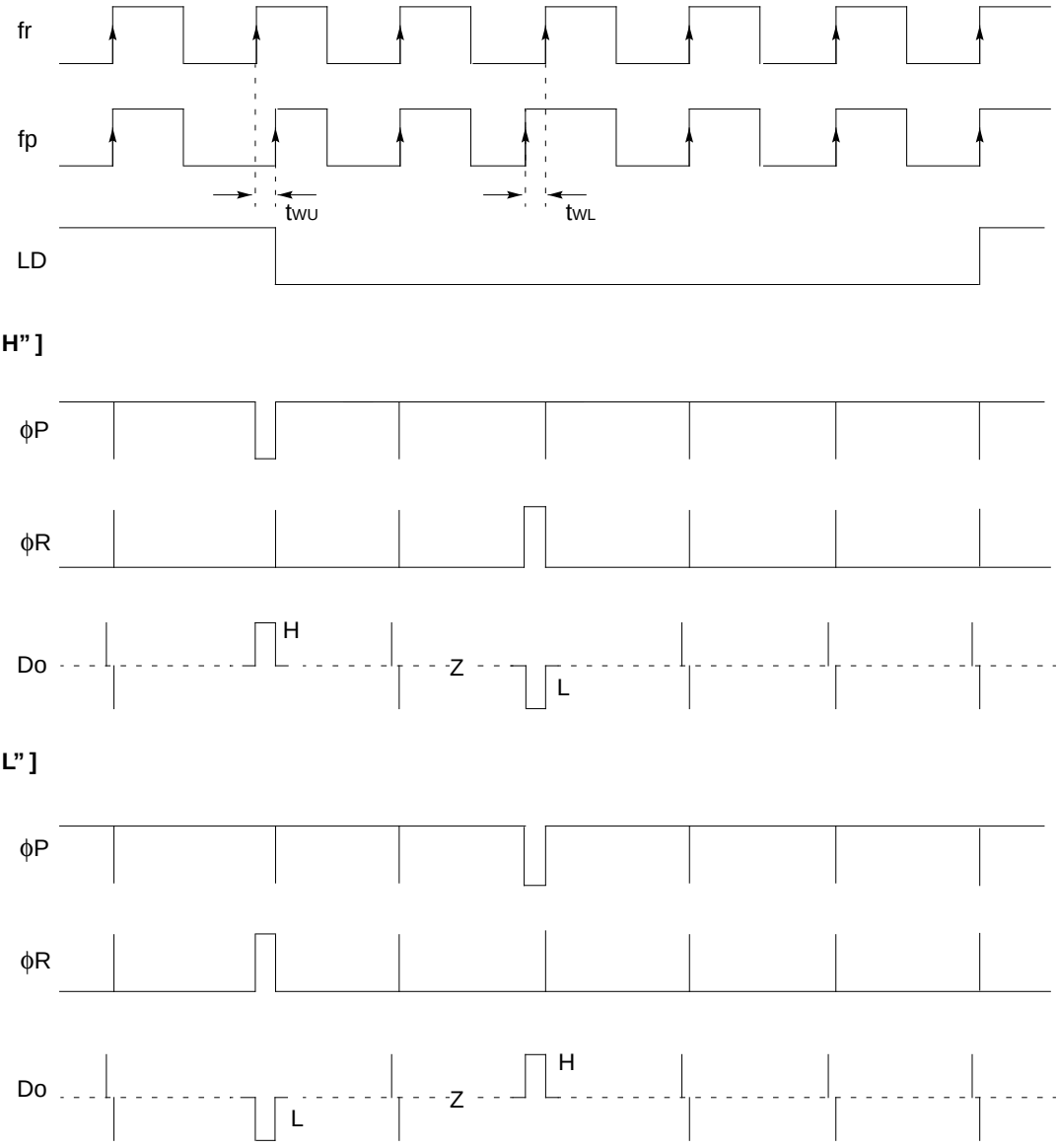


On rising edge of the clock, one bit of the data is transferred into the shift register.

Parameter	Min.	Typ.	Max.	Unit
t1	20	–	–	ns
t2	20	–	–	ns
t3	30	–	–	ns
t4	20	–	–	ns

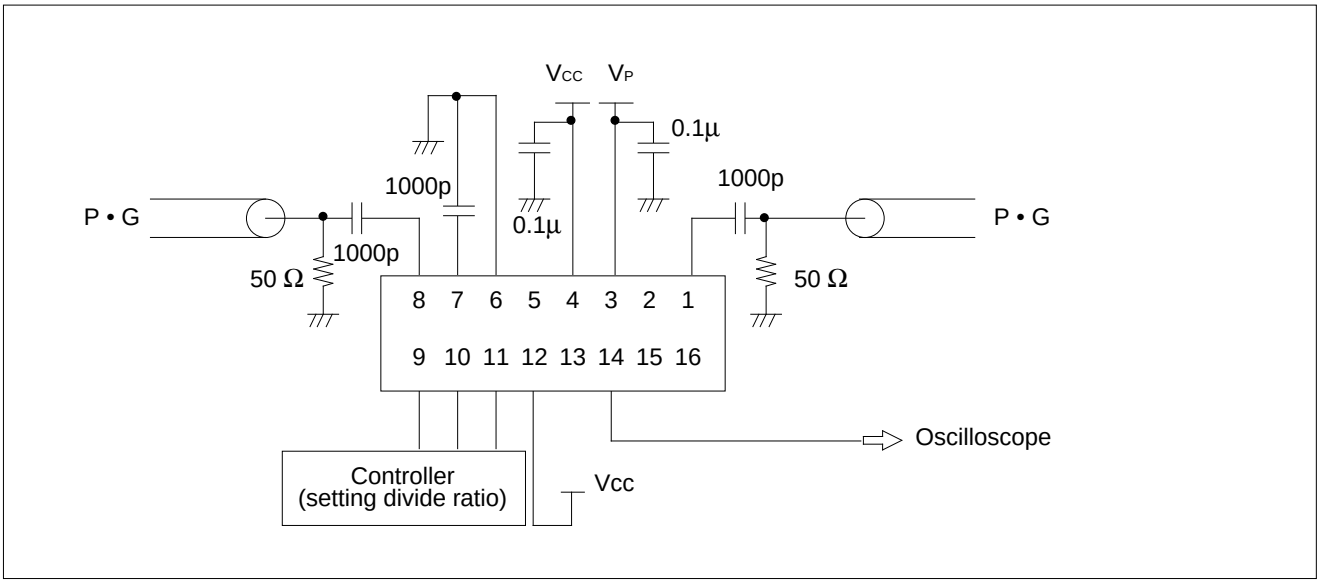
Parameter	Min.	Typ.	Max.	Unit
t5	30	–	–	ns
t6	100	–	–	ns
t7	100	–	–	ns

■ PHASE COMPARATOR OUTPUT WAVEFORM

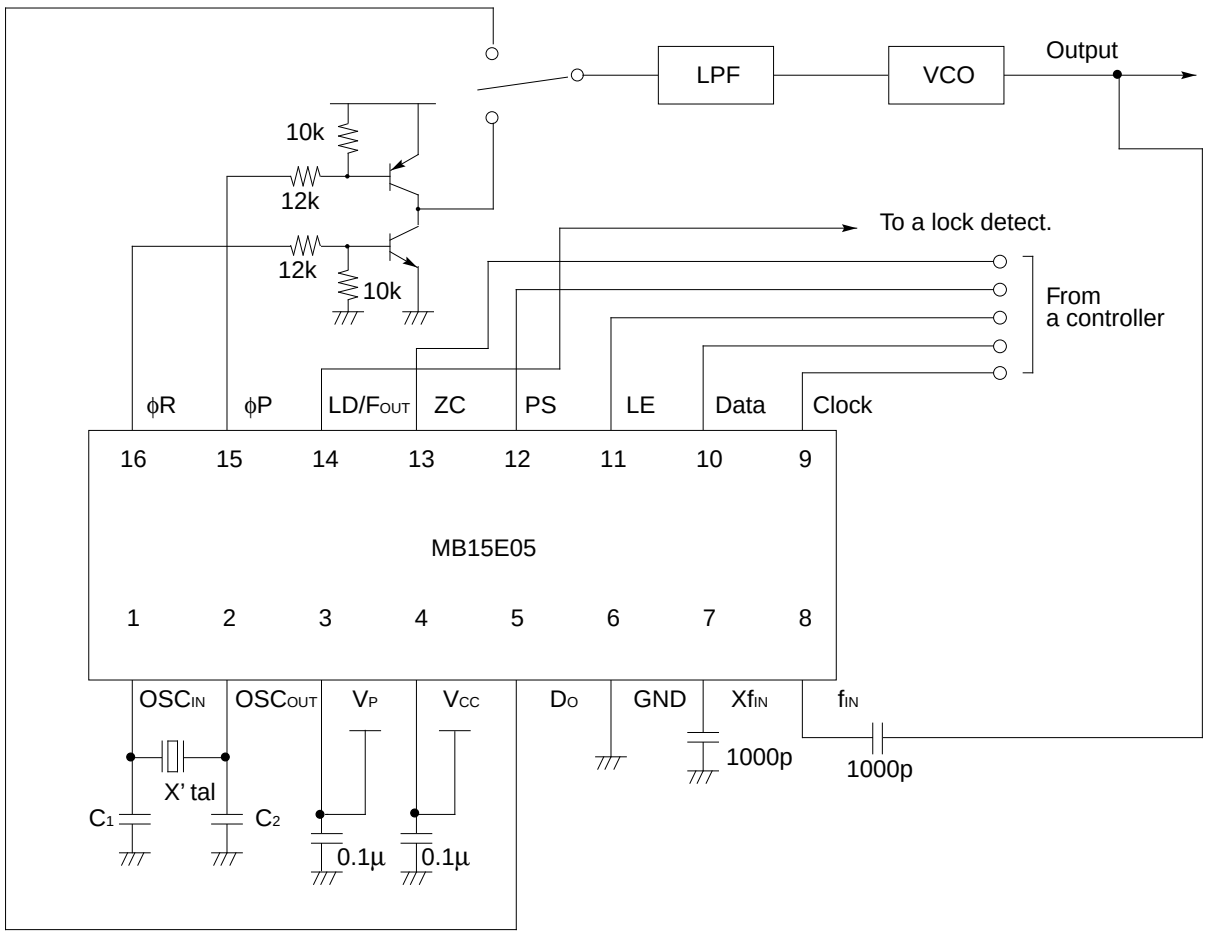


Notes:
1. Phase error detection range: -2π to $+2\pi$
2. Pulses on Do output signal during locked state are output to prevent dead zone.
3. LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cysles or more.
4. t_{WU} and t_{WL} depend on OSCin input frequency.
   $t_{WU} \geq 8/fosc$ (e. g. $t_{WU} \geq 625ns$, foscin = 12.8 MHz)
   $t_{WL} \leq 16/fosc$ (e. g. $t_{WL} \leq 1250ns$, foscin = 12.8 MHz)
5. LD becomes high during the power saving mode (PS = "L".)

■ TEST CIRCUIT (for Measuring Input Sensitivity fin/OSCin)



■ APPLICATION EXAMPLE

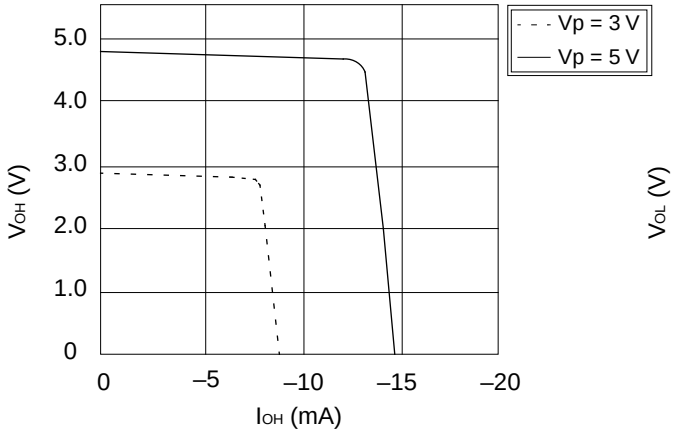


C_1, C_2 : Depend on the crystal parameters

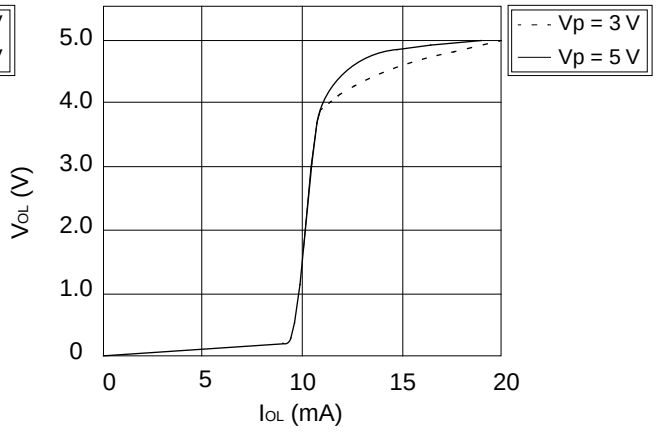
■ TYPICAL CHARACTERISTICS

Do Output Current

[Ta = +25°C]
[V_{CC} = 3 V, Vp =3 V, 5 V]

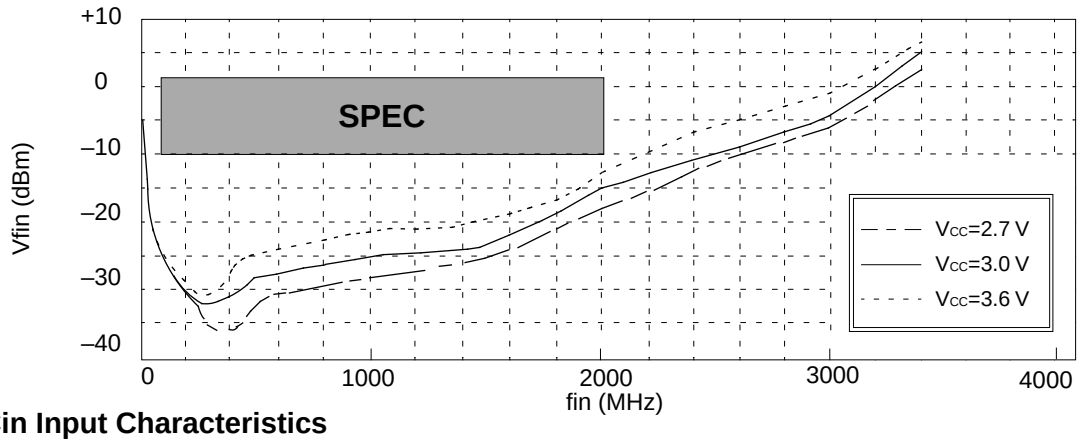


[Ta = +25°C]
[V_{CC} = 3 V, Vp =3 V, 5 V]



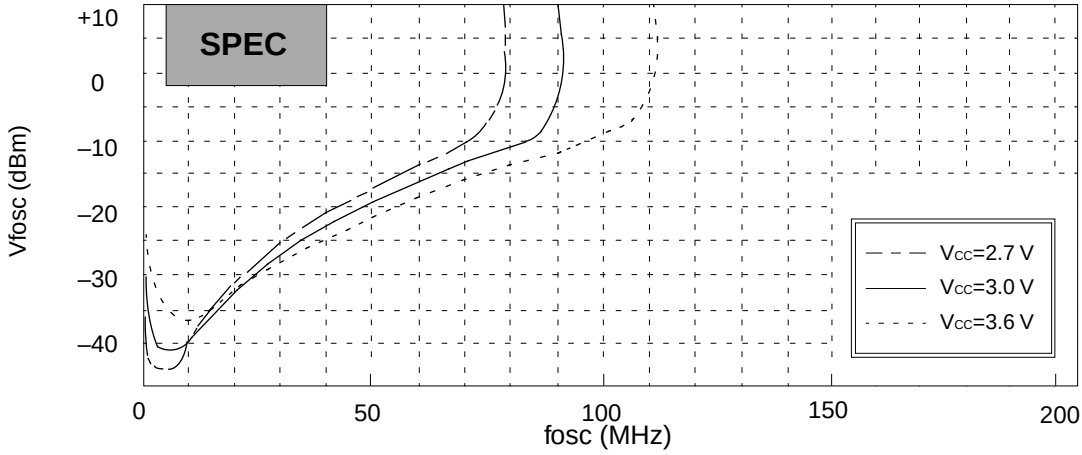
fin Input Sensitivity

Vfin vs. fin
[Ta = +25°C]
Main. counter div. ratio = 4104
Swallow="ON"
V_{CC} = Vp



OSCin Input Characteristics

Vfiosc vs. fosc
[Ta = +25°C]
Ref. counter div. ratio = 767
fin, Xfin : OPEN



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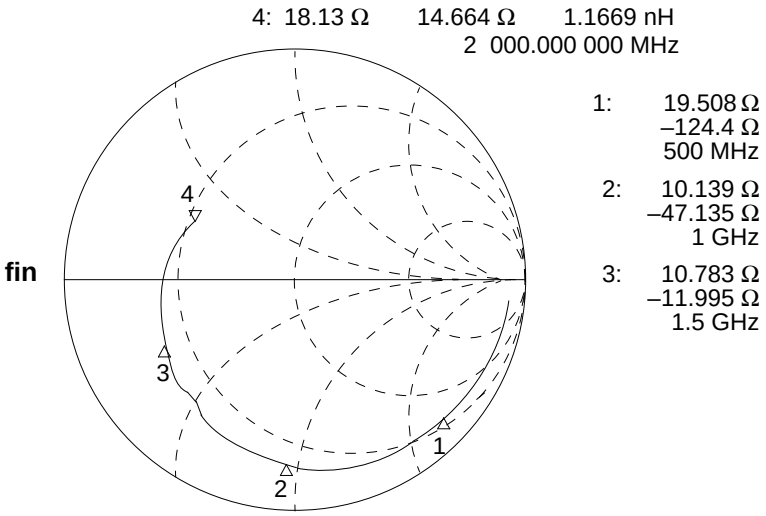
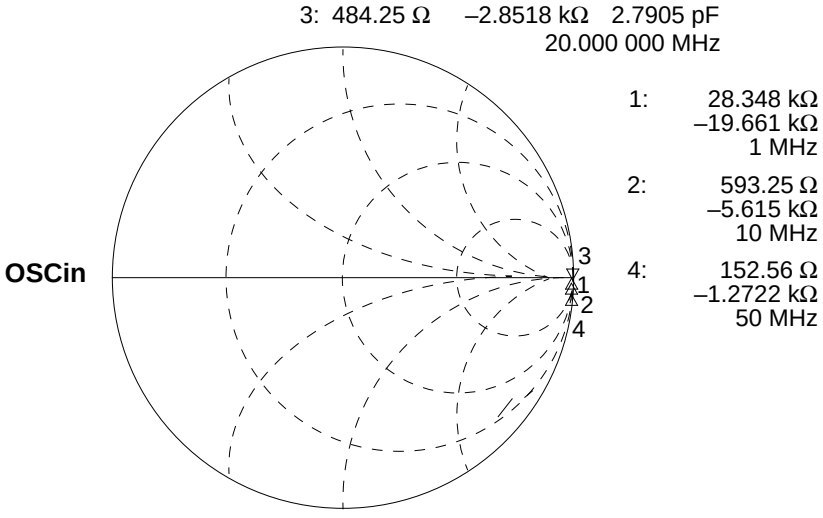
fin Input Impedance



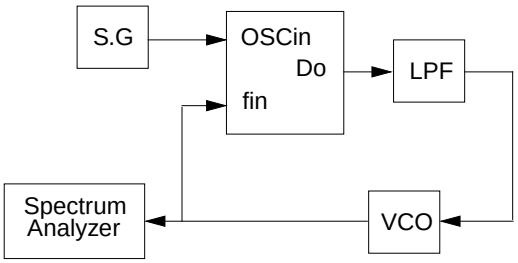
OSCin Input Impedance



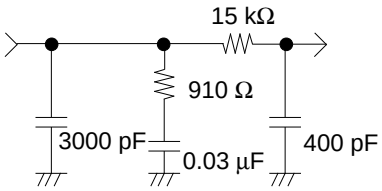
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise and reference leakage.

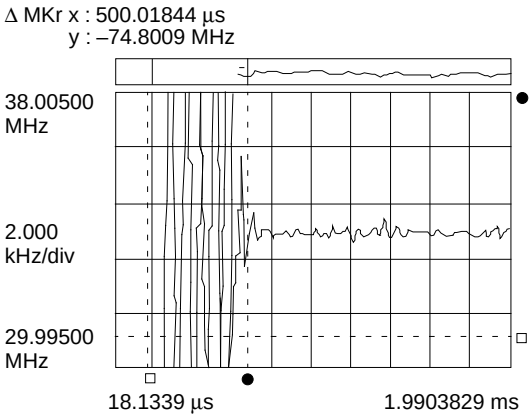
Test Circuit



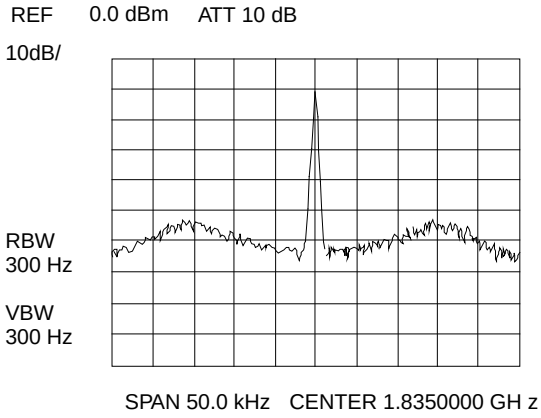
- fvco = 1835 MHz
- Kv = 87 MHz/v
- fr = 200 kHz
- fosc = 13 MHz
- LPF:

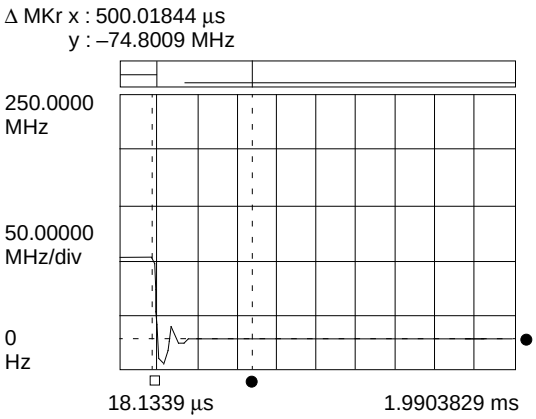


PLL Lock Up Time = 500 µs
(1797.6 MHz → 1872.4 MHz, within ± 1kHz)

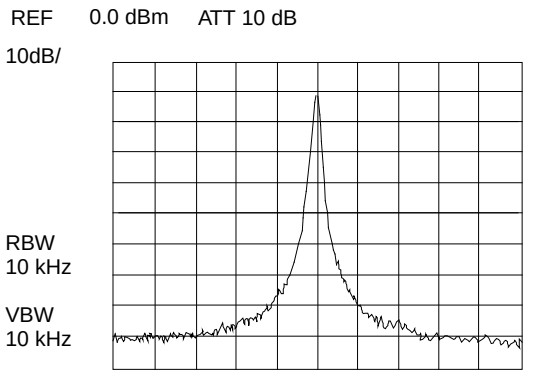


PLL Phase Noise
@ within loop band = 69.4 dBc/Hz





PLL Reference Leakage
@ 200 kHz offset = 74.6 dBc



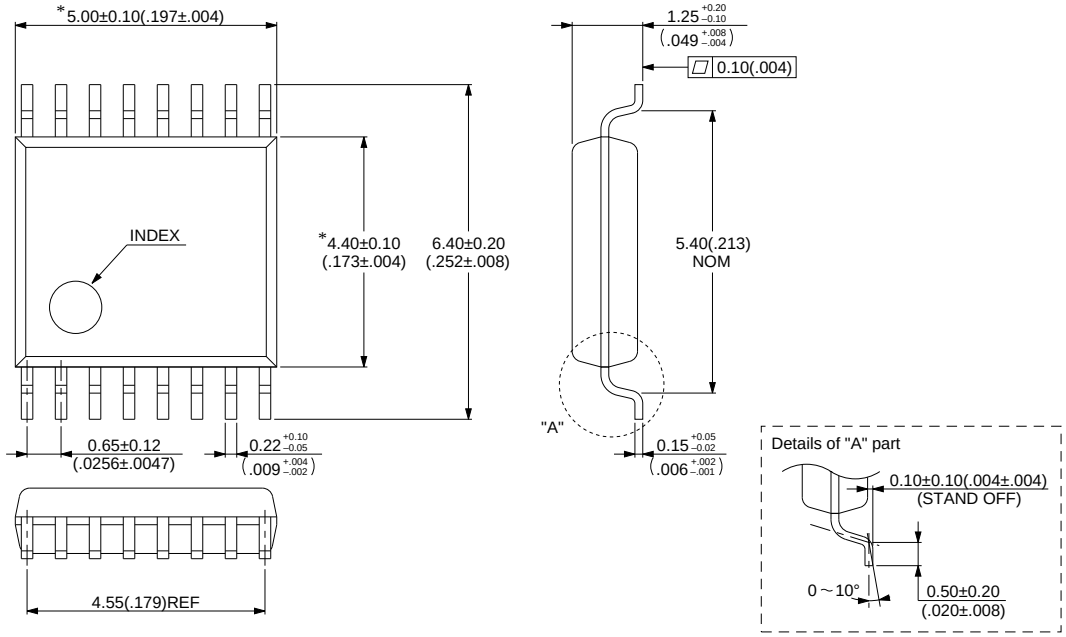
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15E05PFV1	16-pin Plastic SSOP (FPT-16P-M05)	

■ PACKAGE DIMENSION

16 pins, Plastic SSOP
(FPT-16P-M05)

* : These dimensions do not include resin protrusion.



Dimensions in mm (inches)

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