DS04-21329-2E

FUJITSU

DATA SHEET

ASSP for DTS
BiCMOS 1.1 GHz PLL Frequency Synthesizer
MB15A03

■ DESCRIPTION

The MB15A03 is a Phase Locked Loop (PLL) frequency synthesizer LSI operating at up to 1.1 GHz. It incorporates a dual-modulus prescaler allowing either a 64/65 or a 128/129 frequency division to be selected.

The MB15A03 has a built-in power save function, achieving low power consumption.

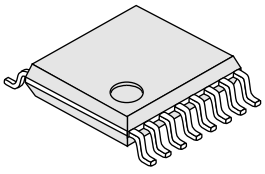
The MB15A03 design is ideal for analog mobile telecommunications equipment.

■ FEATURES

- Operation at high speed: Up to 1.1 GHz
- Operation at low voltage: 2.7 to 3.6 V
- Low current consumption: Typical 6.5 mA (V_{CC} = 3 V)
- Built-in power saving function: Typical 100 μA (V_{CC} = 3V)
- Dual-modulus prescaler divide ratio: 64/65 or 128/129
- Reference divider
  Binary 14-bit reference counter (divide ratio of 6 to 16,383)
- Comparative dividers
  Binary 7-bit swallow counter (divide ratio of 0 to 127)
  Binary 11-bit programmable counter (divide ratio of 5 to 2,047)
- Internal phase comparator with phase conversion features
- Internal digital lock detection circuit for PLL lock/unlock detection
- Operating temperature range: –40 to +85°C

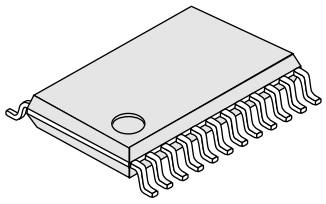
■ PACKAGES

16-pin, plastic SSOP



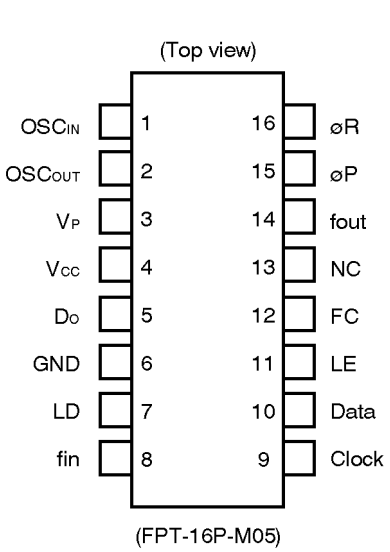
(FPT-16P-M05)

20-pin, plastic SSOP

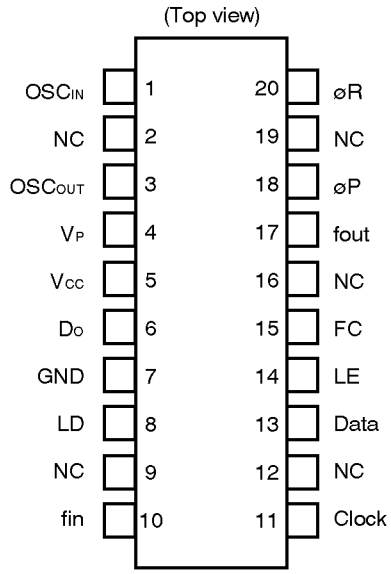


(FPT-20P-M03)

■ PIN ASSIGNMENTS



(FPT-16P-M05)

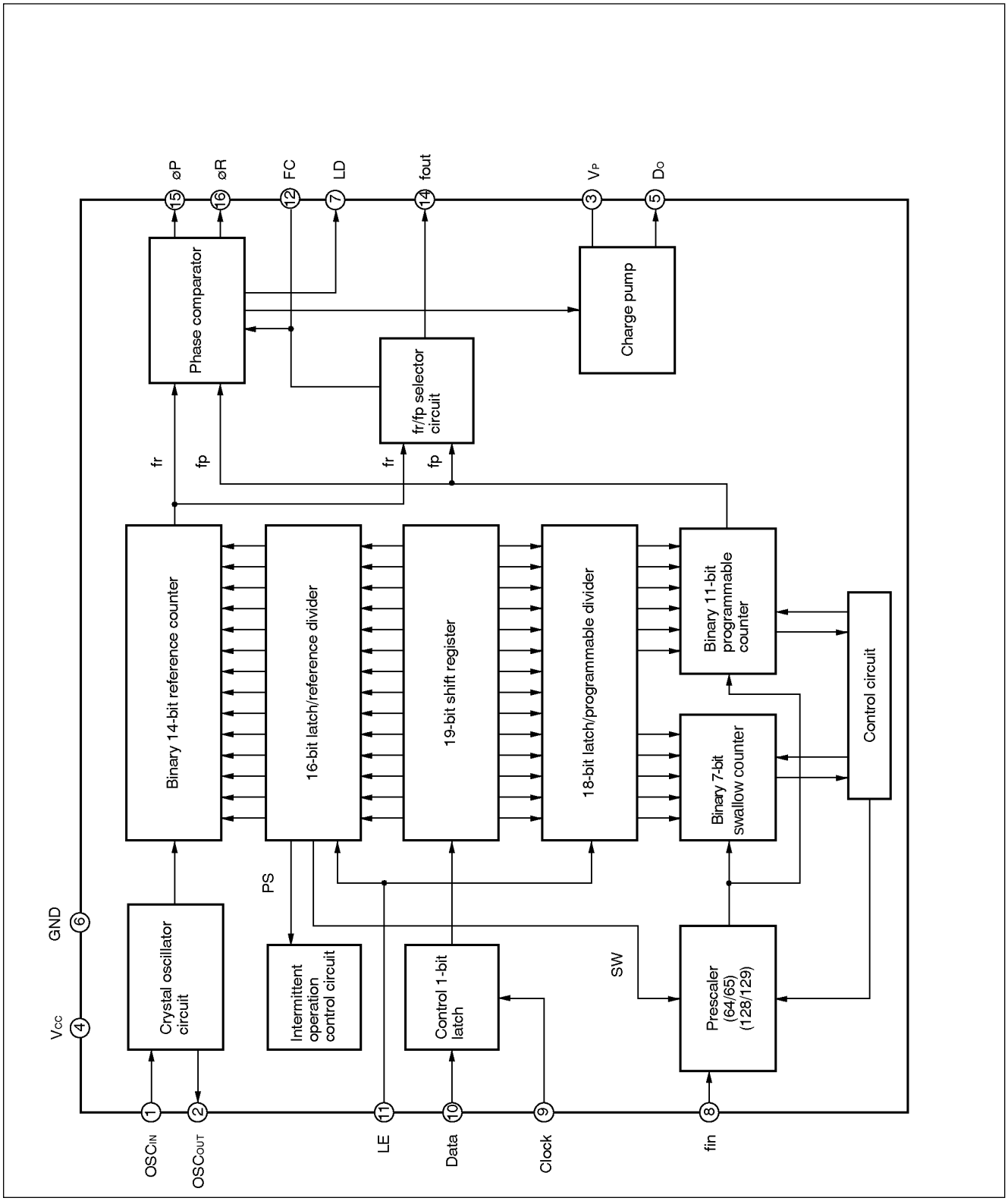


(FPT-20P-M03)

■ PIN DESCRIPTIONS

Pin No.		Symbol	I/O	Function
SSOP-16	SSOP-20			
1	1	OSC_{IN}	I	Crystal oscillator connection pin serving as a reference divider input pin (oscillator circuit input pin).
2	3	OSC_{OUT}	O	Crystal oscillator connection pin (oscillator circuit output pin).
3	4	V_P	—	Power supply pin for charge pump output.
4	5	V_{CC}	—	Power supply pin.
5	6	D_O	O	Internal charge pump output pin. The phase characteristic is inverted according to the FC pin setting.
6	7	GND	—	GND pin
7	8	LD	O	Lock detector output pin. When locked: LD = “H”; when unlocked: LD = “L”.
8	10	fin	I	Prescaler input pin. The pin must be AC-coupled for input.
9	11	Clock	I	Clock input pin for 19-bit shift registers. The shift register reads data at the rise of the clock pulse.
10	13	Data	I	Binary-coded serial data input pin. The last bit in the data is a control bit. Control bit = “H”: Sends data to the 16-bit latch. “L”: Sends data to the 18-bit latch.
11	14	LE	I	Load enable signal input pin. When LE = “H”, the pin sends the contents of the shift register to the latch according to the control bit.
12	15	FC	I	Phase comparator phase switching pin. When FC = “L”, the pin inverts the characteristics of the charge pump and the phase comparator. The pin also switches the fout pin (test pin) output between fr and fp.
14	17	fout	O	Phase comparator input monitor pin. The pin outputs the reference divider output (fr) or programmable divider output (fp) signal according to the FC pin input level. FC = “H”: Equivalent to fr output FC = “L”: Equivalent to fp output This pin is an N-channel open-drain output.
15	18	øP	O	Phase comparator output pin for external charge pump. The phase characteristic is inverted according to the FC pin setting. This pin is an N-channel open-drain output.
16	20	øR	O	Phase comparator output pin for external charge pump. The phase characteristic is inverted according to the FC pin setting. This pin is a CMOS output.
13	2, 9, 12, 16, 19	N.C.	—	No connection

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min.	Max.	
Power supply voltage	V_{CC}	–0.5	5.0	V
	V_P	V_{CC}	5.5	V
Output voltage	V_O	–0.5	V_{CC} + 0.5	V
Output current	I_O	–10	10	mA
Open-drain voltage	V_{OOP}	–0.5	6.0	V
Storage temperature	Tstg	–55	+125	°C

Note: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_P	V_{CC}	—	5.0	V
Input voltage	V_{IN}	GND	—	V_{CC}	V
Operating temperature	Ta	–40	—	+85	°C

HANDLING PRECAUTIONS

Although the MB15A03 contains an antistatic element to prevent electrostatic breakdown and the circuitry has been improved in electrostatic protection, observe the following precautions when handling the device:

- Store or carry this device in a conductive case.
- As this is a static-sensitive device, take proper anti-ESD precautions. Ensure that personnel and equipment are properly grounded. Cover workbenches with grounded conductive mats.
- Always turn the power supply off before inserting or removing the device from its socket.
- Protect leads with a conductive sheet when handling or transporting PC boads with devices.

■ ELECTRICAL CHARACTERISTICS

(V_{CC} = 2.7 V to 3.6 V, Ta = –40°C to +85°C)

Parameter		Symbol	Condition	Value			Unit
				Min.	Typ.	Max.	
Power supply current*1		I_{CC}	—	—	6.5	—	mA
Power saving current		I_{PS}	—	—	100	—	µA
Operating frequency	fin*2	fin	—	300	—	1100	MHz
	OSC_{IN}	f_{OSC}	—	—	12	20	MHz
Input sensitivity	fin	P_{fin}	50 Ω system	–10	—	6	dBm
	OSC_{IN}	V_{OSC}	—	0.5	—	—	V_{P-P}
High-level input voltage	Data, Clock, LE, FC	V_{IH}	—	0.7 × V_{CC}	—	—	V
Low-level input voltage		V_{IL}	—	—	—	0.3 × V_{CC}	V
High-level input current	Clock, Data	I_{IH}	—	—	—	1.0	µA
Low-level input current		I_{IL}*3	—	–1.0	—	—	µA
Input current	OSC_{IN}	I_{OSC}*3	—	—	±50	—	µA
High-level output voltage	Excluding D_O and OSC_{OUT}	V_{OH}*4	—	2.1	—	—	V
Low-level output voltage		V_{OL}*5	—	—	—	0.4	V
High impedance cutoff current	D_O, fout, øP	I_{OFF}*6	—	—	—	1.1	µA
Output currrent	Excluding D_O and OSC_{OUT}	I_{OH}*3	V_{CC} = 3.0 V	–1.0	—	—	mA
		I_{OL}		—	—	1.0	mA

*1: Assuming the PLL lock conditions: fin = 1.1 GHz, f_{OSC} = 12 MHz, V_{CC} = 3.0 V

*2: The fin pin must be AC-coupled. The minimum operating frequency assumes coupling at 1000 pF.

*3: A minus sign (–) indicates the direction of the signal flowing from the IC.

*4: Assuming V_{CC} = 3.0 V and I_{OH} = –1 mA

*5: Assuming V_{CC} = 3.0 V and I_{OL} = 1 mA

*6: V_{CC} = 3.6 V, V_P = V_{CC} to 5.0 V, V_{OOP} = GND to 6.0 V

■ FUNCTIONAL DESCRIPTIONS

1. Pulse Swallow Function

For the pulse swallow function, select the respective setting values using the following equation:

$$f_{VCO} = [(P \times N) + A] \times f_{OSC} \div R$$

f_{VCO}	:	Output frequency of external VCO
P	:	Divide ratio of prescaler (64 or 128)
N	:	Divide ratio of 11-bit programmable counter (5 to 2047)
A	:	Divide ratio of 7-bit swallow counter (0 to 127, where A < N)
f_{OSC}	:	Reference oscillation frequency (OSC_{IN} input frequency)
R	:	Divide ratio of 14-bit programmable reference counter (6 to 16383)

2. Serial Data Input Method

Serial data is processed using three input pins (Data, Clock, and LE) to control the 16-bit reference divider and the 18-bit programmable divider separately.

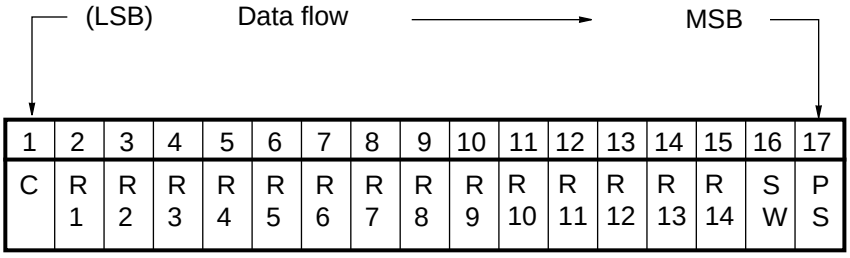
Binary serial data is entered through the Data pin.

Serial data is transfered to the internal shift register in sequence on the rising edge of each clock. When the load enable signal is high, the input data is transferred to the latch according to the control bit.

Control bit = “H” → Transfer to the 16-bit latch
Control bit = “L” → Transfer to the 18-bit latch

(1) Serial Data Format

Programmable Reference Counter

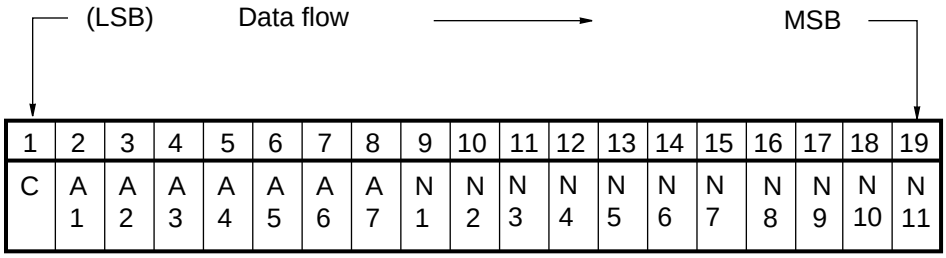


1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
C	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	SW	PS

R1 to R4	:	Divide ratio setting bits for the programmable reference counter (6 to 16,383)
SW	:	Divide ratio setting bits for the prescaler
PS	:	Power saving control bit
C	:	Control bits

Note: Start data input with MSB first.

Programmable Divider



1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
C	A1	A2	A3	A4	A5	A6	A7	N1	N2	N3	N4	N5	N6	N7	N8	N9	N10	N11

A1 to A7 : Divide ratio setting bits for the swallow counter (set value: 0 to 127)
N1 to N11 : Divide ratio setting bits for the programmable counter (set value: 5 to 2047)
C : Control bits

Note: Start data input with MSB first.

(2) Data Settings

- **Binary 14-bit reference counter (R1 to R14)**

Divide ratio	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Note: A divide ratio less than 6 is prohibited.

- **Binary 11-bit programmable counter (N1 to N11)**

Divide ratio	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: A divide ratio less than 5 is prohibited.

- **Binary 7-bit swallow counter (A1 to A7)**

Divide ratio	A7	A6	A5	A4	A3	A2	A1
0	0	0	0	0	0	0	0
1 • • • 127	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	0 • • • 1	1 • • • 1

- **Prescaler (SW)**

Divide ratio	SW
64/65	1
128/129	0

- **Power saving (intermittent operation) control (PS)**

Mode	PS
Normal mode	1
Power saving mode	0

Note: Be sure to reset the PS bit to 0 immediately after turning the power on.

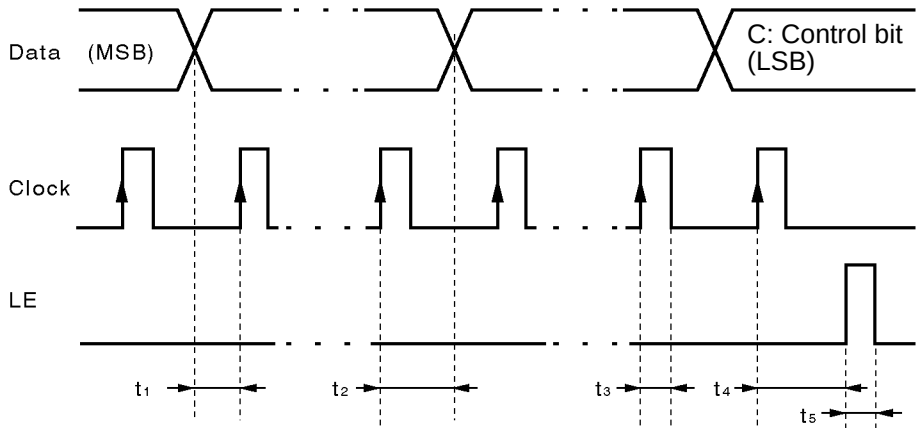
Users can operate internal circuits only when required and halt them when not required. This process reduces the overall circuit power consumption (intermittent operation).

However, letting the LSI simply start operating the halted circuit results in excessive error signal output from the phase comparator unlocking the PLL. This is because the reference frequency (fr) and comparative frequency (fp) inputs to the phase comparator have an undefined phase relationship even when the two frequencies are the same.

To solve this problem, the MB15A03 provides intermittent operation control to suppress variation in the locked frequency by forcibly aligning the phases when the circuit returns from the halted state.

(3) Serial Data Input Timing

t_1, t_4 > 100 ns, t_2 > 1000 ns, t_3 > 300 ns, t_5 > 800 ns



Note: Serial data is fetched on the rising edge of the clock.

3. Relationships between FC Pin Inputs and Phase Characteristics

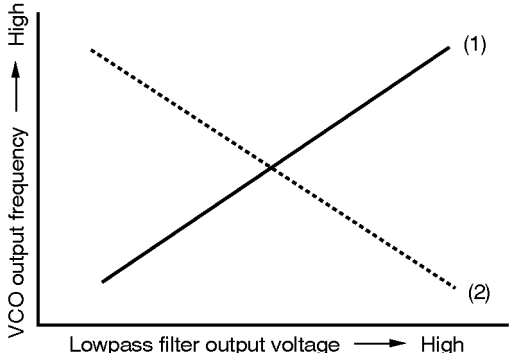
The FC pin is the phase switching pin for the phase comparator. Controlling the FC pin input allows the characteristics of the internal charge pump output (D_O) and external charge pump outputs (øR and øP) to be selected. Also, the phase comparator input monitor pin (fout) is controlled through the FC pin.
The following table shows the relationship between FC pin inputs and D_O, øR, øP, and fout:

Phase comparator input	FC: "H"				FC: "L"			
	D_O	øR	øP	fout	D_O	øR	øP	fout
fp < fr	H	L	L	fr	L	H	Z	fp
fr < fp	L	H	Z		H	L	L	
fp = fr	Z	L	Z		Z	L	Z	

Z: High impedance

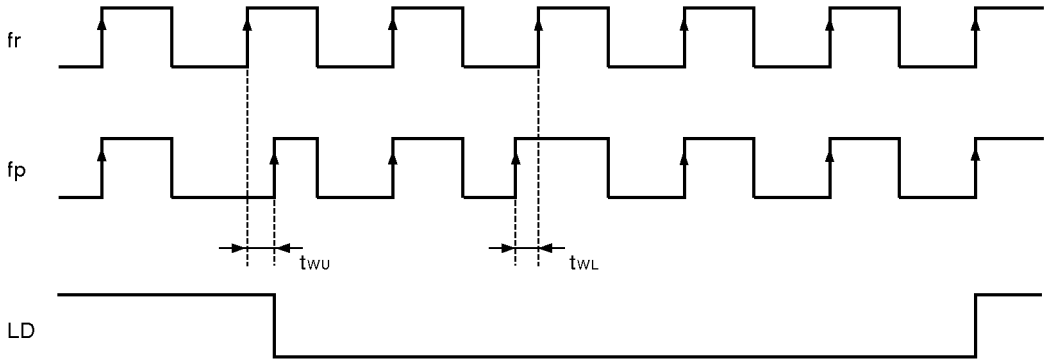
When designing a PLL frequency synthesizer, control the FC pin according to the lowpass filter and VCO polarities.

When the LPF/VCO polarity is (1)
(FC: "H")
When the LPF/VCO polarity is (2)
(FC: "L")

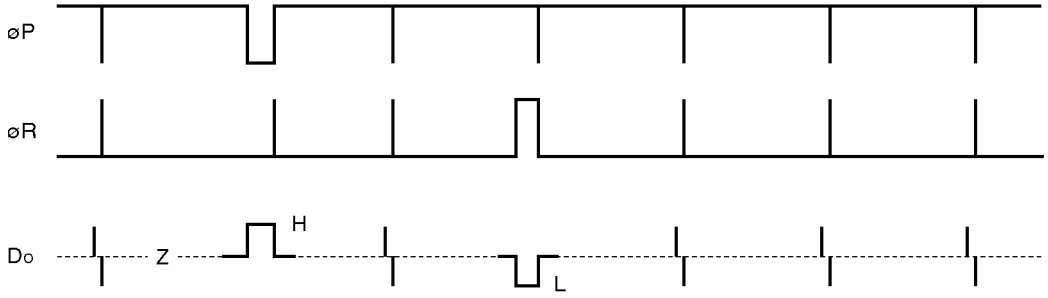


Note: Take note of the polarity when using an active lowpass filter.

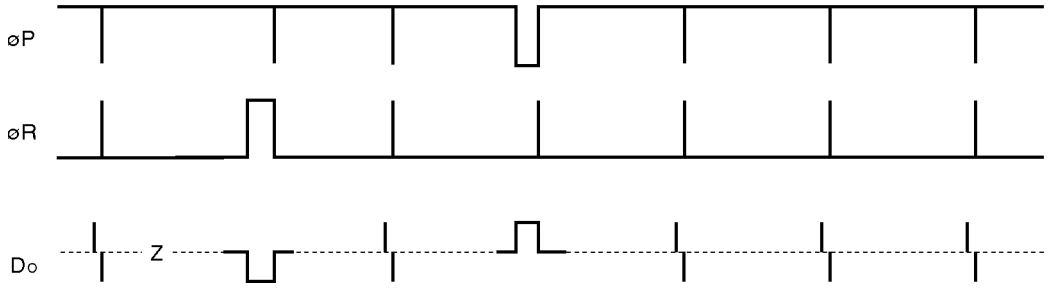
■ PHASE COMPARATOR OUTPUT WAVEFORMS



• When the FC bit = "H"



• When the FC bit = "L"

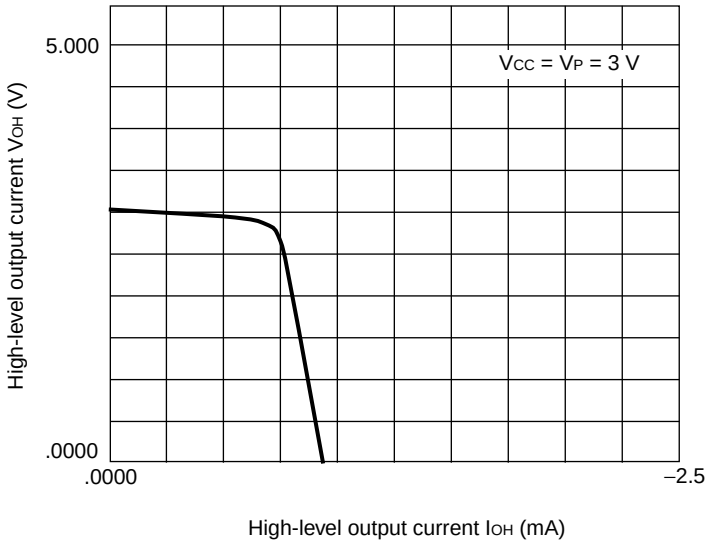


Note: • A phase error is detected between -2π and $+2\pi$. The phase comparator conversion gain is $Vp/4\pi$.
- The LD output becomes low when the phase difference is t_{WU} or more. The LD output becomes high when the phase difference is equal to or smaller than t_{WL} and continues to be so for three cycles or more.
- t_{WU} and t_{WL} depend on the OCS_{IN} input frequency as follows:
  $t_{WU} \geq 8/f_{OSC}$ [s] ..... When f_{OSC} = 12.8 MHz, $t_{WU} \geq 625$ ns
  $t_{WL} \leq 16/f_{OSC}$ [s] ..... When f_{OSC} = 12.8 MHz, $t_{WL} \leq 1250$ ns

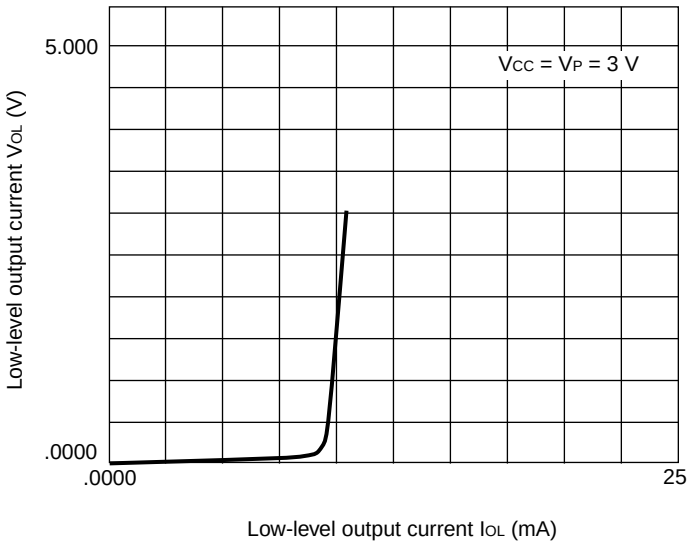
■ TYPICAL CHARACTERISTIC CURVES

1. D_O Output Current Characteristics

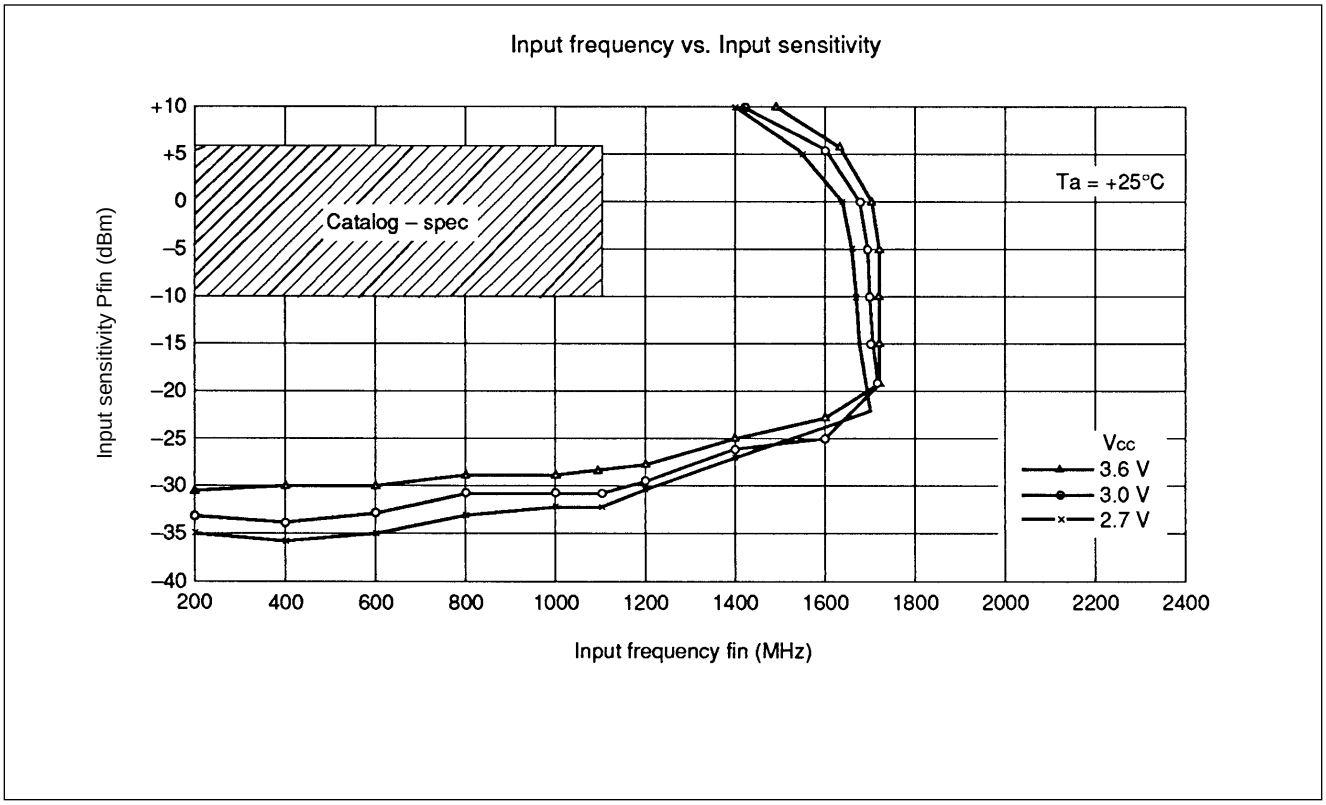
I_{OH} vs. V_{OH} characteristics



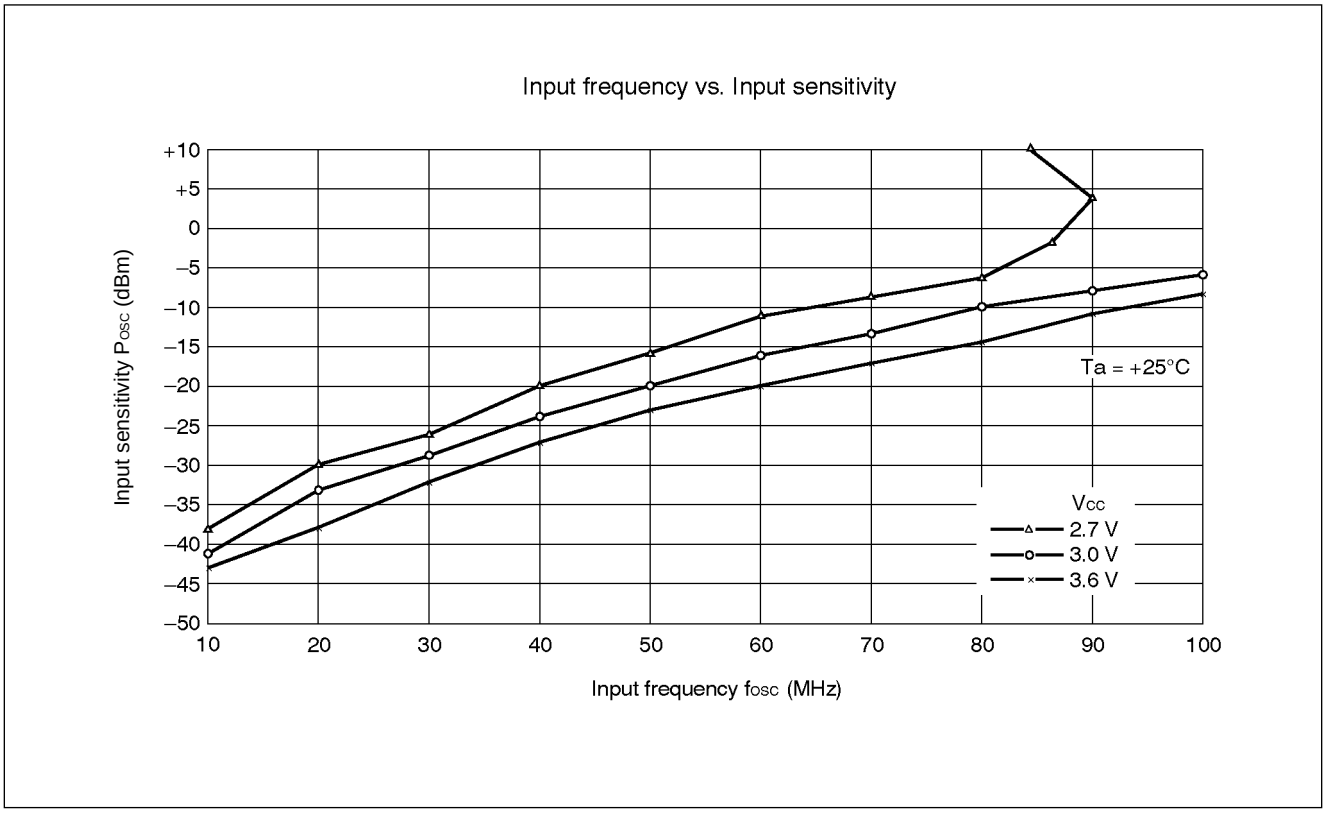
I_{OL} vs. V_{OL} characteristics



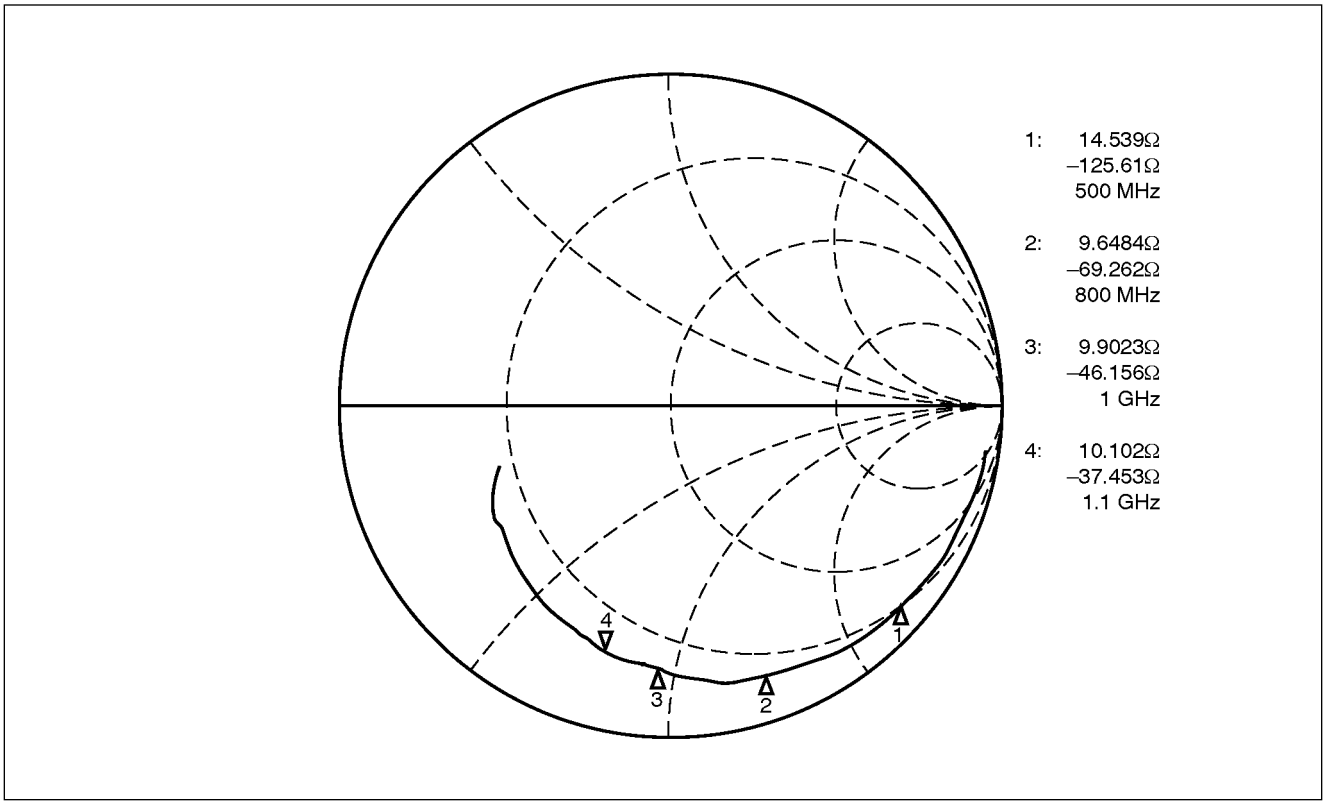
2. fin Input Sensitivity Characteristics



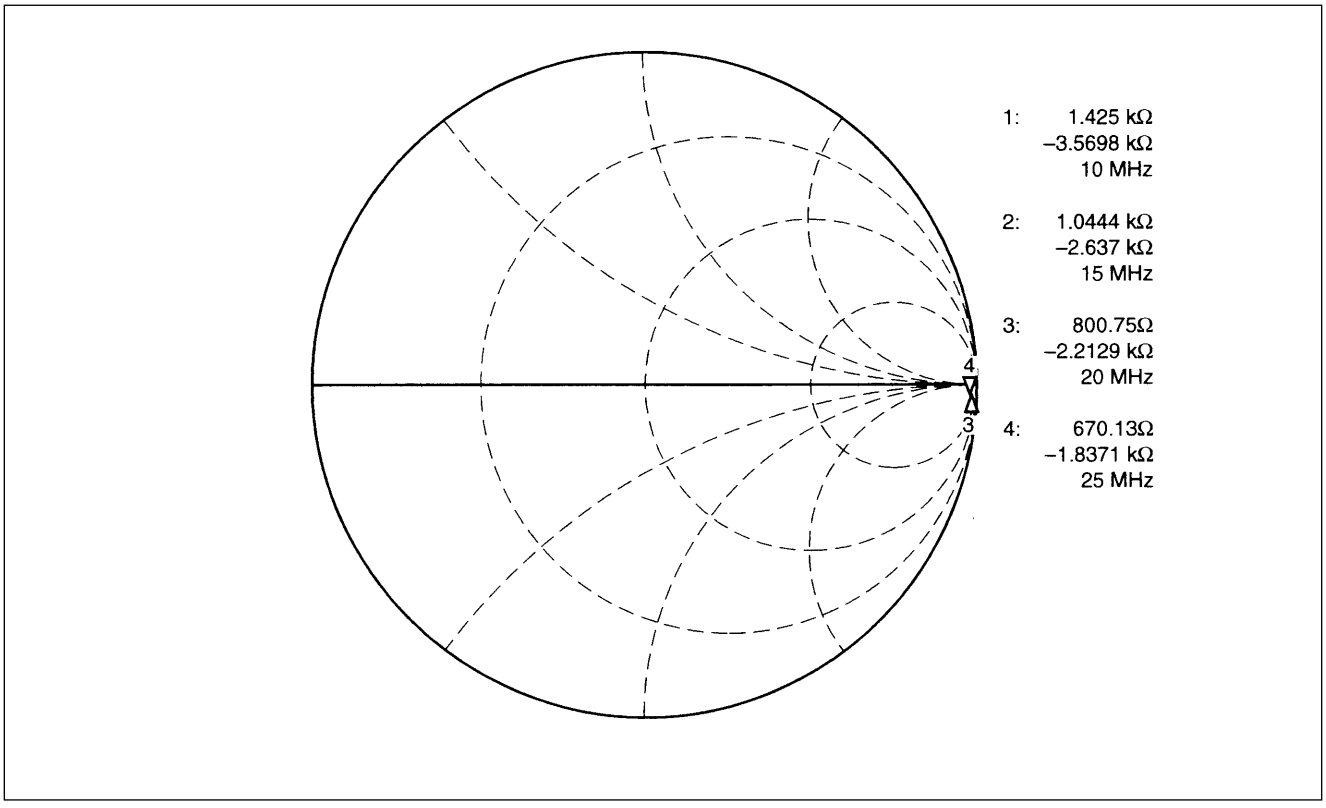
3. OSC_{IN} Input Sensitivity Characteristics



4. fin Input Impedance Characteristics



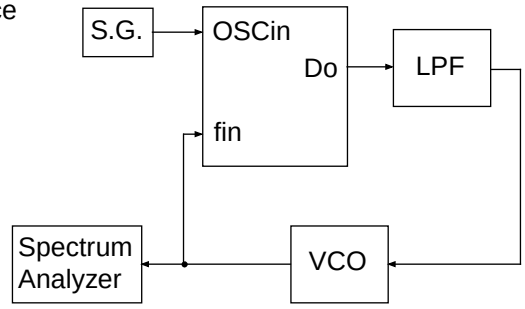
5. OSC_{IN} Input Impedance Characteristics



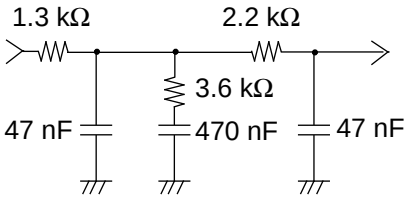
■ REFERENCE INFORMATION

Typical plots measured with the test circuit are shown below. Each plot shows lock up time, phase noise, and reference leakage.

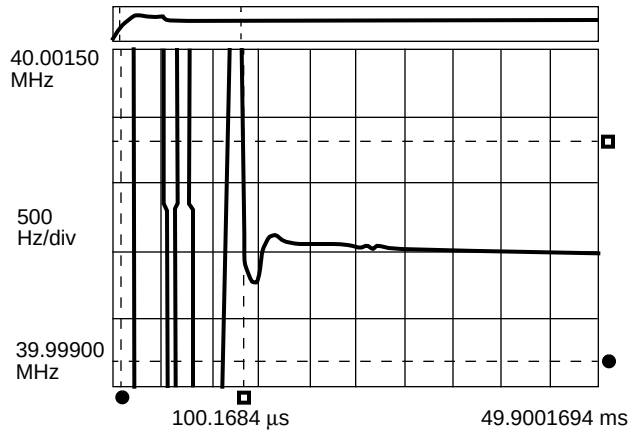
Test Circuit



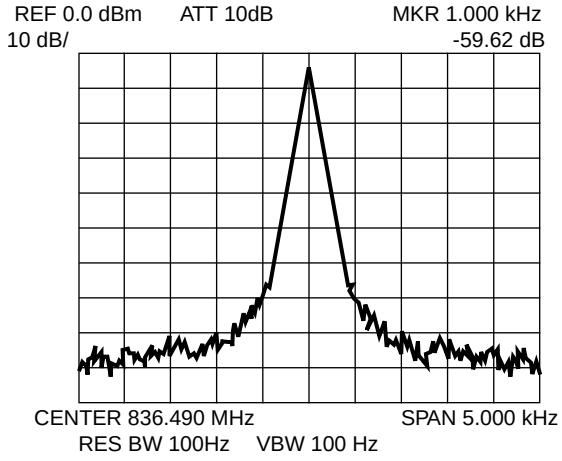
- f_{VCO} = 836.49 MHz
- K_V = 12 MHz/V
- f_r = 30 kHz
- f_{OSC} = 15.36 MHz
- LPF



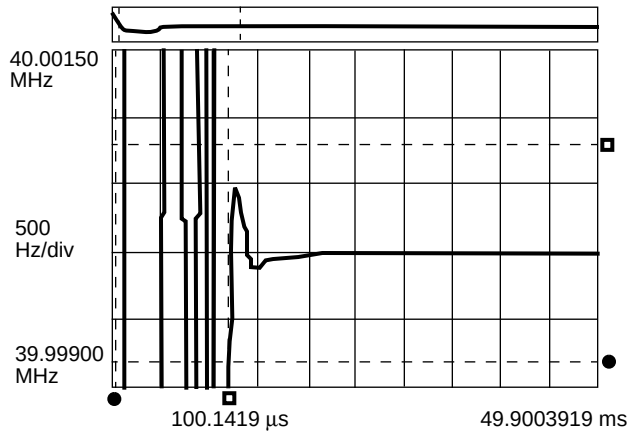
PLL Lock Up Time = 12.8 ms
(824.010 MHz → 848.97 MHz, within ±800 Hz)



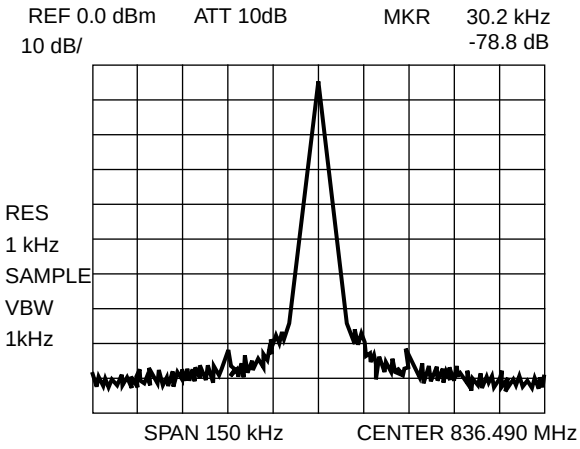
PLL Phase Noise
@ within loop band = 79.6 dBc/Hz



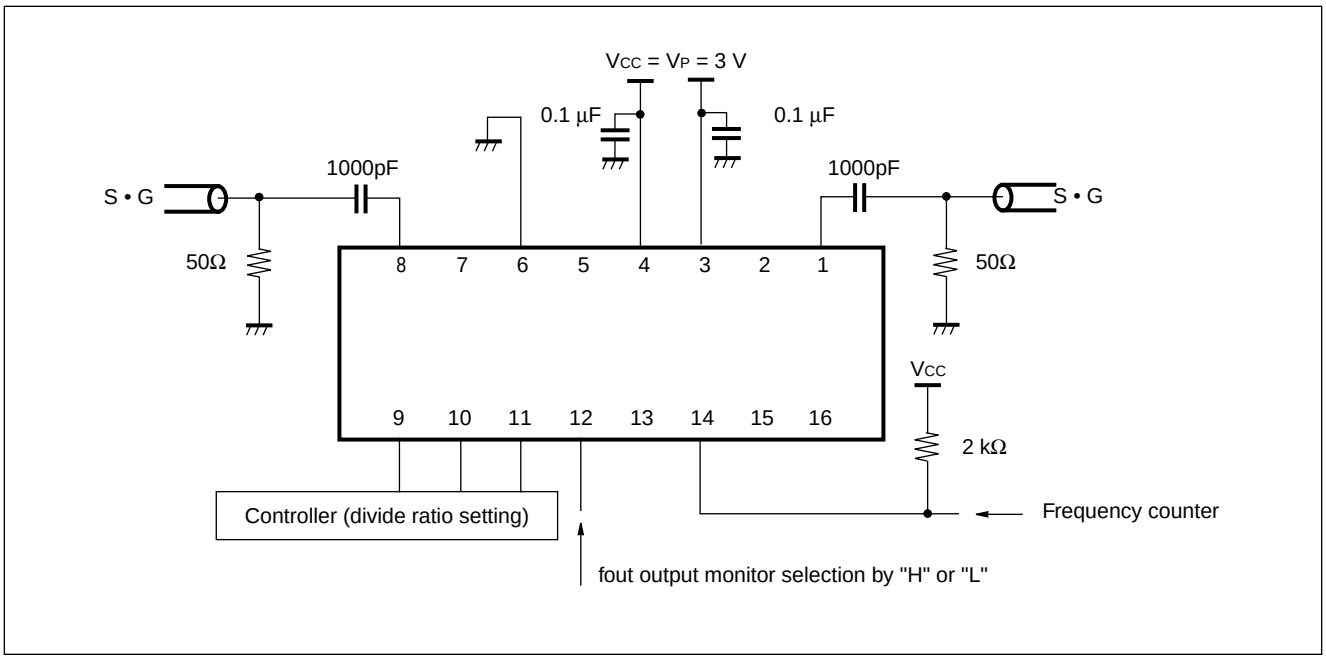
PLL Lock Up Time = 11.6 ms
(848.97 MHz → 824.010 MHz, within ±800 Hz)



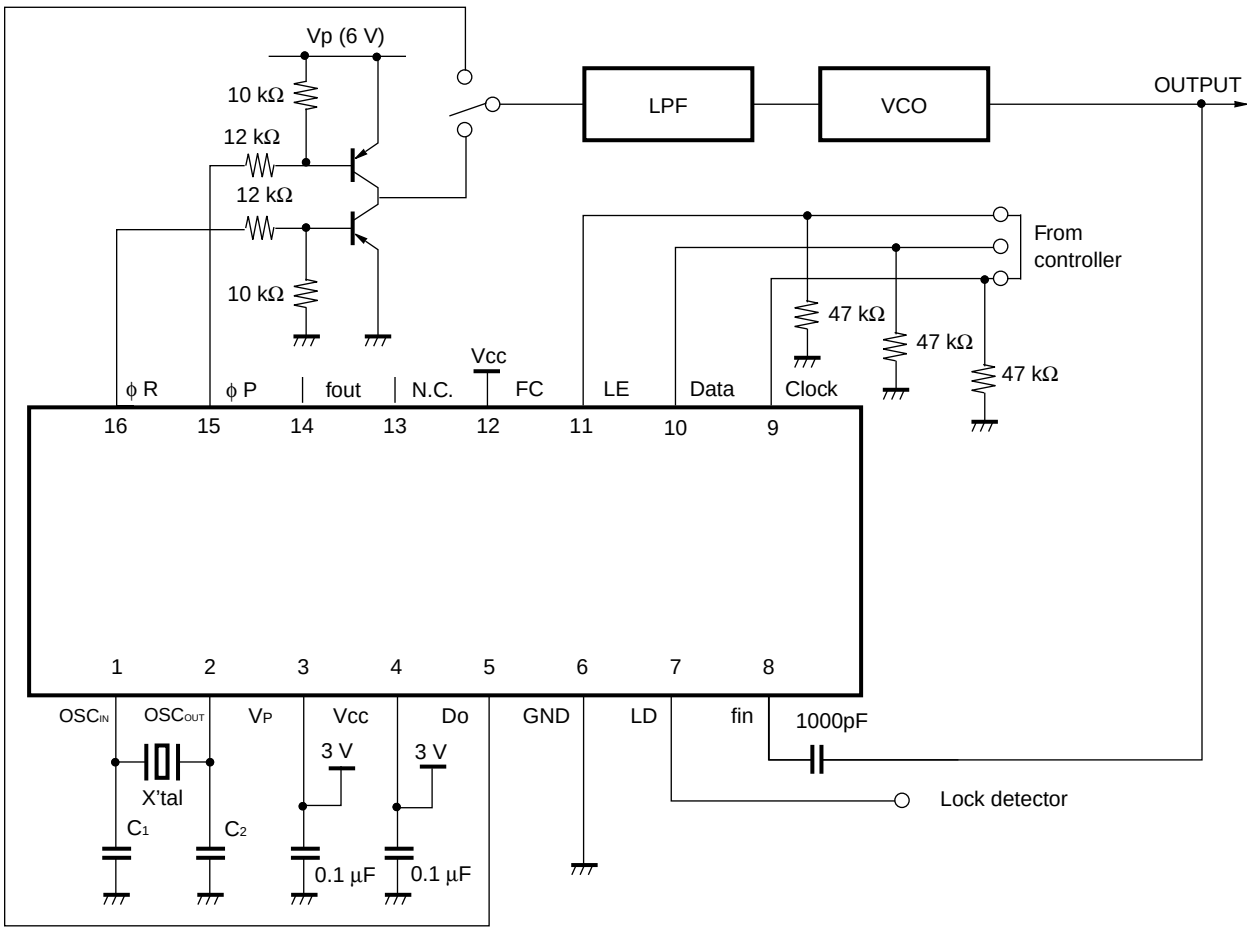
PLL Reference Leakage
@ 30 kHz offset = 78.8 dBc



■ TEST CIRCUIT EXAMPLE (fin/OSC_{IN} Input Sensitivity Measurement)



■ APPLICATION EXAMPLE (16-Pin Package)



V_P : 5 V max.
C1, C2 : Determined by the crystal oscillator.
Clock, Data, LE : Insert a pull-down resistor if an input is open.

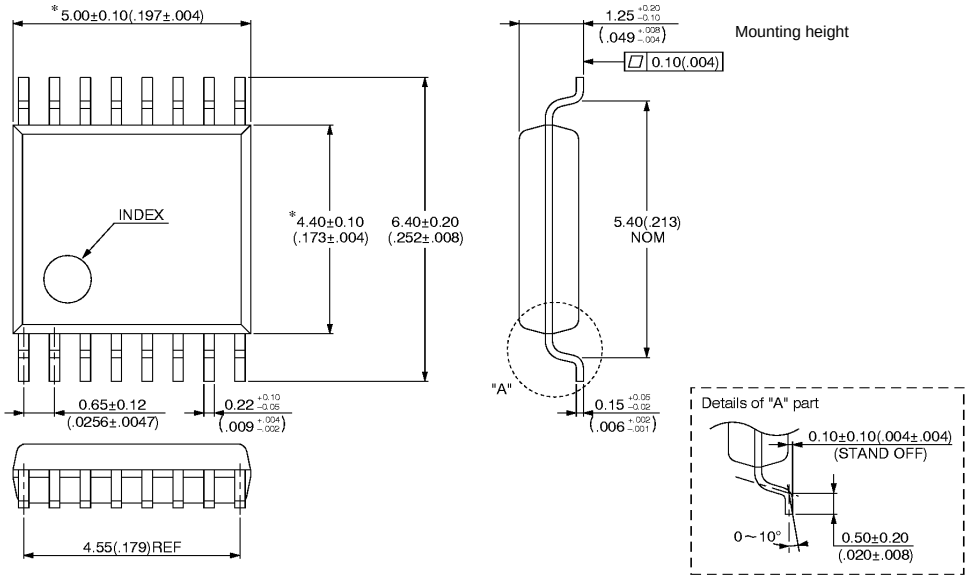
■ ORDERING INFORMATION

Part number	Package	Remarks
MB15A03PFV1	16-pin, plastic SSOP (FPT-16P-M05)	
MB15A03PFV2	20-pin, plastic SSOP (FPT-20P-M03)	

■ PACKAGE DIMENSIONS

16-pin, plastic SSOP
(FPT-16P-M05)

*: These dimensions do not include resin protrusion.



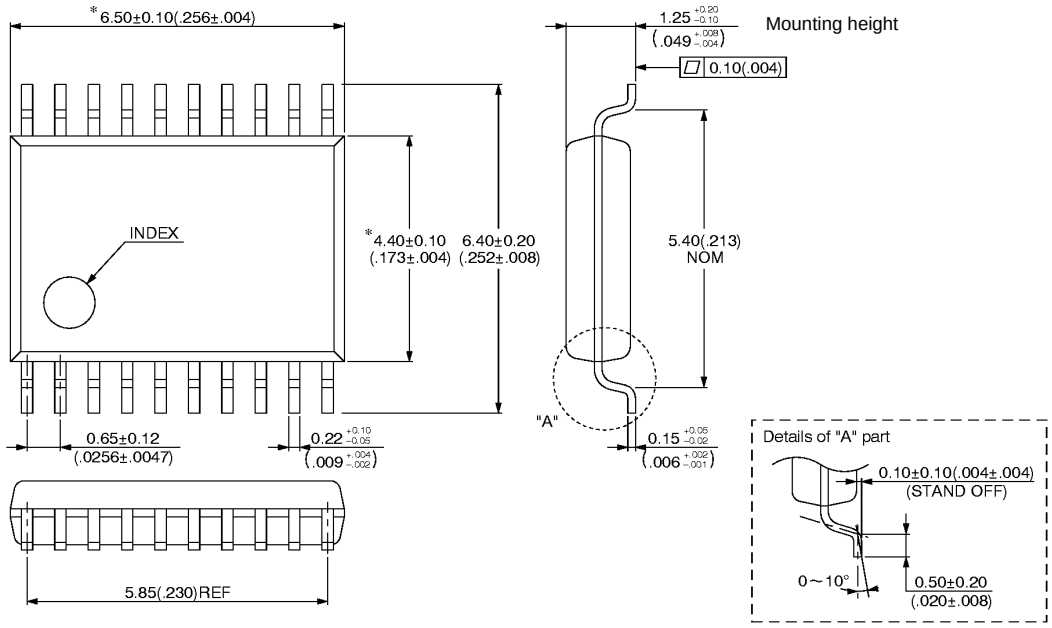
Dimensions in mm (inches)

(Continued)

(Continued)

20-pin, plastic SSOP
(FPT-20P-M03)

*: These dimensions do not include resin protrusion.



Dimensions in mm (inches)

MB15A03

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