DS04–21323–2aE

FUJITSU

DATA SHEET

MB1516A *ASSP*

1.1GHz High-Speed Tuning PLL Frequency Synthesizer

DESCRIPTION

The Fujitsu MB1516A is a serial input phase-locked loop (PLL) frequency synthesizer with a pulse-swallow function. MB1516A achieves the low noise performance as well as the high–speed lock-up which is required for digital mobile communications.
The MB1516A can operate from a single +3 V supply. Fujitsu's advanced technology achieves an Icc of 6.5 mA (typical).

FUNCTION

- High operating frequency : f_{IN} = 1.1 GHz (P_{IN} = –10 dBm)
- Pulse-swallow function : High-speed dual-modulus prescaler with selectable 64/65 and 128/129 divide ratios
- Low supply current : I_{CC} = 6.5 mA typ. at 3 V
- Power saving funtion : I_{PS} = 100 μA typ.
- Serial input, 18-bit programmable divider consisting of:
  Binary 7-bit swallow counter : 0 to 127
  Binary 11-bit programmable counter : 5 to 2,047
- Serial input 16-bit programmable reference divider consisting of:
  Binary 14-bit programmable reference counter: 6 to 16,383
  1-bit switch counter sets prescaler divide ratio
  1-bit power saving function control
- On-chip high performance charge pump circuit and phase comparator, achieving high-speed lock-up and low phase noise
- Two types of phase comparator outputs selectable
  On-chip charge pump output
  Output for an external charge pump
- Wide operating temperature range: –40 to +85°C
- Plastic 16–pin SSOP (shrink small outline) package (Suffix : –PFV)

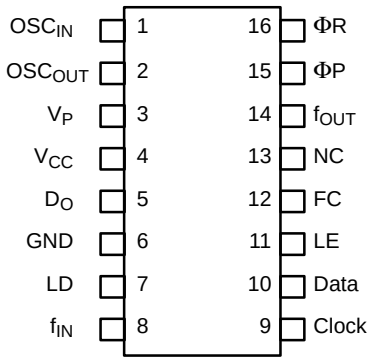
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Parameter	Symbol	Rating	Unit	Remark
Supply voltage	V_{CC}	–0.5 to +5.0	V	
	V_P	V_{CC} to 5.5	V	
Output voltage	V_O	–0.5 to V_{CC} +0.5	V	
Open drain voltage	V_{OOP}	–0.5 to 6.0	V	ΦP, fout
Output current	I_O	±10	mA	
Storage temperature	Tstg	–55 to +125	°C	

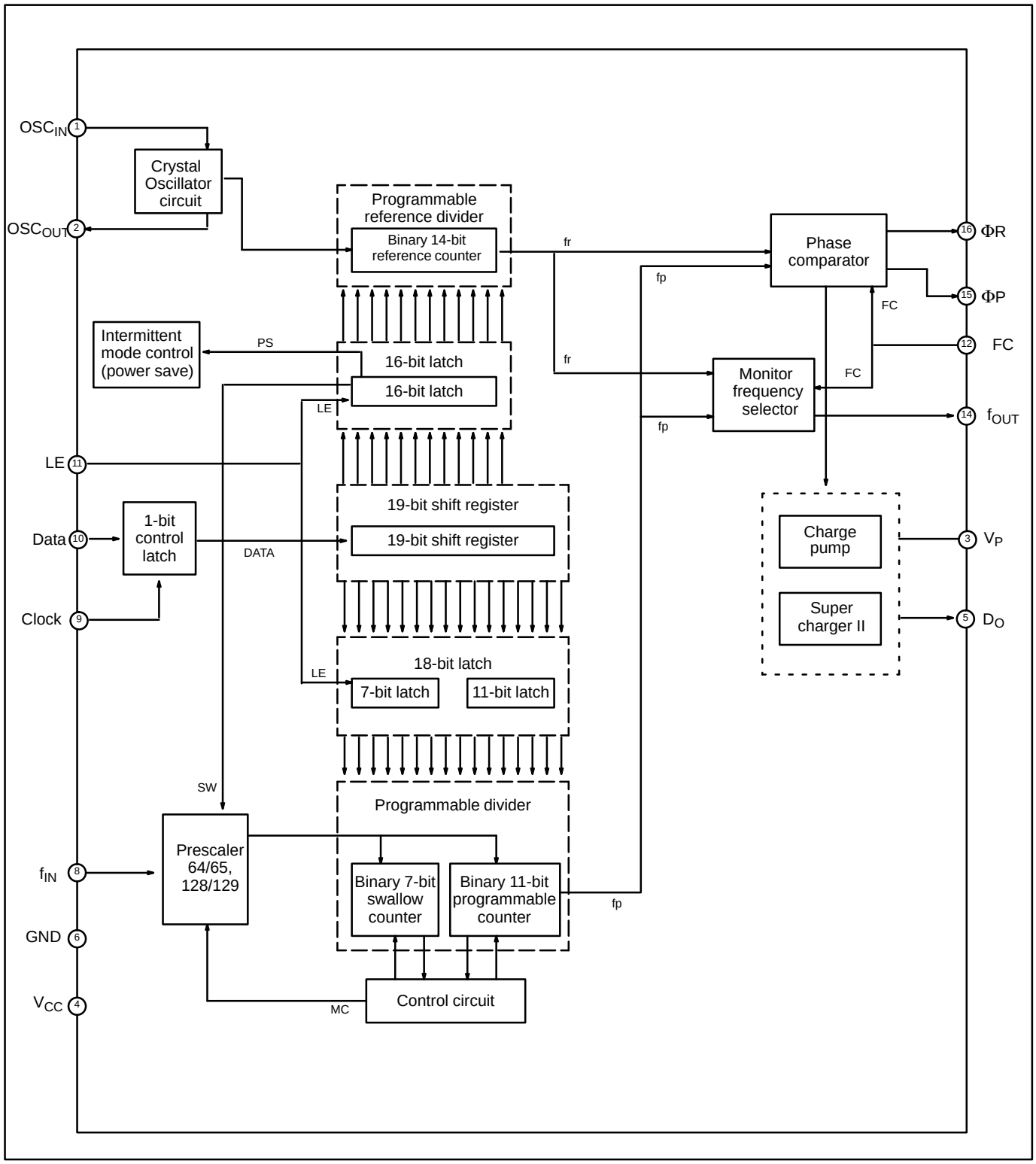
NOTE: Permanent device damage may occur if the above **Absolute Maximum Ratings** are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PIN ASSIGNMENT

(TOP VIEW)



BLOCK DIAGRAM



PIN DESCRIPTION

Pin No.	Pin name	I/O	Description
1	OSC_{IN}	I	Programmable reference divider input Oscillator input Connection for external crystal or TCXO.
2	OSC_{OUT}	O	Oscillator output Connection for external crystal.
3	V_P	–	Power supply input for charge pump
4	V_{CC}	–	Power supply
5	D_O	O	Charge pump output Phase of charge pump can be reversed based on FC input.
6	GND	–	Ground
7	LD	O	Lock detector output The output level is usually high. Only when there is a phase error between fr and fp, LD becomes low for the period corresponding to the error.
8	f_{IN}	I	Prescaler input Connection with an external VCO should be done AC coupled.
9	Clock	I	Clock input for 19-bit shift register Data is shifted into the shift register on the rising edge of the clock.
10	Data	I	Serial data input using binary code The last bit of the data is a control bit. When the control bit is high, data is transmitted to the 16-bit latch. When it is low, data is transmitted to the 18-bit latch.
11	LE	I	Load enable signal input (with internal pull up resistor) When LE is high, the data of the shift register are transferred to a latch, depending on the control bit in the serial data.
12	FC	I	Phase switch input for phase comparator (with internal pull-up resistor) When FC is low, the characteristics of the charge pump and phase comparator are reversed The FC input signal is also used to control the f_{OUT} pin (test pin) output (f_R or f_P).
13	NC	–	No connection
14	f_{OUT}	O	Monitor pin of phase comparator When FC is high, f_{OUT} outputs programmable reference divider output(fr). When FC is low, f_{OUT} outputs programmable divider output(fp).
15	ΦP	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input. ΦP pin is a N-ch open drain output.
16	ΦR	O	Phase comparator output for an external charge pump Phase of the output is reversed depending on FC input. ΦR pin is a C-MOS output.

FUNCTION DESCRIPTIONS

Pulse swallow function

The divide ratio can be calculated using the following equation:

$f_{VCO} = [(M \times N) + A] \times f_{OSC} \div R \quad (A < N)$

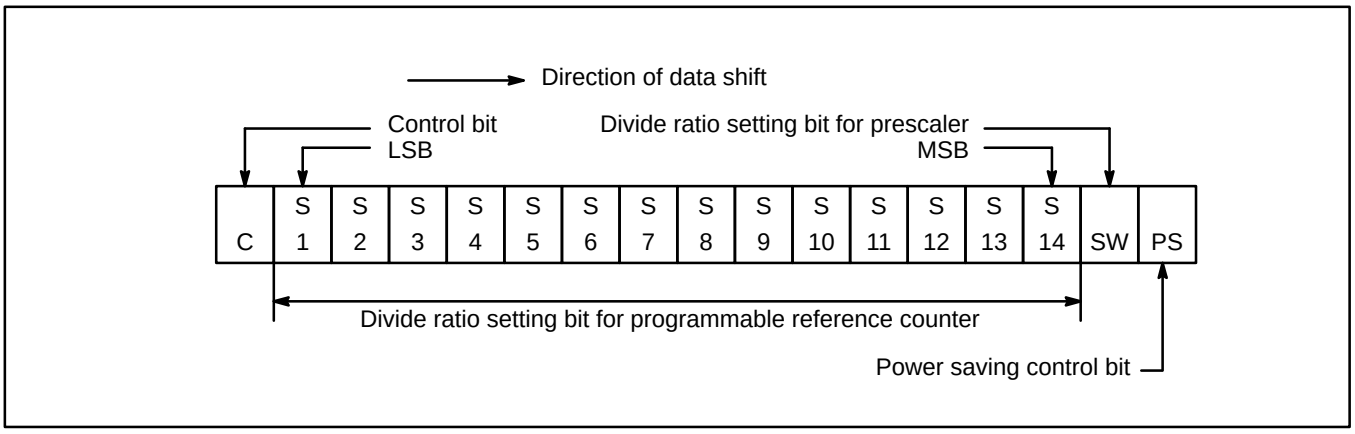
- f_{VCO} : Output frequency of external voltage controlled oscillator (VCO)
- N : Preset divide ratio of binary 11-bit programmable counter (5 to 2,047)
- A : Preset divide ratio of binary 7-bit swallow counter ($0 \le A \le 127$)
- f_{OSC} : Output frequency of the reference frequency oscillator
- R : Preset divide ratio of binary 14-bit programmable reference counter (6 to 16,383)
- M : Preset divide ratio of modules prescaler (64 or 128)

Serial data input

Serial data is processed using the Data, Clock, and LE pins. Serial data controls the 16-bit programmable reference divider and 18-bit programmable divider separately.
Binary serial data is entered via the Data pin.
One bit of data is shifted into the internal shift register on the rising edge of the clock. When the load enable pin is high or open, stored data is latched depending on the control data as follows:

Control data	Destination of serial data
H	16 bit latch
L	18 bit latch

(a) Programmable reference divider ratio
The programmable reference divider consists of a 16-bit latch and a 14-bit reference counter. The serial 17-bit data format is shown below:



- 14-bit programmable reference counter divide ratio

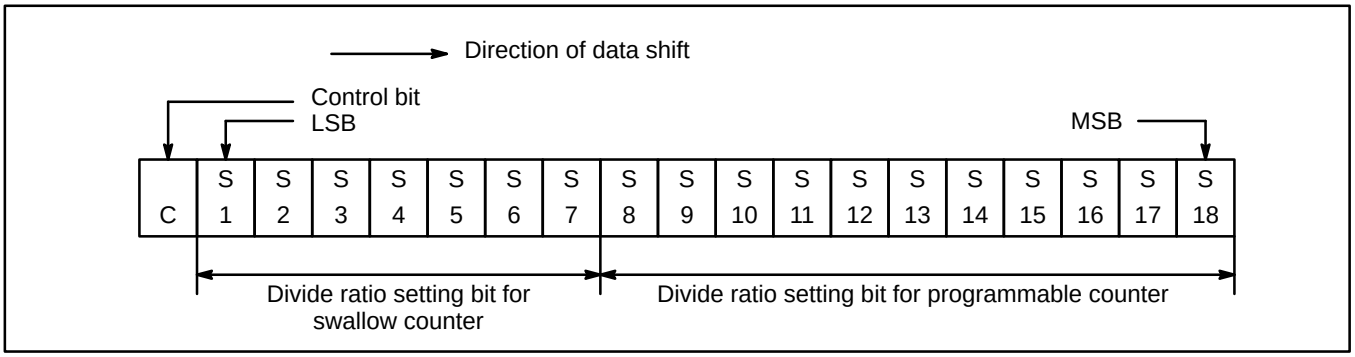
Divide ratio R	S 14	S 13	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
6	0	0	0	0	0	0	0	0	0	0	0	1	1	0
7	0	0	0	0	0	0	0	0	0	0	0	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
16383	1	1	1	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 6 to 16,383)

Notes: 1. Divide ratios less than 6 are prohibited.
2. SW : This bit selects the divide ratio of the prescaler.
   Low: 128 or 129
   High: 64 or 65
3. S1 to S14: These bits select the divide ratio of the programmable reference counter (6 to 16,383).
4. C: Control bit: Set high.
5. PS: This bit controls stand by mode.
   High : Nomal mode
   Low : Stand by mode
6. Start data input with MSB first .

(b) Programmable divider divide ratio

The programmable divider consists of a 19-bit shift register, a 18-bit latch, a 7-bit swallow counter, and a 11-bit programmable counter. The serial 19-bit data format is shown below:



- 7-bit swallow counter divide ratio

Divide ratio A	S 7	S 6	S 5	S 4	S 3	S 2	S 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

(Divide ratio = 0 to 127)

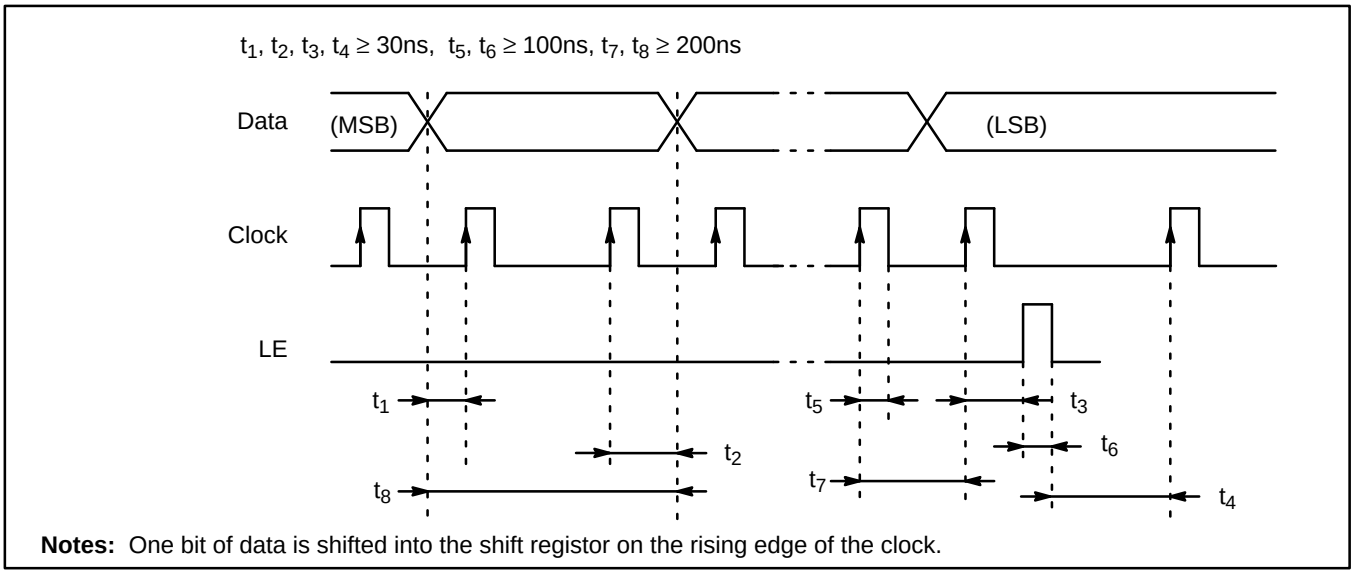
- 11-bit programmable counter divide ratio

Divide ratio N	S 18	S 17	S 16	S 15	S 14	S 13	S 12	S 11	S 10	S 9	S 8
5	0	0	0	0	0	0	0	0	1	0	1
6	0	0	0	0	0	0	0	0	1	1	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

(Divide ratio = 5 to 2,047)

Notes: 1. Divide ratios less than 5 are prohibited for 11–bit programmable counter.
2. S1 to S7: These bits select the divide ratio of swallow counter (0 to 127).
3. S8 to S18: These bits select the divide ratio of programmable counter (5 to 2,047).
4. C: Control bit: (Set low)
5. Start data input with MSB first.

Serial data input timing



Notes: One bit of data is shifted into the shift registor on the rising edge of the clock.

Power saving mode (Intermittent operation control circuit)

Setting PS bit to Low, MB1516A enters into power saving mode resultatly current sonsumption can be limited to 100µA (typ.). Setting PS bit to High, power saving mode is released so that the device works normally.
In addition, the intermittent operation control circuit is included which helps smooth start up from stand by mode. The power consumption can be reduced by the intermittent operation that powering down or waking up parts of the PLL circuitry. If a PLL is powered up uncontrolled, the resulting phase comparator output signal is unpredictable due to an undefined phase relation between reference frequency (f_R) and comparison frequency (f_P) and may in the worst case take longer time for lock up of the loop. To prevent this, the intermittent operation control circuit enforces a limited error signal output of the phase detector during power up, thus keeping the loop locked.

Relation between the FC input and phase characteristics

The FC pin changes the phase characteristics of the phase comparator. Both the internal charge pump output level (D_O) and the phase comparator output (ΦR, ΦP) are reversed depending on the FC pin input level. Also, the monitor pin (f_{OUT}) output is controlled by the FC pin. The relationship between the FC input level and each of D_O, ΦR, and ΦP is shown below:

	FC = High or open				**FC = Low**			
	Do	ΦR	ΦP	f_{OUT}	Do	ΦR	ΦP	f_{OUT}
$f_R > f_P$	H	L	L	(fr)	L	H	Z(∗1)	(fp)
$f_R < f_P$	L	H	Z(∗1)	(fr)	H	L	L	(fp)
$f_R = f_P$	Z(∗1)	L	Z (∗1)	(fr)	Z(∗1)	L	Z(∗1)	(fp)

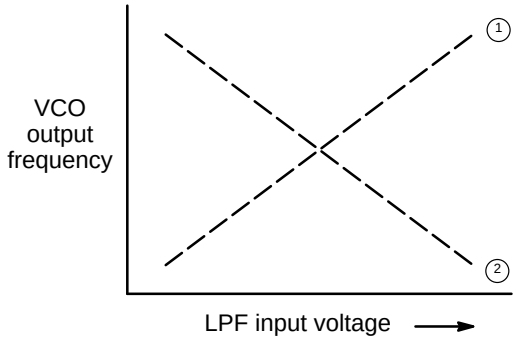
∗1: High impedance

When designing a synthesizer, the FC pin setting depends on the VCO and LPF characteristics.

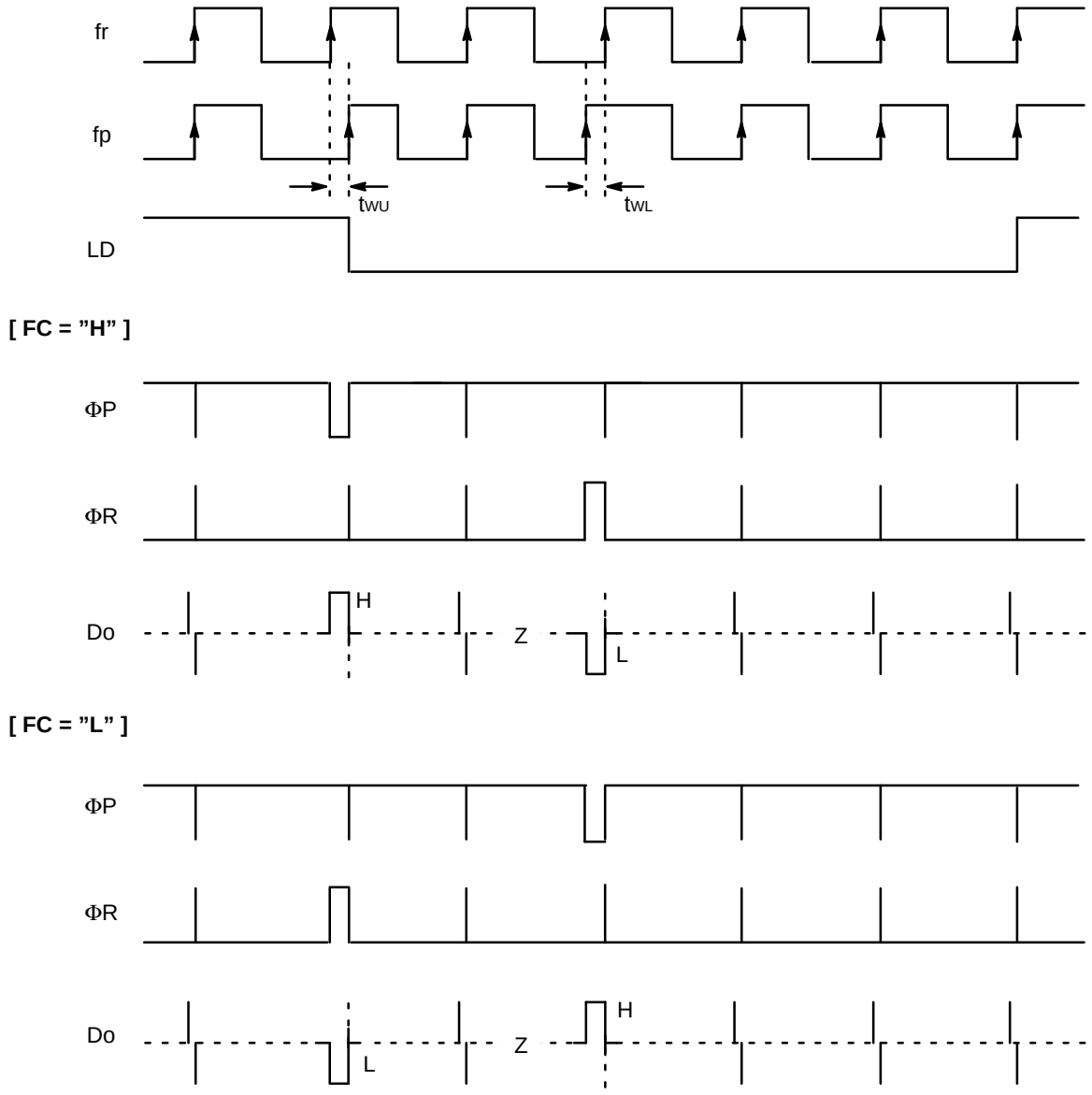
∗: When the LPF and VCO characteristics are similar to ①, set FC high or open.

∗: When the VCO characteristics are similar to ②, set FC low.

PLL → LPF → VCO



Phase comparator output waveforms



Notes: 1. Phase difference detection range: -2π to $+2\pi$

2. LD output becomes low when phase is t_{WU} or more. LD output becomes high when phase error is t_{WL} or less and continues to be so for three cysles or more.
3. t_{WU} and t_{WL} depend on OSCin input frequency.

   $t_{WU} \geq 8/fosc$ (e. g. $t_{WU} \geq 625ns$, foscin = 12.8 MHz)

   $t_{WL} \leq 16/fosc$ (e. g. $t_{WL} \leq 1250ns$, foscin = 12.8 MHz)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit	Remark
		Min	Typ	Max		
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	Vp	Vcc	–	5.0	V	
Input voltage	V_I	GND	–	V_{CC}	V	
Operating temperature	Ta	–40	–	+85	°C	

Notes: To protect against damage by electrostatic discharge, note the following handling precautions:

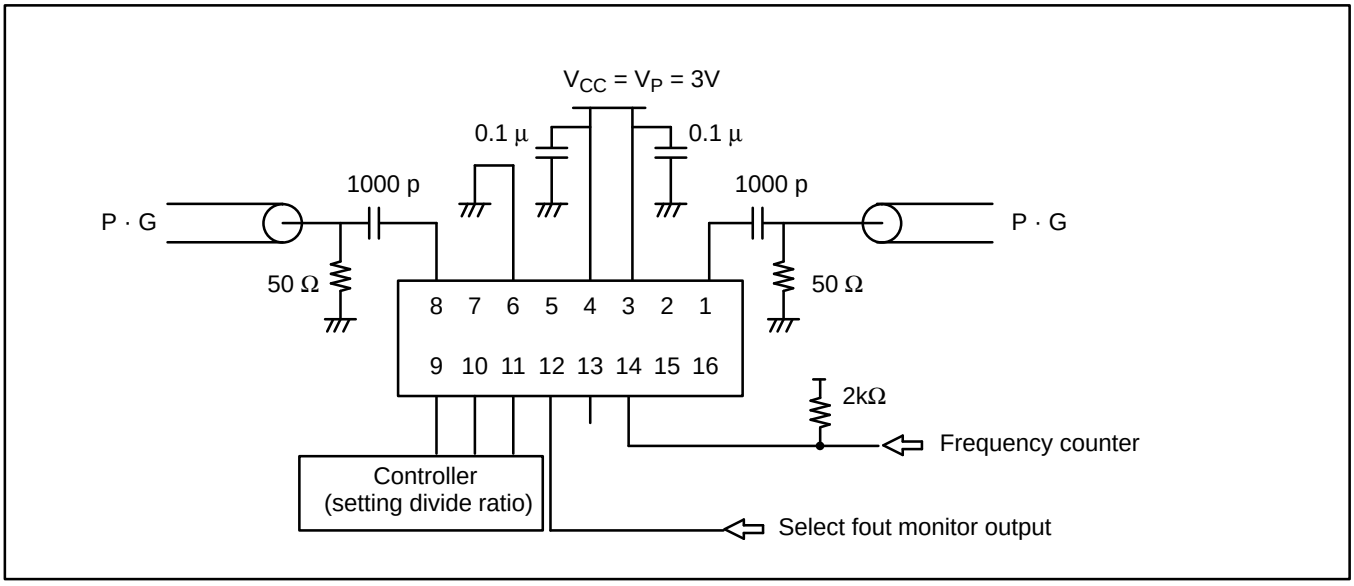
- Store and transport devices in conductive containers.
- Use properly grounded workstations, tools, and equipment.
- Turn off power before inserting or removing this device into or from a socket.
- Protect leads with conductive sheet, when transporting a board mounted device.

ELECTRICAL CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

Parameter		Symbol	Value			Unit	Condition
			Min	Typ	Max		
Supply current		I_{CC}	–	6.5	–	mA	With f_{IN} = 1.1 GHz, OSC_{IN} = 12 MHz, V_{CC} = 3.0 V. In locked state.
Operating frequency	f_{IN}	f_{IN}	300	–	1100	MHz	AC coupling. The minimum operating frequency is measured with a 1000pF capacitor connected.
	OSC_{IN}	f_{OSC}	–	12	23	MHz	
Input sensitivity	f_{IN}	$P_{f\,IN}$	–10	–	6	dBm	50Ω
	OSC_{IN}	V_{OSC}	0.5	–	–	Vp–p	
High-level input voltage	Except f_{IN} and OSC_{IN}	V_{IH}	V_{CC} x 0.7	–	–	V	
Low-level input voltage		V_{IL}	–	–	V_{CC} x 0.3	V	
High-level input current	Data, Clock	I_{IH}	–	–	1.0	µA	
Low-level input current		I_{IL}	–	–	–1.0	µA	
Input current	OSC_{IN}	I_{OSC}	–	±50	–	µA	
	FC, LE	I_{LE}	–	–60	–	µA	
High-level output voltage	Except D_O and OSC_{OUT}	V_{OH}	2.1	–	–	V	V_{CC} = 3 V, I_{OH} = –1.0mA
Low-level output voltage		V_{OL}	–	–	0.4	V	Vcc = 3V, I_{OL} = 1.0mA
High-impedance Cut off current	D_O, fout, ΦP	I_{OFF}	–	–	1.1	µA	V_{CC} = 3.6V V_P = 5 V
Output current	Except D_O and OSC_{OUT}	I_{OH}	–1.0	–	–	mA	Vcc = 3V
		I_{OL}	–	–	1.0	mA	Vcc = 3V

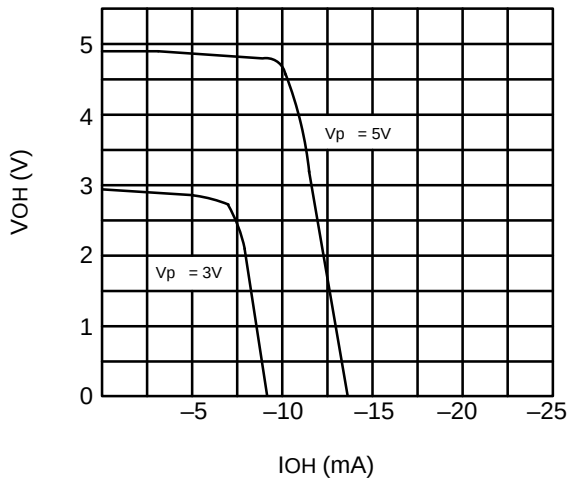
TEST CIRCUIT
(FOR MEASURING INPUT SENSITIVITY fin/OSCin)



TYPICAL CHARACTERISTIC CURVES

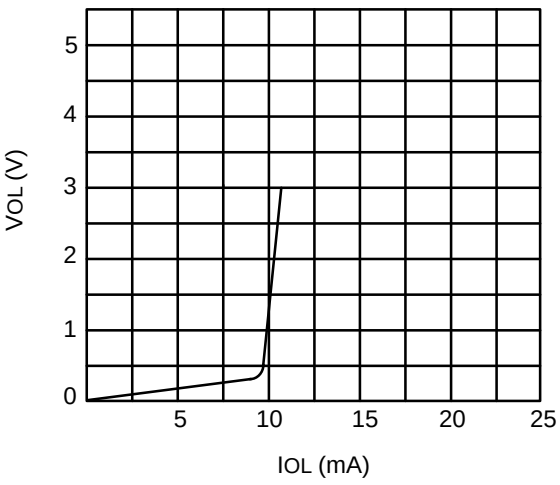
Charge pump current vs. Do voltage

Vcc =3.0V

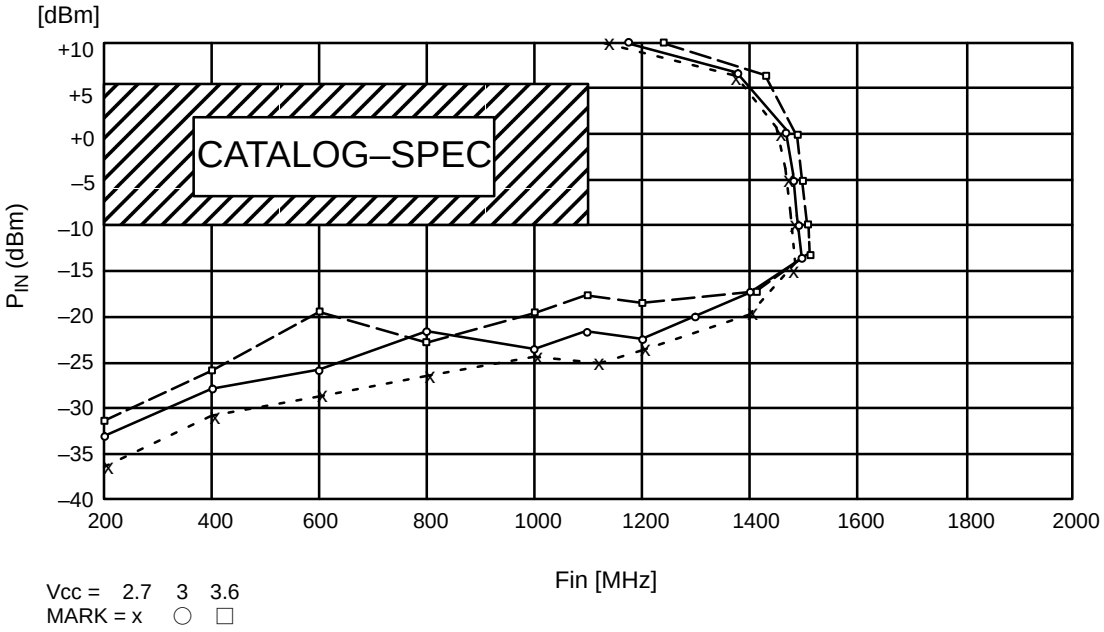


Charge pump current vs. Do voltage

Vcc =3.0V



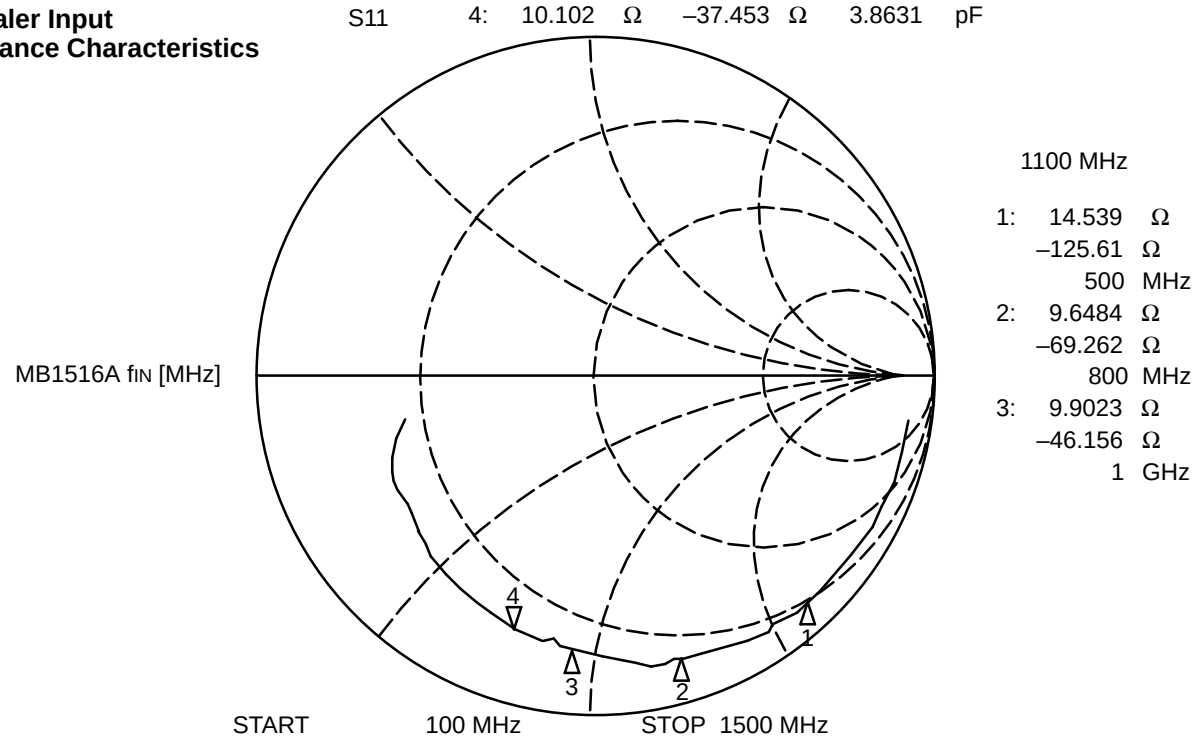
Fin Input sensitivity vs. Input frequency



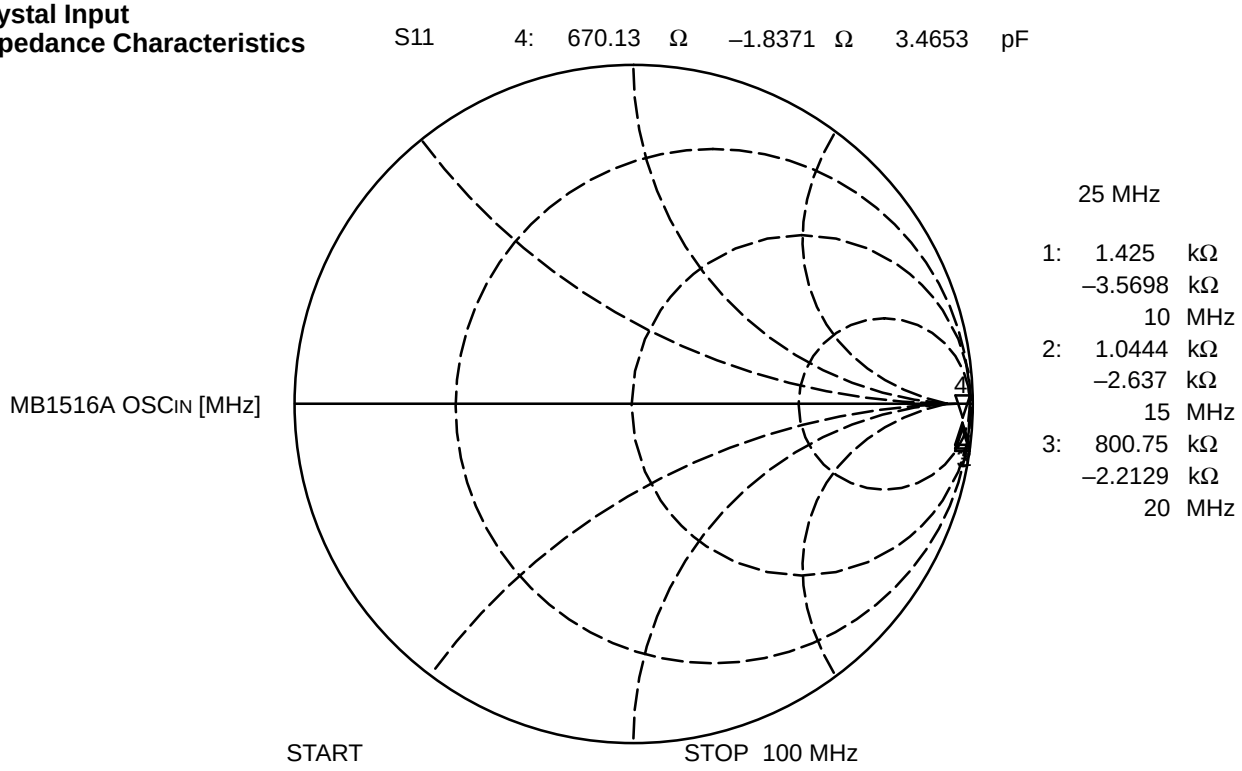
Vcc = 2.7 3 3.6
MARK = x ○ □

TYPICAL CHARACTERISTIC CURVES (Continued)

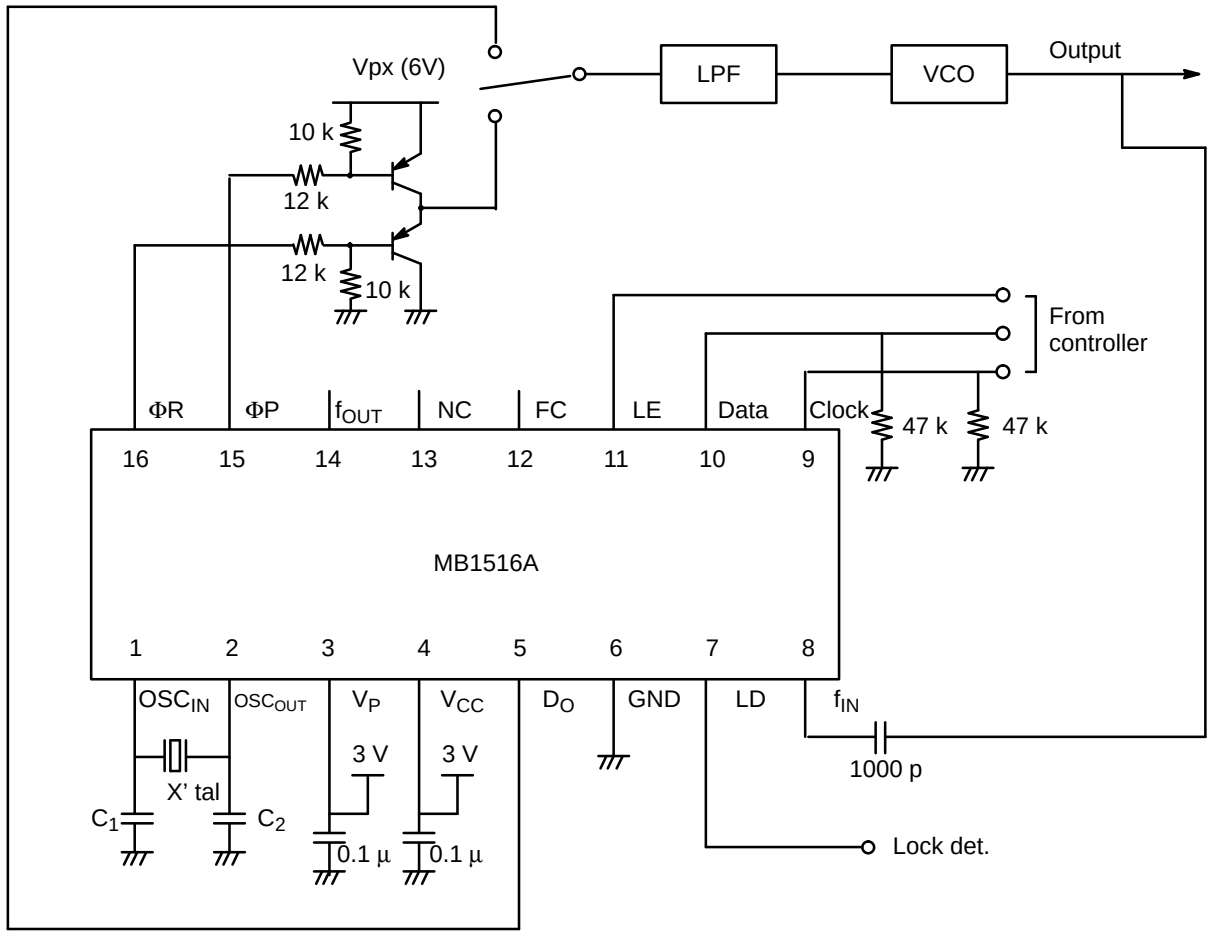
Prescaler Input Impedance Characteristics



Crystal Input Impedance Characteristics



APPLICATION EXAMPLE

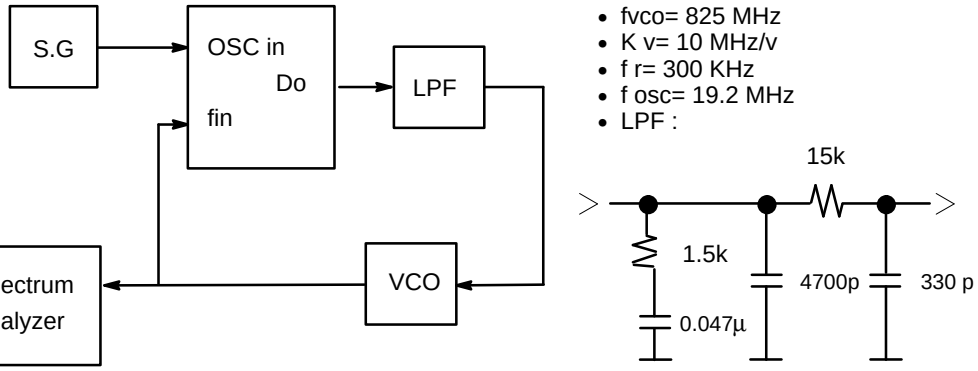


V_{PX} : Maximum 6 V
C_1, C_2 : Depend on the crystal parameters
LE, FC : With internal pull-up resistor
ΦP : N-ch open drain output
ΦR : C-MOS output

REFERENCE INFORMATION

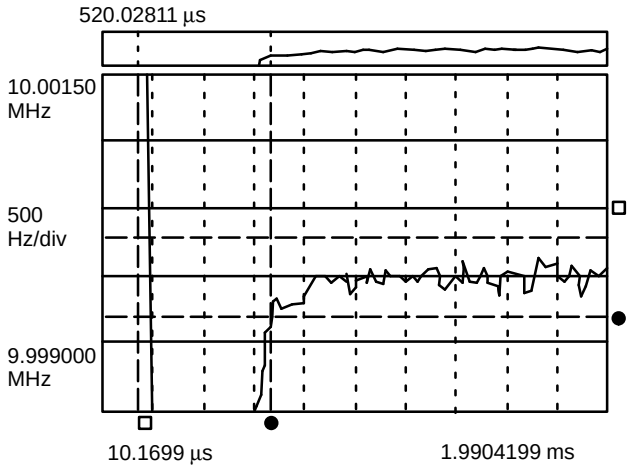
Typical plots measured with the test circuit shown on the right of this description are shown below. Each plot shows lock up time, phase noise with various span.

Test Circuit

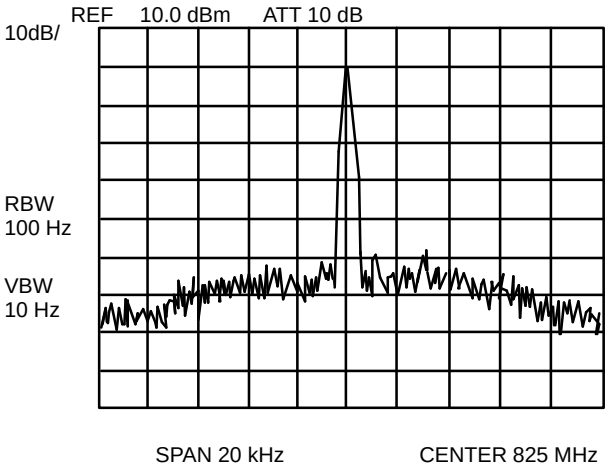


- fvco= 825 MHz
- K v= 10 MHz/v
- f r= 300 KHz
- f osc= 19.2 MHz
- LPF :

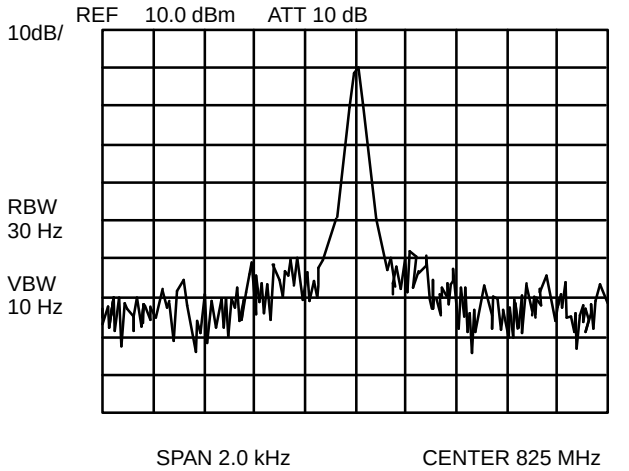
PLL Lock Up Time



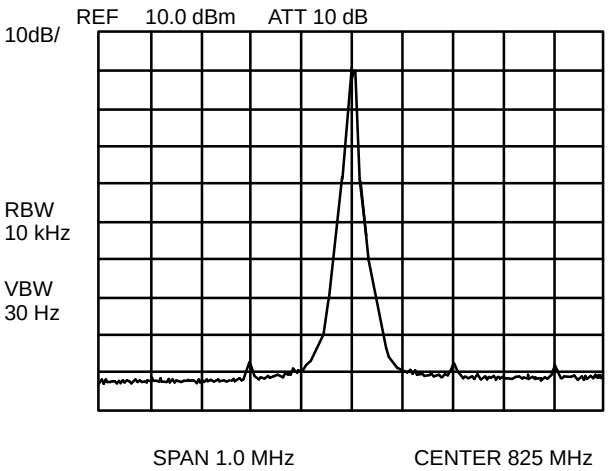
PLL Phase Noise



PLL Phase Noise

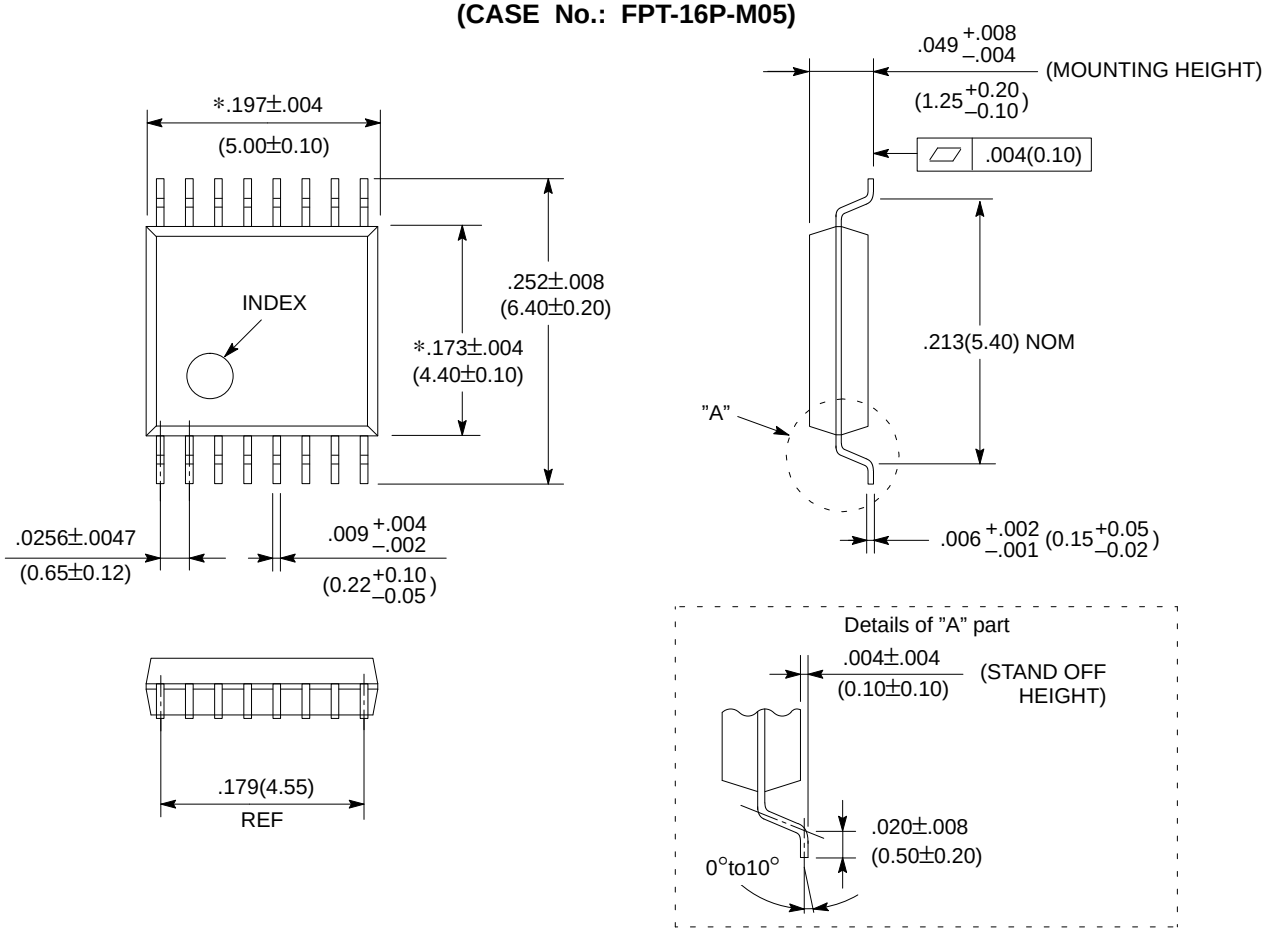


PLL Reference Leakage



PACKAGE AND DIMENSION

16-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-16P-M05)



*:This dimension does not include resin protruction.

Dimensions in inches (millimeters)

MEMO

MEMO

FUJITSU LIMITED

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