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FUJITSU

DATA SHEET

MB1515 ASSP

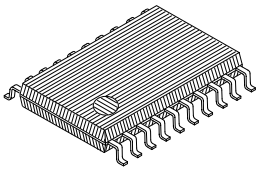
BiCMOS 2.5GHz PLL FREQUENCY SYNTHESIZER WITH BUILT-IN PRESCALER

DESCRIPTION

The MB1515 is a serial input PLL (Phase-Locked Loop) frequency synthesizer with a built-in prescaler allowing for a pulse swallow system in the two modulus 2.5 GHz band. It is suitable for BS and TV tuners and CATV systems.

The synthesizer is powered by 5 V (typical). Using the latest proprietary process, current consumption has been reduced to I_{CC} = 16 mA (typical).

20–pin Plastic SSOP



(FPT-20P-M03)

FEATURES

- Supply voltage: V_{CC} = 5 V
- High-speed operation capability: fin = 2.5 GHz (Pin = - 4 dBm)
- Low current consumption: I_{CC} = 16 mA (typical)
- Broad operating temperature range: Ta = - 40°C to +85°C
- Integrated Functions
  24-bit shift register
  24-bit latch
  Reference divider
  Binary 2-bit programmable reference counter (Divide ratios: 256, 512, 1024, and 2048)
  Comparison Divider
  Binary 5-bit swallow counter (Divide ratios: 0 to 31)
  Binary 12-bit bit programmable counter (Divide ratios: 32 to 4095)
  Phase comparator with phase conversion feature
  Two modulus prescaler for 2.5 GHz band (Divide ratios: 256/272 and 512/528)
  4-bit band switching signals
  Control signal generator
  Crystal oscillator
  Charge pump

MAXIMUM RATINGS

Parameter	Symbol	Value	Units
Supply voltage	V_{CC}	–0.5 to +7.0	V
Output voltage	V_O	–0.5 to V_{CC}+0.5	V
Output current	I_O	±10	mA
Storage temperature	Tstg	–55 to +125	°C

RECOMMENDED OPERATING CONDITIONS

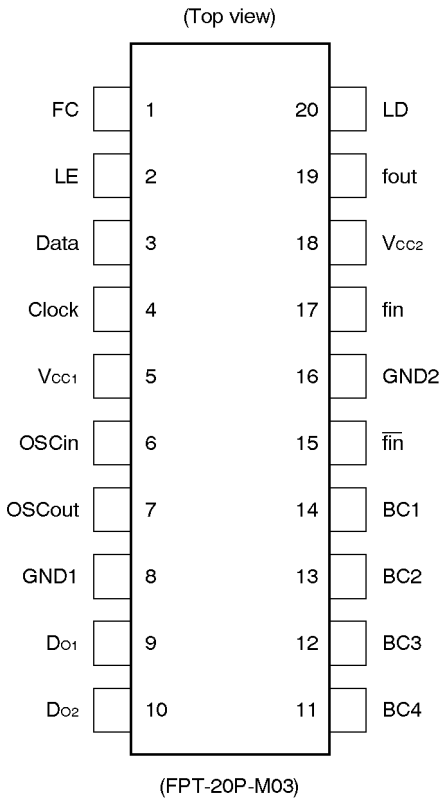
Parameter	Symbol	Value			Unit
		Min.	Typ.	Max	
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_I	GND	—	V_{CC}	V
Operating temperature	Ta	–40	—	+85	°C

NOTES:

1. To prevent damage caused by static electricity, an antistatic element is added and antistatic enhancement is also built into the circuit. However, the following handling cautions must be observed:
   - Contain the device in a conductive case when storing or transporting it.
   - Before handling, verify that the person handling the device, fixtures, and tools are not charged (grounded). Use a grounded conductive sheet as the work surface.
   - Turn off power before connecting or disconnecting the device to or from the socket.
   - Protect the lead with a conductive sheet when handling (such as transporting) a board on which this device is mounted.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

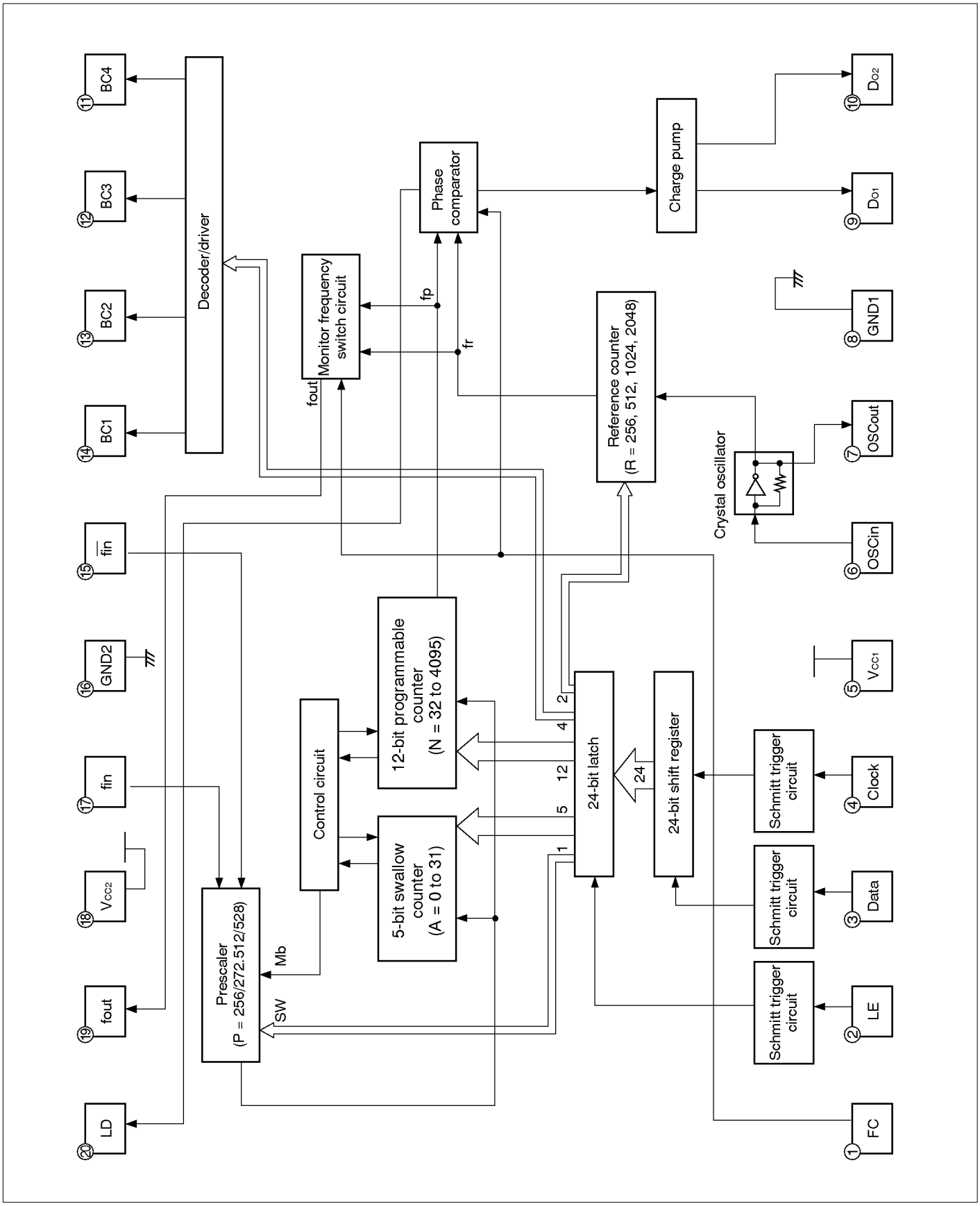
PIN ASSIGNMENT



PIN DESCRIPTION

Pin No.	Pin name	I/O	Descriprion
1	FC	I	Phase switch input pin to the phase comparator (with pull up resistor). This pin allows for inverting the polarity of phase comparator output, according to the polarity of the externally connected LPF and VCO. When FC is at “L” level, charge pump and phase comparator characteristics are reversed. This pin also toggles the output of the fout pin (test pin) between fr and fp.
2	LE	I	Load enable signal input pin (with Schmitt trigger circuit). The pin sends shift register contents to the latch when LE is at “H” (or open).
3	Data	I	Serial data input pin using binary codes (with Schmitt trigger circuit).
4	Clock	I	24-bit shift register clock input pin (with Schmitt trigger circuit). Data is read at the rising edge of the clock pulse.
5	V_{CC1}	—	Power supply pin (for PLL).
6	OSCin	I	Cystal oscillator connect pin and reference divider input pin. (OSCin: Oscillator input pin, OSCout: Oscillator output pin)
7	OSCout	O	
8	GND1	—	Grounding pin (for PLL)
9	DO1	O	Charge pump output pin. Phase characteristics invert with FC pin settings.
10	DO2	O	
11	BC4	O	Band switch output pin (open collector output). Output is controlled by the serial data band bit setting. When BCX bit is “H”, the BCX output transistor turns ON. When BCX bit is “H”, the BCX output transistor turns OFF. (X: 1 to 4)
12	BC3	O	
13	BC2	O	
14	BC1	O	
15	fin	I	fin’s complementary input pin. Connect to ground via a capacitor.
16	GND2	—	Ground pin (for prescaler).
17	$\overline{fin}$	I	Prescaler input pin. Input using ac coupling.
18	V_{CC2}	—	Power supply pin (for prescaler).
19	fout	O	Phase comparator input monitor pin.Produces either the reference divider output (fr)or the comparison divider output (fp) signal depending on the FC pin’s input level. FC: “H” → Output Signal: fr FC: “L” → Output Signal: fp
20	LD	O	Phase comparator output pin. LD is usually “H”, and is set to “L” for the duration equivalent to the phase error between fr and fp.

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Parameter		Symbol	Condition	Value			Units
				Min.	Typ.	Max.	
Power supply current		I_{CC}	When input at fin=2.5GHz and OSCin= 4MHz, V_{CC}=5V. Other input pins are GND and output pins are open.	—	16.0	—	mA
Operating frequency	fin	fin	Must be AC-coupled. The minimum operating frequency when coupled at 1000 pF.	100	—	2500	MHz
	OSCin	f_{OSC}	—	—	4	10	MHz
Permissible input voltage	fin	Pfin1	2300 to 2500 MHz	–4	—	6	dBm
		Pfin2	1900 to 2300 MHz	–7	—	6	dBm
		Pfin3	1000 to 1900 MHz	–10	—	6	dBm
		Pfin4	100 to 1000 MHz	–20	—	6	dBm
	OSCin	V_{OSC}	—	0.5	—	—	V_{P-P}
High level input voltage	Other the fin and OSCin	V_{IH}		$V_{CC} \times 0.7 + 0.4$			V
Low level input voltage		V_{IL}	—	—	—	$V_{CC} \times 0.3 - 0.4$	V
High level input current	Data, Clock, LE	I_{IH}	—	—	1.0	—	μA
		I_{IL}	—	—	–1.0	—	μA
Low level input current	FC	I_{ILFC}	—	—	–60	—	μA
Input current	OSCin	I_{IOSC}	—	—	±50	—	μA
High level output voltage	Excluding Do and BC	V_{OH}	When V_{CC} = 5 V	4.4	—	—	V
Low level output voltage		V_{OL}	—	—	—	0.4	V
High impedance cutoff current	Do 1, 2 BC 1 to 4	I_{OFF}	—	—	—	1.1	μA
Output current	Excluding Do and BC	I_{OH}	—	–1.0	—	—	mA
		I_{OL}	—	1.0	—	—	mA
Output voltage breakdown	BC1 to 4	V_B	—	—	—	12	V

FUNCTIONAL DESCRIPTIONS

1. Formula for calculation of divide ratio

Set divider's divide ratio according to the following formula:

$$f_{VCO} = [(P \times N) + (16 \times A)] \times f_{OSC} \div R$$

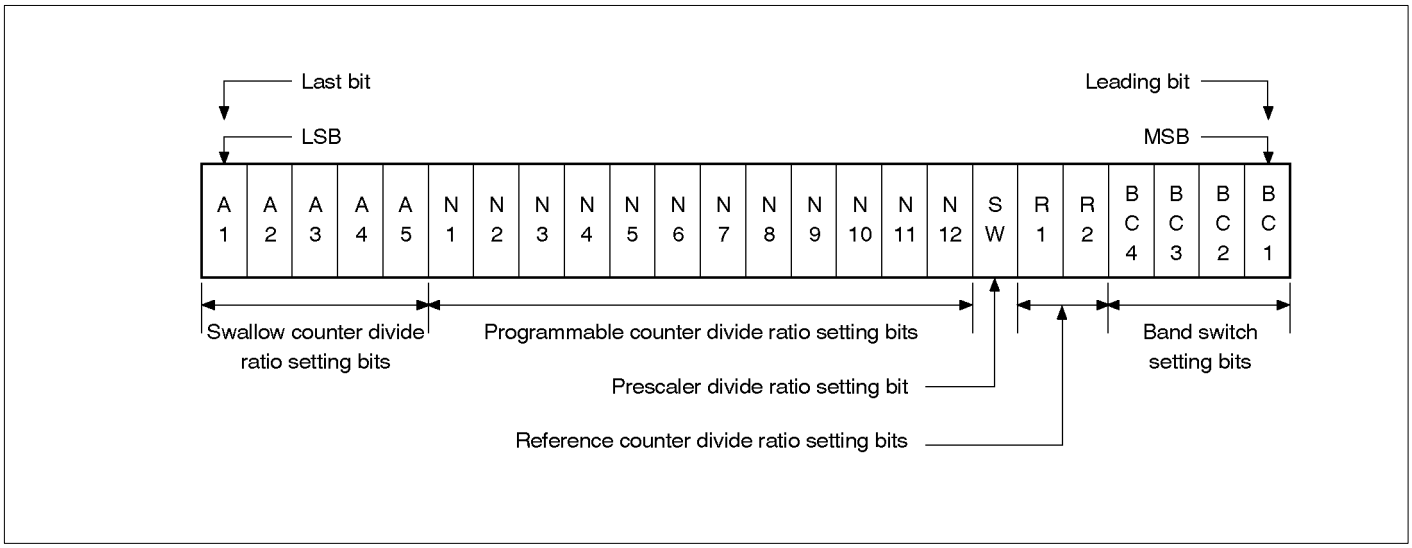
where

f_{VCO}	:	Externally connected VCO output frequency
P	:	Prescaler divide ratio (256 or 512)
N	:	Binary 12-bit programmable counter setting (32 to 4095)
A	:	Binary 5-bit swallow counter setting (0 to 31)
f_{OSC}	:	Reference oscillation frequency
R	:	Reference counter setting (256, 512, 1024, 2048)

2. Serial data input procedure

Serial data is input from three inputs, Data pin, Clock pin and LE pin, allowing for control of the 4-bit band switch setting, the 3-bit reference divider and the 17-bit comparison divider respectively. The data is sequentially fetched into the internal shift register at the rising edge of the clock and transferred to the latch when load enable is at the "H" level.

The 24-bit shift register is configured as follows:



- **Band switch setting (BC1 to BC4)**
  When data set in the band bits is at "H," output is turned ON. When data is at "L," output is turned OFF.
- **Prescaler divide ratio (SW)**
  Divided by 256/272 when data set in the SW bit is at "H." Divided by 512/528 when data is at "L."

- **Divide ratios for 5-bit swallow counter (A1 to A5)**

Divide ratio A	A5	A4	A3	A2	A1
0	0	0	0	0	0
1	0	0	0	0	1
2	0	0	0	1	0
• •	• •	• •	• •	• •	• •
31	1	1	1	1	1

- **Reference counter divide ratios (R1 and R2)**

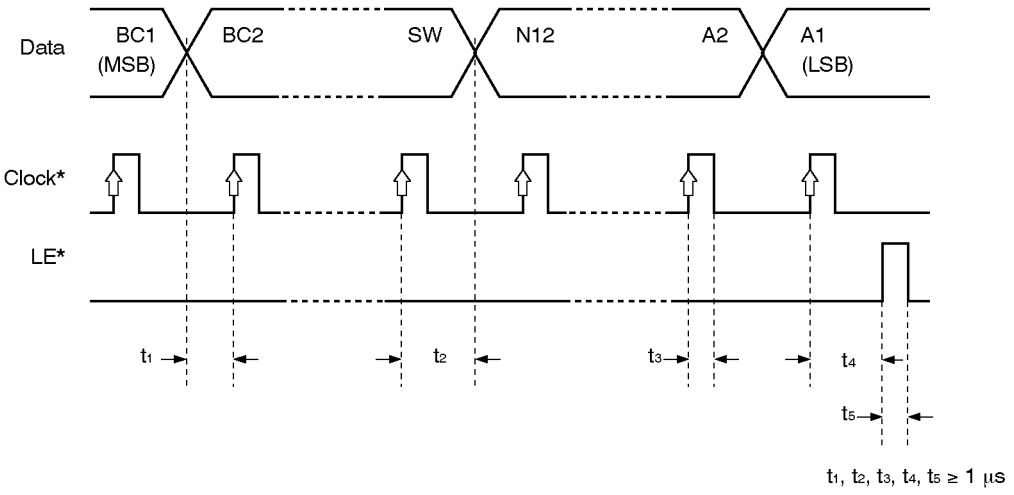
Divide ratio R	R2	R1
256	0	0
512	0	1
1024	1	0
2048	1	1

- **Divide ratios for 12-bit programmable counter (N1 to N12)**

Divide ratios	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1
0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0	0	1
2	0	0	0	0	0	0	1	0	0	0	1	0
• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •	• •
4095	1	1	1	1	1	1	1	1	1	1	1	1

3. Serial data input timings

When designing the synthesizer, control the FC pin according to the VCO polarity.



*: Fetches data at the rising edge of the clock.
*: Fetches data when LE is at “H” level.

4. FC pin input in relation to phase characteristics

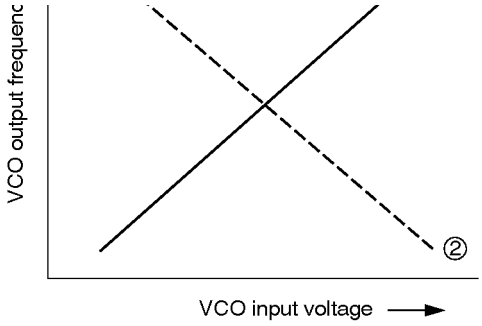
The FC pin switches the phase of the phase comparator. Phase characteristics (charge pump output) are inverted by controlling this pin. Output from the phase comparator input monitor pin (fout) is also controlled by this FC pin. The relation of FC pin input with Do and fout is as follows:

	FC: “H” (or open)		**FC: “L”**	
	DO1, DO2	**fout**	**DO1, DO2**	**fout**
fr>fp	H	Outputs reference divider output (fr)	L	Outputs comparison divider output (fp)
fr=fp	Z		Z	
fr<fp	L		L	

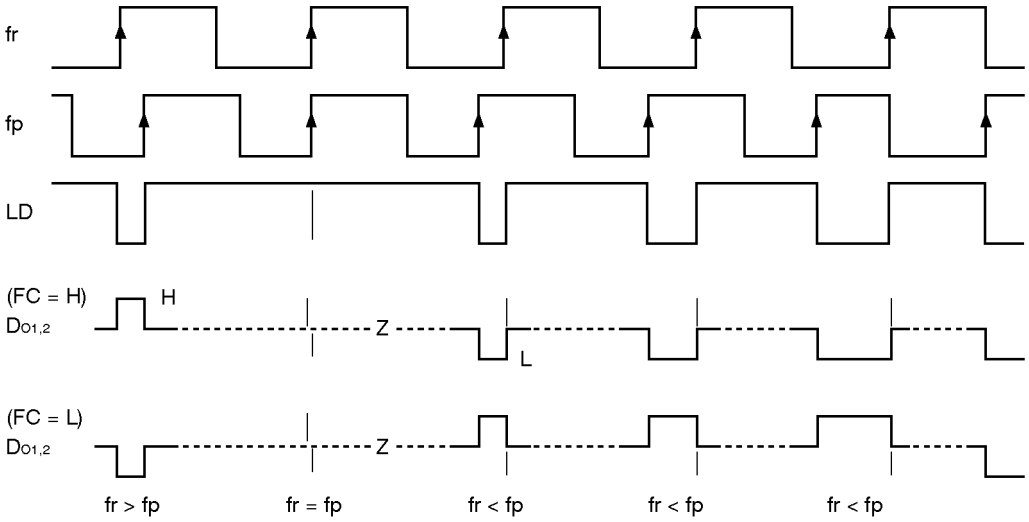
Z: high impedance

When designing the synthesizer, control the FC pin according to the VCO polarity.

- When the VCO polarity is ① in the figure, the FC pin is either at “H” or open.
- When the VCO polarity is ② in the figure, the FC pin is at “L”.



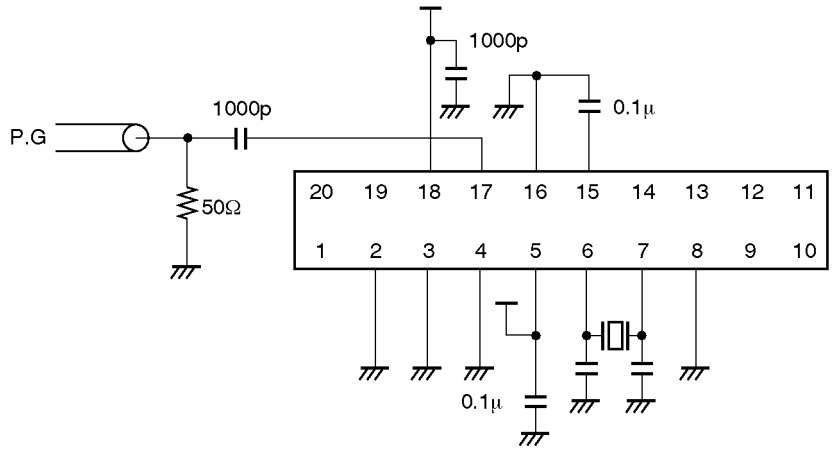
PHASE COMPARATOR OUTPUT WAVEFORMS



Notes:

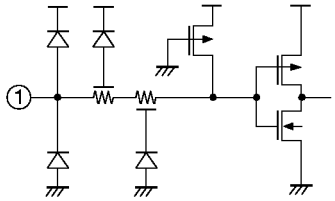
1. The phase error is detected in a range of - 2 π to +2 π.
2. Output of a “glitch” varies slightly with charge pump characteristics. This “glitch” is output to eliminate an dead band.

EXAMPLE MEASUREMENT CIRCUIT (PRESCALER INPUT SENSITIVITY)

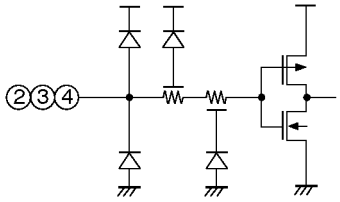


EQUIVALENT CIRCUIT DIAGRAM

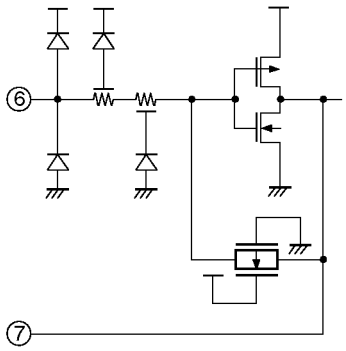
• FC



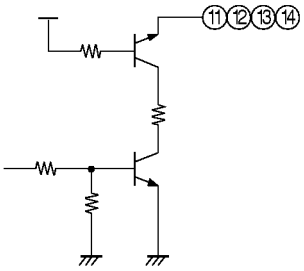
• LE, Data, clock



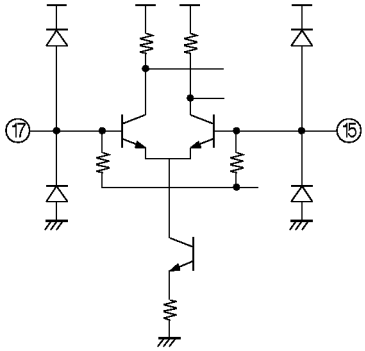
• OSCin, OSCout



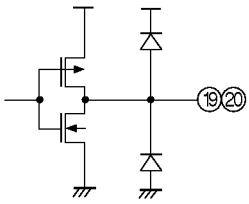
• BC1, BC2, BC3, BC4



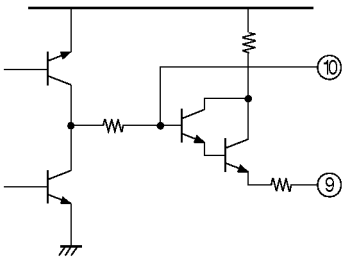
• $\overline{\text{fin}}$, fin



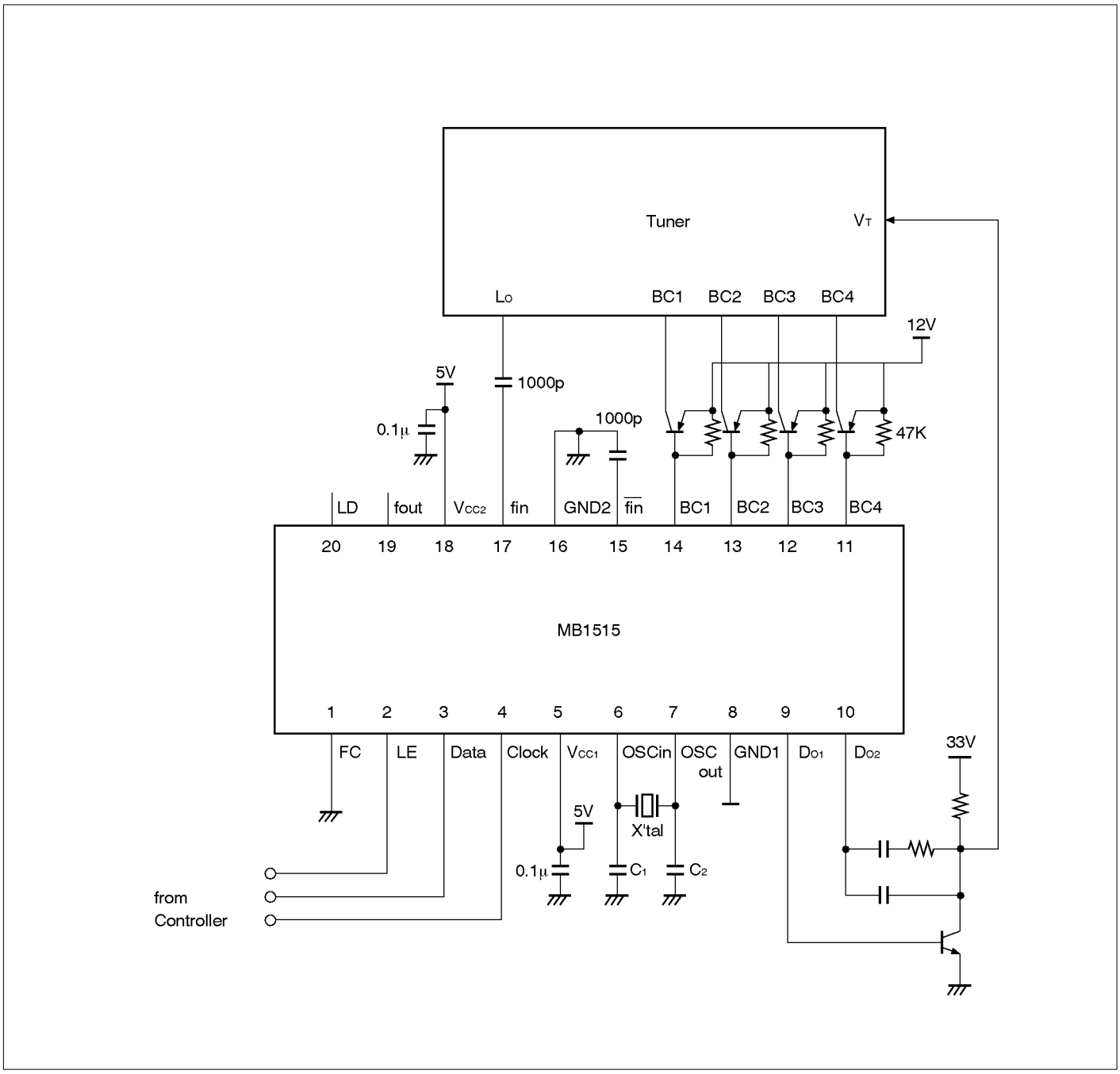
• LE, Data, clock



• LE, Data, clock



EXAMPLE APPLICATION



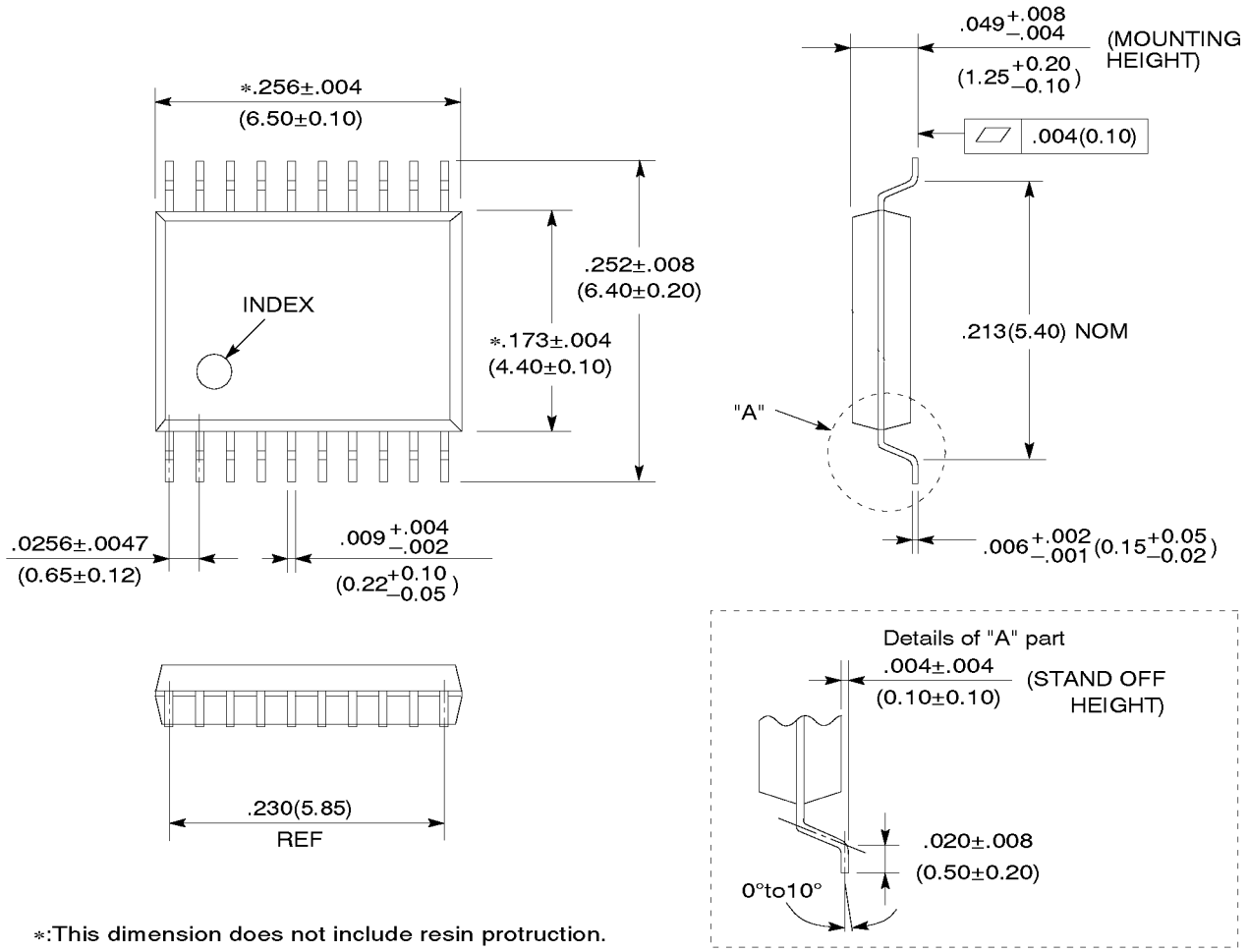
C1, C2: Determined by the crystal oscillator
FC: with pull up resistor

ORDERING INFORMATION

Parts Number	Package	Notes
MB1515PFV	Plastic SSOP, 20 pins (FPT–20P–M03)	

EXTERNAL DIMENSIONS

20-pin plastic SSOP
(FPT-20P-M03)



∗:This dimension does not include resin protruction.

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Dimensions in inches (millimeters)

NOTES

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