# **Technical Data**

# Integrated Silicon Pressure Sensor On-Chip Signal Conditioned, Temperature Compensated and Calibrated

The MPXV5004G series piezoresistive transducer is a state-of-the-art monolithic silicon pressure sensor designed for a wide range of applications, but particularly those employing a microcontroller or microprocessor with A/D inputs. This sensor combines a highly sensitive implanted strain gauge with advanced micromachining techniques, thin-film metallization, and bipolar processing to provide an accurate, high level analog output signal that is proportional to the applied pressure.

#### **Features**

- Temperature Compensated over 10° to 60°C
- Available in Gauge Surface Mount (SMT) or Throughhole (DIP) Configurations
- · Durable Thermoplastic (PPS) Package

## **Application Examples**

- · Washing Machine Water Level
- Ideally Suited for Microprocessor or Microcontroller-Based Systems

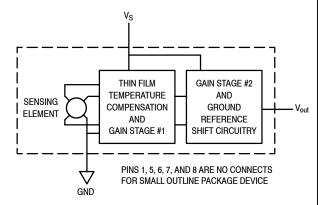


Figure 1. Fully Integrated Pressure Sensor Schematic

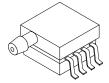
# SMALL OUTLINE PACKAGE SURFACE MOUNT



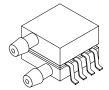
MPXV5004G6U CASE 482



MPXV5004GC6U CASE 482A



MPXV5004GP CASE 1369



MPXV5004DP CASE 1351



MPXV5004GVP CASE 1368

# MPXV5004G SERIES

INTEGRATED
PRESSURE SENSOR
0 to 3.92 kPa
(0 to 400 mm H<sub>2</sub>O)
1.0 to 4.9 V OUTPUT

#### SMALL OUTLINE PACKAGE THROUGH-HOLE



MPXV5004GC7U CASE 482C



MPXV5004G7U CASE 482B

PIN NUMBER				
1	N/C	5	N/C	
2	V <sub>S</sub>	6	N/C	
3	Gnd	7	N/C	
4	V <sub>out</sub>	8	N/C	

NOTE: Pins 1, 5, 6, 7, and 8 are internal device connections. Do not connect to external circuitry or ground. Pin 1 is noted by the notch in the lead.



## MAXIMUM RATINGS(NOTE)

Parametrics	Symbol	Value	Unit
Maximum Pressure (P1 > P2)	P <sub>max</sub>	16	kPa
Storage Temperature	T <sub>stg</sub>	-30 to +100	°C
Operating Temperature	T <sub>A</sub>	0 to +85	°C

NOTE: Exposure beyond the specified limits may cause permanent damage or degradation to the device.

# **OPERATING CHARACTERISTICS** ( $V_S = 5.0 \text{ Vdc}$ , $T_A = 25^{\circ}\text{C}$ unless otherwise noted, P1 > P2. Decoupling circuit shown in Figure 3 required to meet electrical specifications)

Characteristic		Symbol	Min	Тур	Max	Unit	
Pressure Range		P <sub>OP</sub>	0	_	3.92 400	kPa mm H <sub>2</sub> O	
Supply Voltage <sup>(1)</sup>		Vs	4.75	5.0	5.25	Vdc	
Supply Current		I <sub>S</sub>	_	_	10	mAdc	
Span at 306 mm H <sub>2</sub> O (3 kPa) <sup>(2)</sup>		V <sub>FSS</sub>	_	3.0	_	V	
Offset <sup>(3)(5)</sup>			V <sub>off</sub>	0.75	1.00	1.25	V
Sensitivity		V/P	_	1.0 9.8	_	V/kPa mV/mm H <sub>2</sub> O	
Accuracy <sup>(4)(5)</sup>	0 to 100 mm H <sub>2</sub> O 100 to 400 mm H <sub>2</sub> O	(10 to 60°C) (10 to 60°C)	_	_	_	±1.5 ±2.5	%V <sub>FSS</sub> %V <sub>FSS</sub>

#### NOTES:

- 1. Device is ratiometric within this specified excitation range.
- 2. Span is defined as the algebraic difference between the output voltage at specified pressure and the output voltage at the minimum rated pressure.
- 3. Offset (Voff) is defined as the output voltage at the minimum rated pressure.
- 4. Accuracy (error budget) consists of the following:
  - Linearity: Output deviation from a straight line relationship with pressure over the specified pressure range.
  - Temperature Hysteresis: Output deviation at any temperature within the operating temperature range, after the temperature is

cycled to and from the minimum or maximum operating temperature points, with zero differential pressure

applied.

Pressure Hysteresis: Output deviation at any pressure within the specified range, when this pressure is cycled to and from the

minimum or maximum rated pressure, at 25°C.

• Offset Stability: Output deviation, after 1000 temperature cycles, -30 to 100°C, and 1.5 million pressure cycles, with

minimum rated pressure applied.

TcSpan: Output deviation over the temperature range of 10 to 60°C, relative to 25°C.

TcOffset: Output deviation with minimum rated pressure applied, over the temperature range of 10 to 60°C,

relative to 25°C.

- Variation from Nominal: The variation from nominal values, for Offset or Full Scale Span, as a percent of V<sub>FSS</sub>, at 25°C.
- 5. Auto Zero at Factory Installation: Due to the sensitivity of the MPXV5004G, external mechanical stresses and mounting position can affect the zero pressure output reading. Autozeroing is defined as storing the zero pressure output reading and subtracting this from the device's output during normal operations. Reference AN1636 for specific information. The specified accuracy assumes a maximum temperature change of ± 5° C between autozero and measurement.

### ON-CHIP TEMPERATURE COMPENSATION, CALIBRATION AND SIGNAL CONDITIONING

The performance over temperature is achieved by integrating the shear-stress strain gauge, temperature compensation, calibration and signal conditioning circuitry onto a single monolithic chip.

Figure 2 illustrates the gauge configuration in the basic chip carrier (Case 482). A fluorosilicone gel isolates the die surface and wire bonds from the environment, while allowing the pressure signal to be transmitted to the silicon diaphragm.

The MPXV5004G series sensor operating characteristics are based on use of dry air as pressure media. Media, other than dry air, may have adverse effects on sensor performance and long-term reliability. Internal reliability and qualification

test for dry air, and other media, are available from the factory. Contact the factory for information regarding media tolerance in your application.

Figure 3 shows the recommended decoupling circuit for interfacing the output of the MPXV5004G to the A/D input of the microprocessor or microcontroller. Proper decoupling of the power supply is recommended.

Figure 4 shows the sensor output signal relative to pressure input. Typical, minimum and maximum output curves are shown for operation over a temperature range of 10°C to 60°C using the decoupling circuit shown in Figure 3. The output will saturate outside of the specified pressure range.

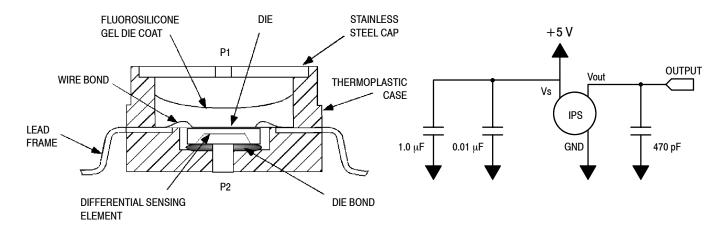


Figure 2. Cross-Sectional Diagram (Not to Scale)

Figure 3. Recommended power supply decoupling and output filtering.

For additional output filtering, please refer to Application Note AN1646.

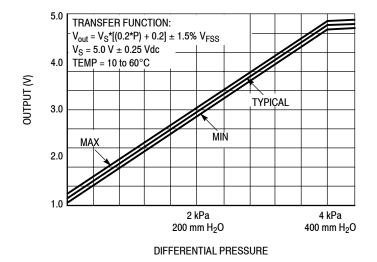


Figure 4. Output versus Pressure Differential

(See Note 5 in Operating Characteristics)

**MPXV5004G SERIES** 

## PRESSURE (P1)/VACUUM (P2) SIDE IDENTIFICATION TABLE

Freescale Semiconductor designates the two sides of the pressure sensor as the Pressure (P1) side and the Vacuum (P2) side. The Pressure (P1) side is the side containing silicone gel which isolates the die from the environment. The

Freescale Semiconductor pressure sensor is designed to operate with positive differential pressure applied, P1 > P2.

The Pressure (P1) side may be identified by using the table below:

Part Number	Case Type	Pressure (P1) Side Identifier	
MPXV5004GC6U/T1	482A	Side with Port Attached	
MPXV5004G6U/T1	482	Stainless Steel Cap	
MPXV5004GC7U	482C	Side with Port Attached	
MPXV5004G7U	482B	Stainless Steel Cap	
MPXV5004GP	1369	Side with Port Attached	
MPXV5004DP	1351	Side with Port Marking	
MPXV5004GVP	1368	Stainless Steel Cap	

### **ORDERING INFORMATION**

MPXV5004G series pressure sensors are available in the basic element package or with a pressure port. Two packing options are offered for the surface mount configuration.

Device Type / Order No.	Case No.	Packing Options	Device Marking
MPXV5004G6U	482	Rails	MPXV5004G
MPXV5004G6T1	482	Tape and Reel	MPXV5004G
MPXV5004GC6U	482A	Rails	MPXV5004G
MPXV5004GC6T1	482A	Tape and Reel	MPXV5004G
MPXV5004GC7U	482C	Rails	MPXV5004G
MPXV5004G7U	482B	Rails	MPXV5004G
MPXV5004GP	1369	Trays	MPXV5004G
MPXV5004DP	1351	Trays	MPXV5004G
MPXV5004GVP	1368	Trays	MPXV5004G

## INFORMATION FOR USING THE SMALL OUTLINE PACKAGE (CASE 482)

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the surface mount packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct fottprint, the packages will self align when subjected to a solder reflow process. It is always recommended to design boards with a solder mask layer to avoid bridging and shorting between solder pads.

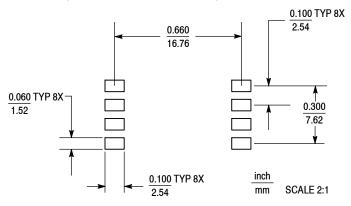


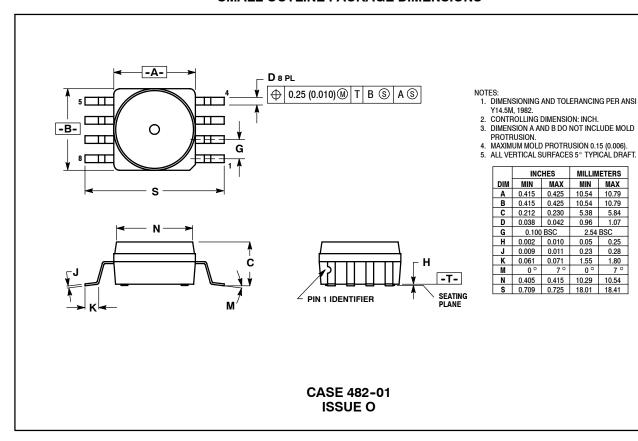
Figure 5. SOP Footprint (Case 482)

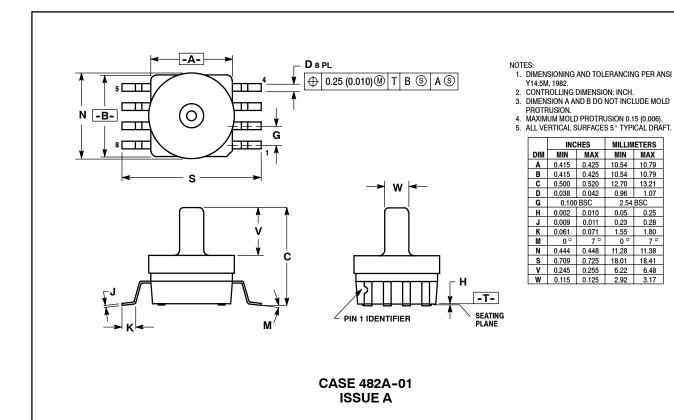
### **MPXV5004G SERIES**

# **NOTES**

# **NOTES**

### **SMALL OUTLINE PACKAGE DIMENSIONS**





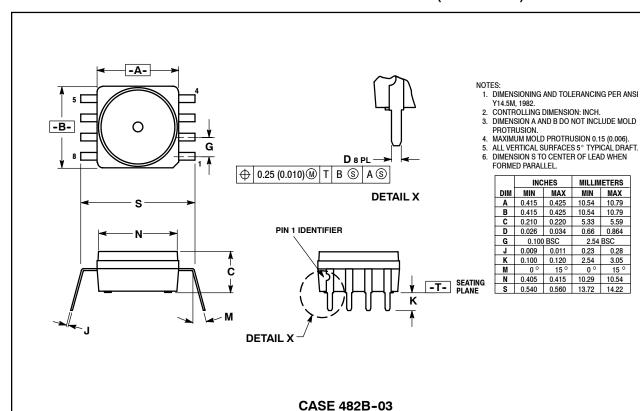
### **MPXV5004G SERIES**

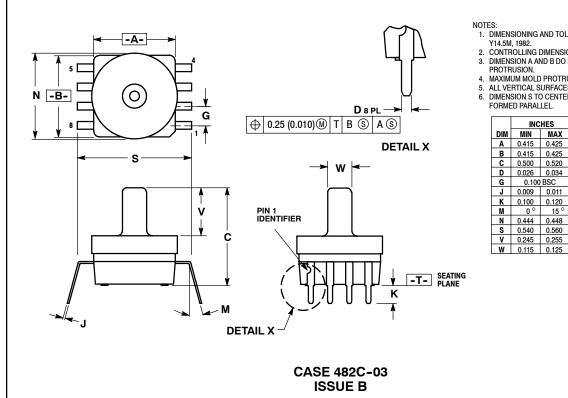
0.28

1.80 7°

11.38

**ISSUE B** 





DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

15 °

- 114-3M, 1962.

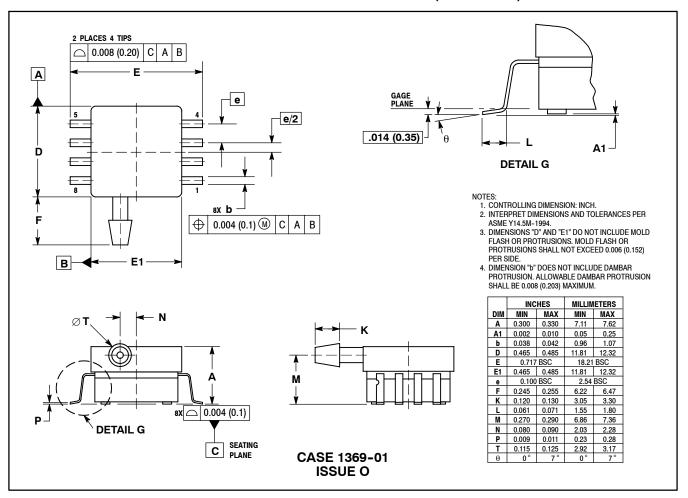
  CONTROLLING DIMENSION: INCH.

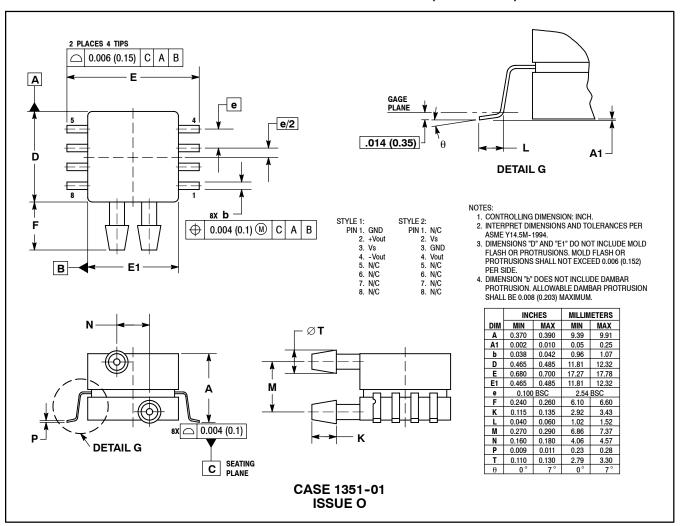
  DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.

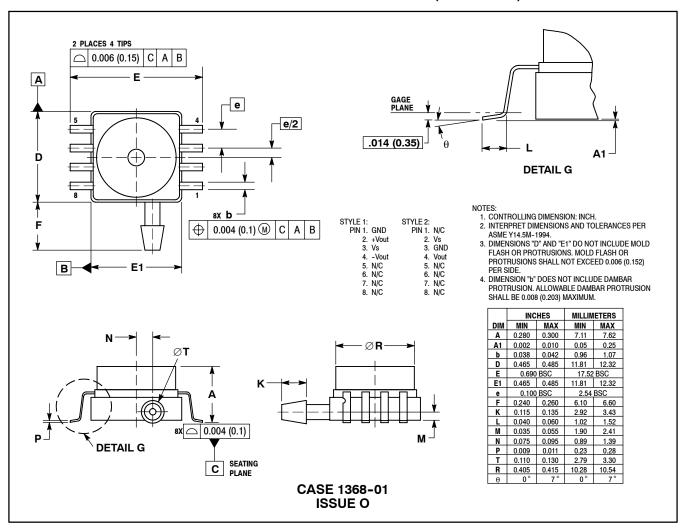
  MAXIMUM MOLD PROTRUSION 0.15 (0.006).
- ALL VERTICAL SURFACES 5° TYPICAL DRAFT.
  DIMENSION S TO CENTER OF LEAD WHEN
  FORMED PARALLEL.
  - MILLIMETERS INCHES DIM MIN MAX MIN MAX A 0.415 0.425 10.54 10.79 **B** 0.415 0.425 10.54 10.79 **C** 0.500 0.520 **D** 0.026 0.034 12.70 13.21 0.66 0.864 0.100 BSC 2.54 BSC J 0.009 0.011 K 0.100 0.120 2.54 3.05 0 ° 15 ° 15 ° 0 ° 0.444 0.448 
     S
     0.540
     0.560
     13.72
     14.22

     V
     0.245
     0.255
     6.22
     6.48

### **MPXV5004G SERIES**







#### How to Reach Us:

#### Home Page:

www.freescale.com

#### E-mail:

support@freescale.com

#### **USA/Europe or Locations Not Listed:**

Freescale Semiconductor Technical Information Center, CH370 1300 N. Alma School Road Chandler, Arizona 85224 +1-800-521-6274 or +1-480-768-2130 support@freescale.com

### Europe, Middle East, and Africa:

Freescale Halbleiter Deutschland GmbH Technical Information Center Schatzbogen 7 81829 Muenchen, Germany +44 1296 380 456 (English) +46 8 52200080 (English) +49 89 92103 559 (German) +33 1 69 35 48 48 (French) support@freescale.com

#### Japan:

Freescale Semiconductor Japan Ltd. Technical Information Center 3-20-1, Minami-Azabu, Minato-ku Tokyo 106-0047, Japan 0120 191014 or +81 3 3440 3569 support.japan@freescale.com

#### Asia/Pacific:

Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

#### For Literature Requests Only:

Freescale Semiconductor Literature Distribution Center P.O. Box 5405 Denver, Colorado 80217

1-800-441-2447 or 303-675-2140

Fax: 303-675-2150

LDCF or Free scale Semiconductor @hibbert group.com

Information in this document is provided solely to enable system and software implementers to use Freescale Semiconductor products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits or integrated circuits based on the information in this document.

Freescale Semiconductor reserves the right to make changes without further notice to any products herein. Freescale Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Freescale Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in Freescale Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals", must be validated for each customer application by customer's technical experts. Freescale Semiconductor does not convey any license under its patent rights nor the rights of others. Freescale Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Freescale Semiconductor product could create a situation where personal injury or death may occur. Should Buyer purchase or use Freescale Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold Freescale Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Freescale Semiconductor was negligent regarding the design or manufacture of the part.

Freescale ™ and the Freescale logo are trademarks of Freescale Semiconductor, Inc. All other product or service names are the property of their respective owners. © Freescale Semiconductor, Inc. 2004. All rights reserved.

