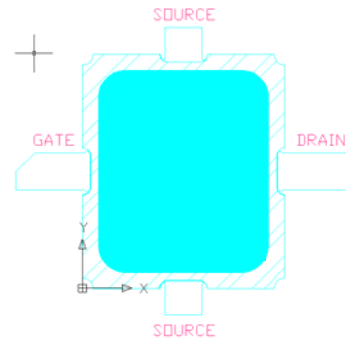


- PERFORMANCE (1.8 GHz)
 - ◆ 31 dBm Output Power (P_{1dB})
 - ◆ 15 dB Power Gain (G_{1dB})
 - ◆ 43 dBm Output IP3
 - ◆ -42 dBc WCDMA ACPR at 21 dBm P_{CH}
 - ◆ 10V Operation
 - ◆ 50% Power-Added Efficiency
 - ◆ Evaluation Boards Available
 - ◆ Design Data Available on Website
 - ◆ Suitable for applications to 5 GHz



SEE PACKAGE OUTLINE FOR MARKING CODE

- DESCRIPTION AND APPLICATIONS

The *FPD1000AS* is a packaged *depletion mode* AlGaAs/InGaAs pseudomorphic High Electron Mobility Transistor (pHEMT), optimized for power applications in L-Band. The surface-mount package has been optimized for low parasitics.

Typical applications include drivers or output stages in PCS/Cellular *base station* transmitter amplifiers, as well as other power applications in WLL/WLAN amplifiers.

- ELECTRICAL SPECIFICATIONS AT 22°C

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
RF SPECIFICATIONS MEASURED AT $f = 1.8$ GHz USING CW SIGNAL						
Power at 1dB Gain Compression	P_{1dB}	$V_{DS} = 10V$; $I_{DS} = 200$ mA Γ_S and Γ_L tuned for Optimum IP3	30	31		dBm
Power Gain at dB Gain Compression	G_{1dB}	$V_{DS} = 10V$; $I_{DS} = 200$ mA Γ_S and Γ_L tuned for Optimum IP3	13.5	15.0		
Maximum Stable Gain S_{21}/S_{12}	MSG	$V_{DS} = 10$ V; $I_{DS} = 200$ mA $P_{IN} = 0$ dBm, 50 Ω system		20		dB
Power-Added Efficiency at 1dB Gain Compression	PAE	$V_{DS} = 10V$; $I_{DS} = 200$ mA Γ_S and Γ_L tuned for Optimum IP3		50		%
3 rd -Order Intermodulation Distortion Γ_S and Γ_L tuned for Optimum IP3	IM3	$V_{DS} = 10V$; $I_{DS} = 200$ mA $P_{OUT} = 19$ dBm (single-tone level)		-46		dBc
Saturated Drain-Source Current	I_{DSS}	$V_{DS} = 1.3$ V; $V_{GS} = 0$ V	480	650	800	mA
Maximum Drain-Source Current	I_{MAX}	$V_{DS} = 1.3$ V; $V_{GS} \cong +1$ V		1100		mA
Transconductance	G_M	$V_{DS} = 1.3$ V; $V_{GS} = 0$ V		720		mS
Gate-Source Leakage Current	I_{GSO}	$V_{GS} = -3$ V		20	50	μ A
Pinch-Off Voltage	$ V_P $	$V_{DS} = 1.3$ V; $I_{DS} = 2.4$ mA	0.7	0.9	1.4	V
Gate-Source Breakdown Voltage	$ V_{BDGS} $	$I_{GS} = 2.4$ mA	6	8		V
Gate-Drain Breakdown Voltage	$ V_{BDGD} $	$I_{GD} = 2.4$ mA	20	22		V
Thermal Resistivity (channel-to-case)	Θ_{CC}	See Note on following page		25		°C/W

- RECOMMENDED OPERATING BIAS CONDITIONS

Drain-Source Voltage: From 5V to 10V
 Quiescent Current: From 25% I_{DSS} to 55% I_{DSS}

- ABSOLUTE MAXIMUM RATINGS¹

Parameter	Symbol	Test Conditions	Min	Max	Units
Drain-Source Voltage	V _{DS}	-3V < V _{GS} < +0V		12	V
Gate-Source Voltage	V _{GS}	0V < V _{DS} < +8V		-3	V
Drain-Source Current	I _{DS}	For V _{DS} > 2V		I _{DSS}	mA
Gate Current	I _G	Forward / Reverse current		+20/-20	mA
RF Input Power ²	P _{IN}	Under any acceptable bias state		575	mW
Channel Operating Temperature	T _{CH}	Under any acceptable bias state		175	°C
Storage Temperature	T _{STG}	Non-Operating Storage	-40	150	°C
Total Power Dissipation	P _{TOT}	See De-Rating Note below		6.0	W
Gain Compression	Comp.	Under any bias conditions		5	dB
Simultaneous Combination of Limits ³		2 or more Max. Limits		80	%

¹T_{Ambient} = 22°C unless otherwise noted ²Max. RF Input Limit must be further limited if input VSWR > 2.5:1

³Users should avoid exceeding 80% of 2 or more Limits simultaneously

Notes:

- Operating conditions that exceed the Absolute Maximum Ratings will result in permanent damage to the device.
- Total Power Dissipation defined as: P_{TOT} ≡ (P_{DC} + P_{IN}) – P_{OUT}, where:
 P_{DC}: DC Bias Power
 P_{IN}: RF Input Power
 P_{OUT}: RF Output Power

- Total Power Dissipation to be de-rated as follows above 22°C:
 $P_{TOT} = 3.5 - (0.04W/°C) \times T_{PACK}$
 where T_{PACK} = source tab lead temperature above 22°C
 (coefficient of de-rating formula is the Thermal Conductivity)

Example: For a 55°C source lead temperature: P_{TOT} = 6.0 - (0.04 x (55 – 22)) = 4.68W

- For optimum heatsinking, metal-filled through (Source) via holes should be used directly below the central metallized ground pad on the bottom of the package.**
- Note on Thermal Resistivity:* The nominal value of 25°C/W is measured with the package mounted on a large heatsink with thermal compound to ensure adequate (unsoldered) contact. The package temperature is referred to the Source leads.

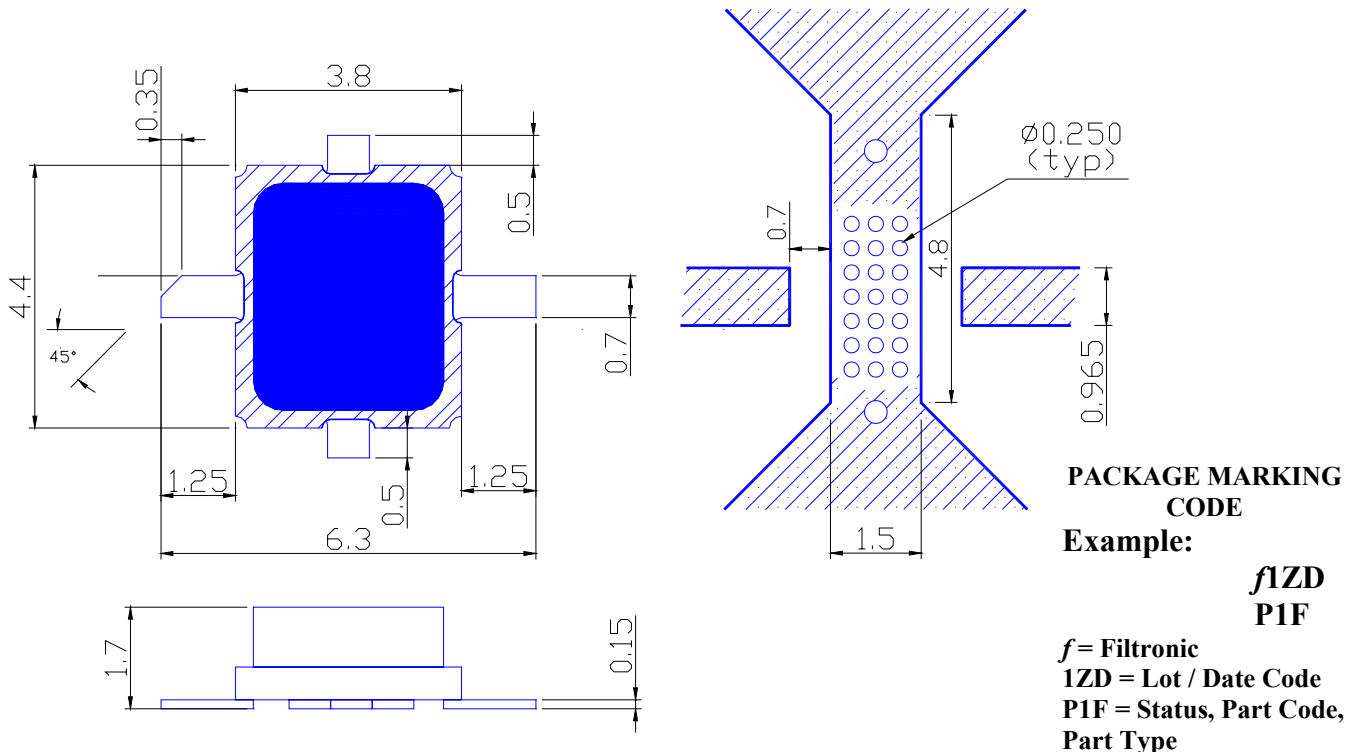
- HANDLING PRECAUTIONS

To avoid damage to the devices care should be exercised during handling. Proper Electrostatic Discharge (ESD) precautions should be observed at all stages of storage, handling, assembly, and testing. This product has been tested to Class 1A (> 250V but < 500V) using JESD22 A114, Human Body Model, and to Class A, (< 200V) using JESD22 A115, Machine Model.

- BIASING GUIDELINES

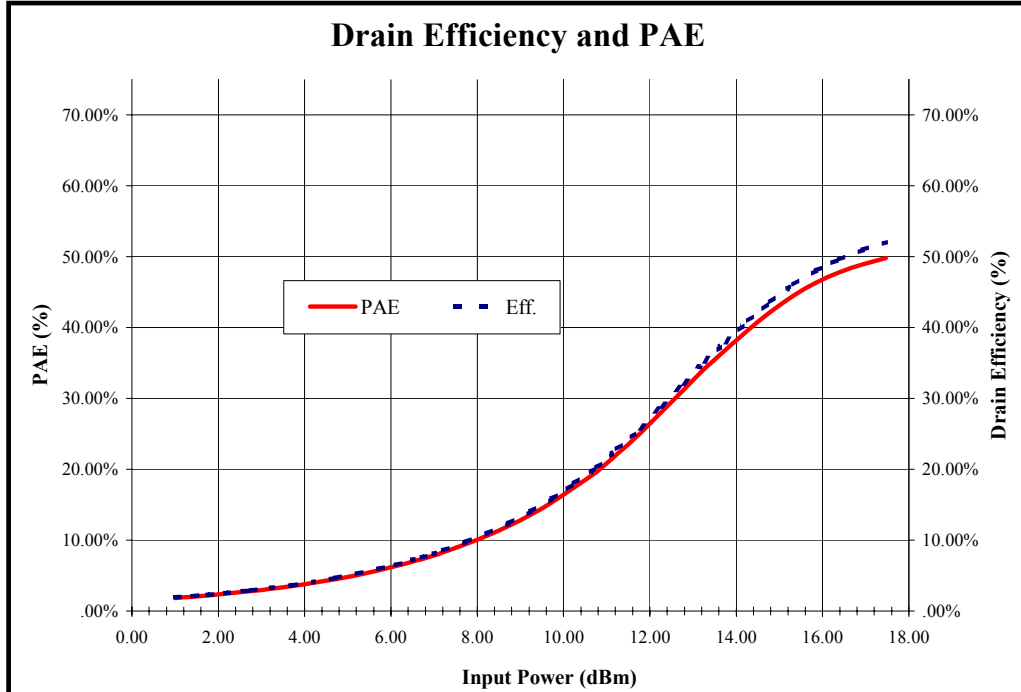
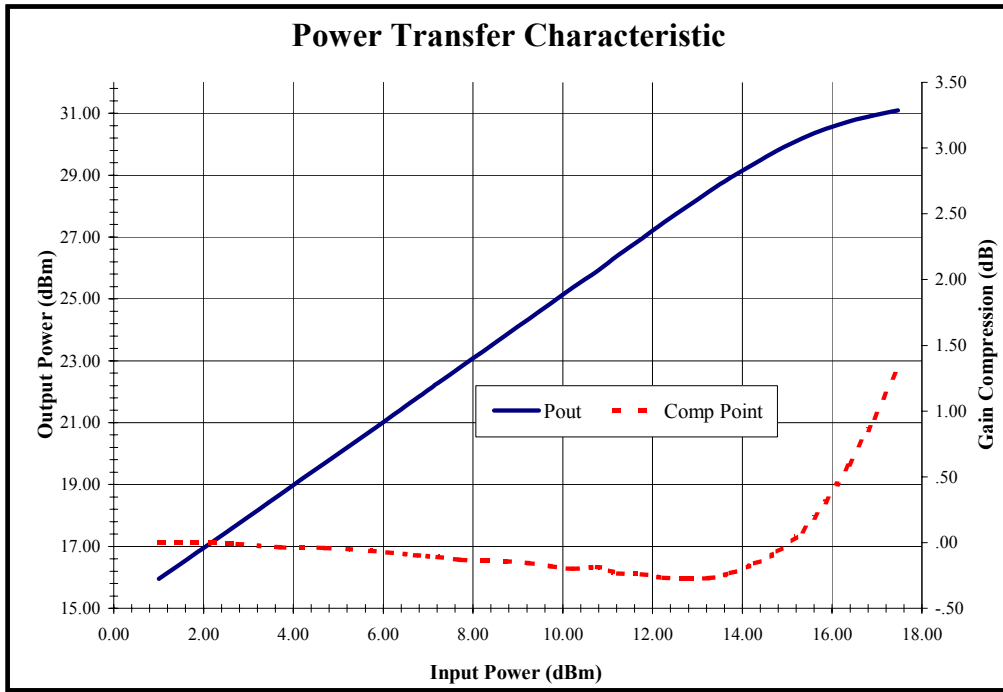
- Active bias circuits provide good performance stabilization over variations of operating temperature, but require a larger number of components compared to self-bias or dual-biased. Such circuits should include provisions to ensure that Gate bias is applied before Drain bias, otherwise the pHEMT may be induced to self-oscillate. Contact your Sales Representative for additional information.
- Dual-bias circuits are relatively simple to implement, but will require a regulated negative voltage supply for depletion-mode devices such as the FPD1000AS.
- Self-biased circuits employ an RF-bypassed Source resistor to provide the negative Gate-Source bias voltage, and such circuits provide some temperature stabilization for the device. A nominal value for circuit development is 3.25Ω for the recommended 200mA operating point.
- The recommended 200mA bias point is nominally a Class AB mode. A small amount of RF gain expansion prior to the onset of compression is normal for this operating point.

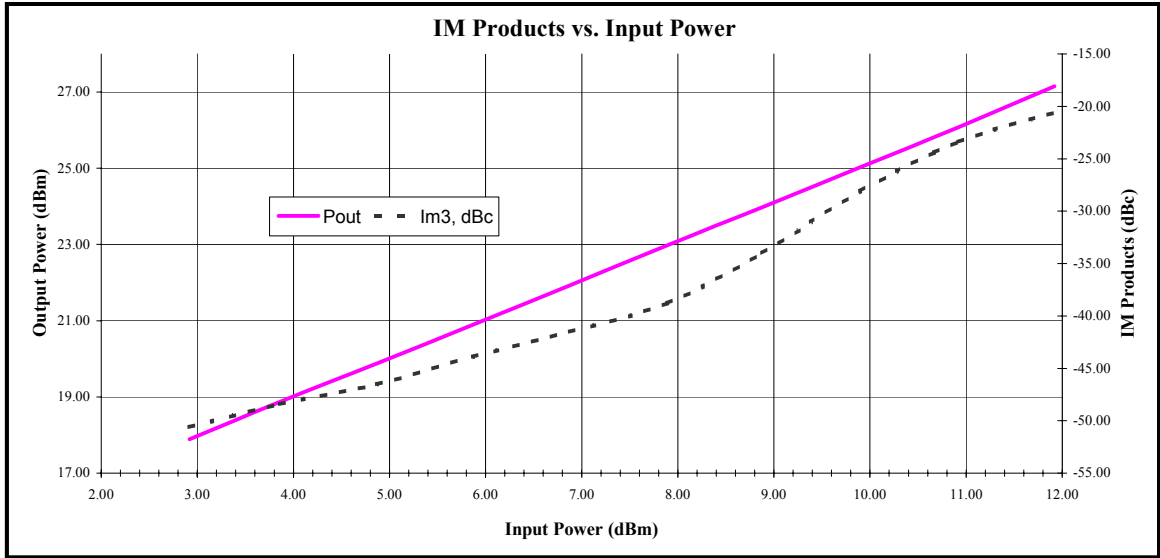
- PACKAGE OUTLINE AND RECOMMENDED PC BOARD LAYOUT
(dimensions in millimeters – mm)



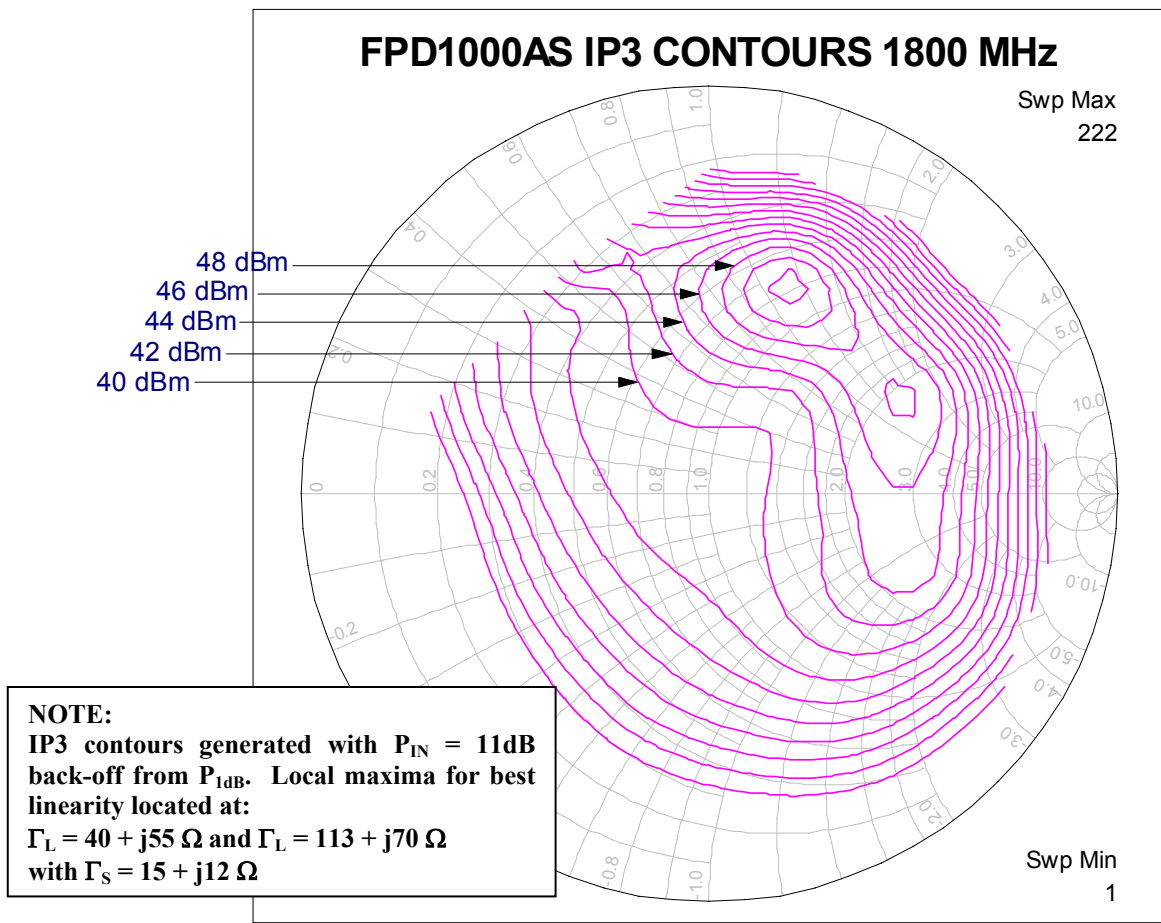
All information and specifications subject to change without notice.

- TYPICAL RF PERFORMANCE ($V_{DS} = 10V$ $I_{DS} = 200mA$ $f = 1800$ MHz):

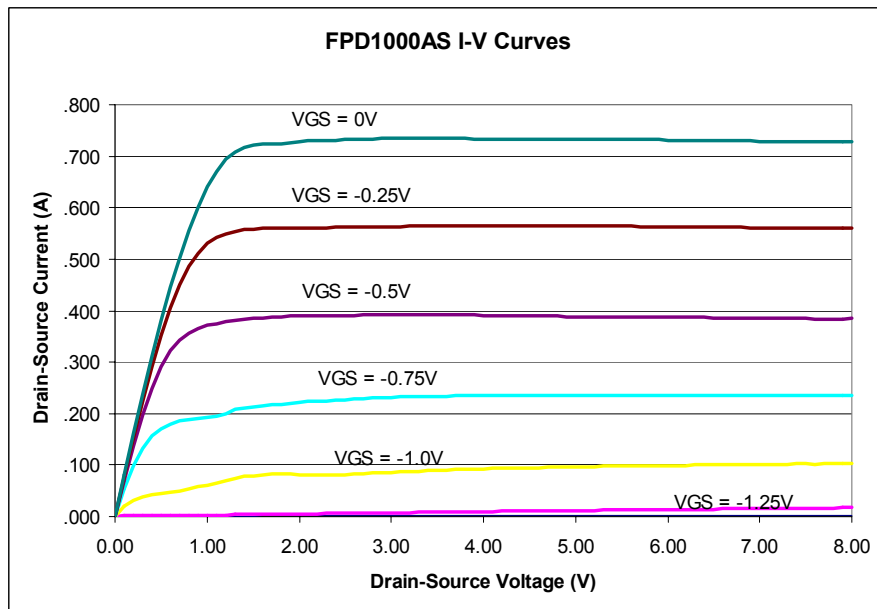
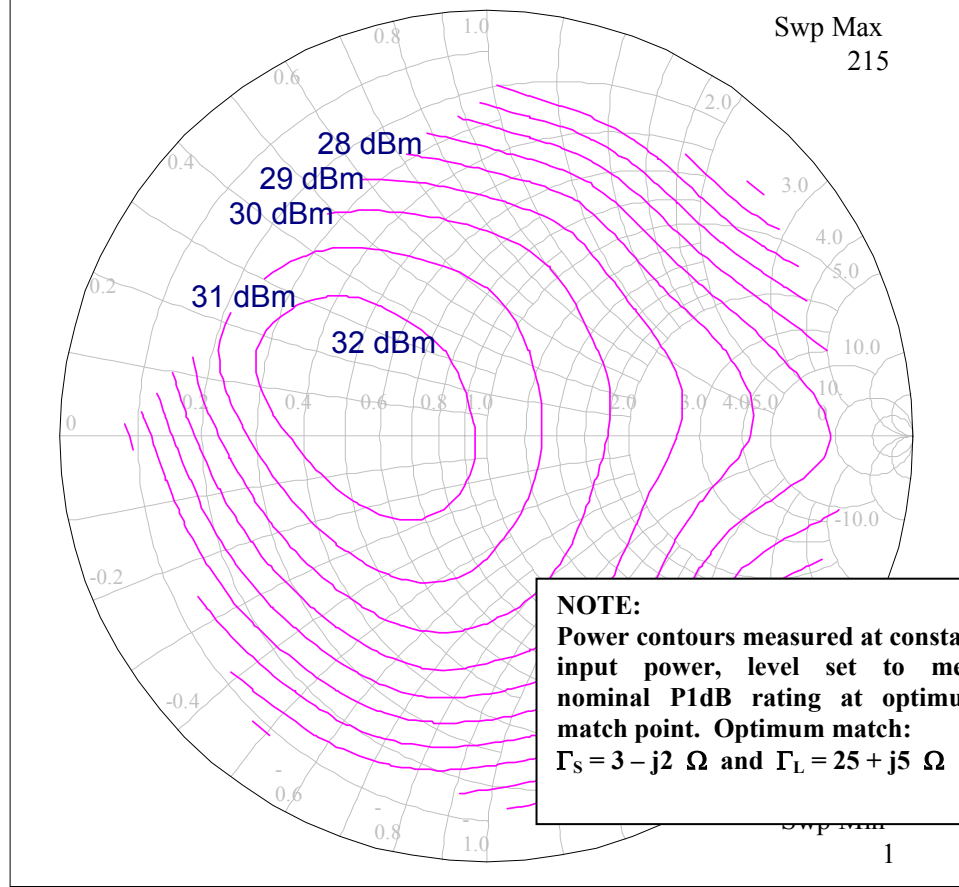




Note: Graph above shows Input and Output power as single carrier or single-tone levels.

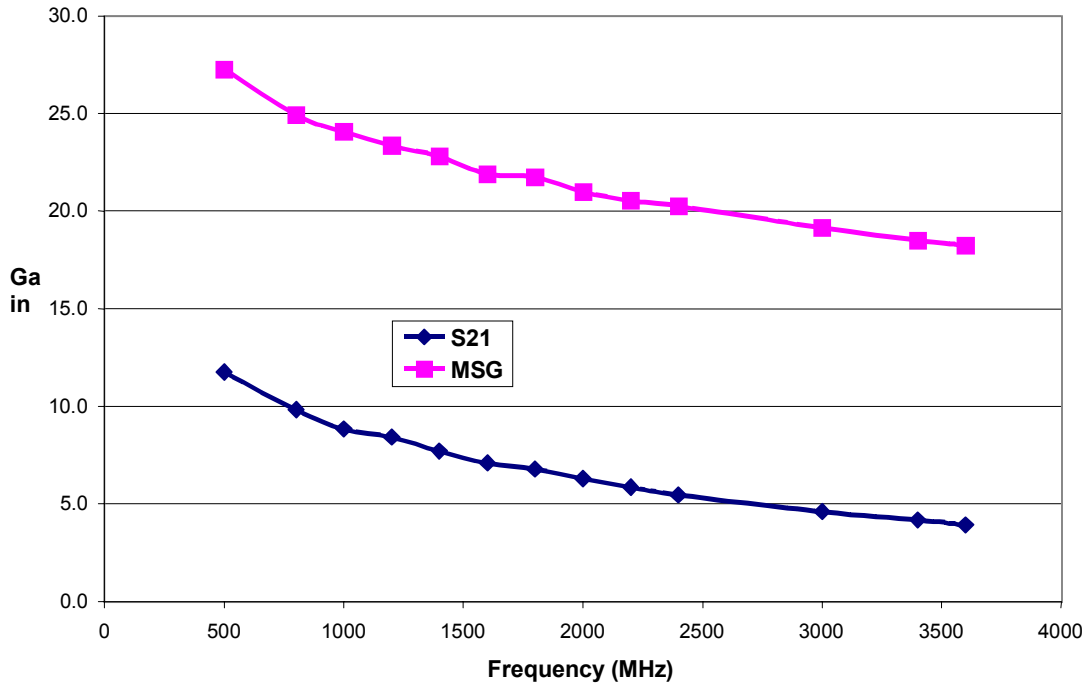


FPD1000AS POWER CONTOURS 1800 MHz

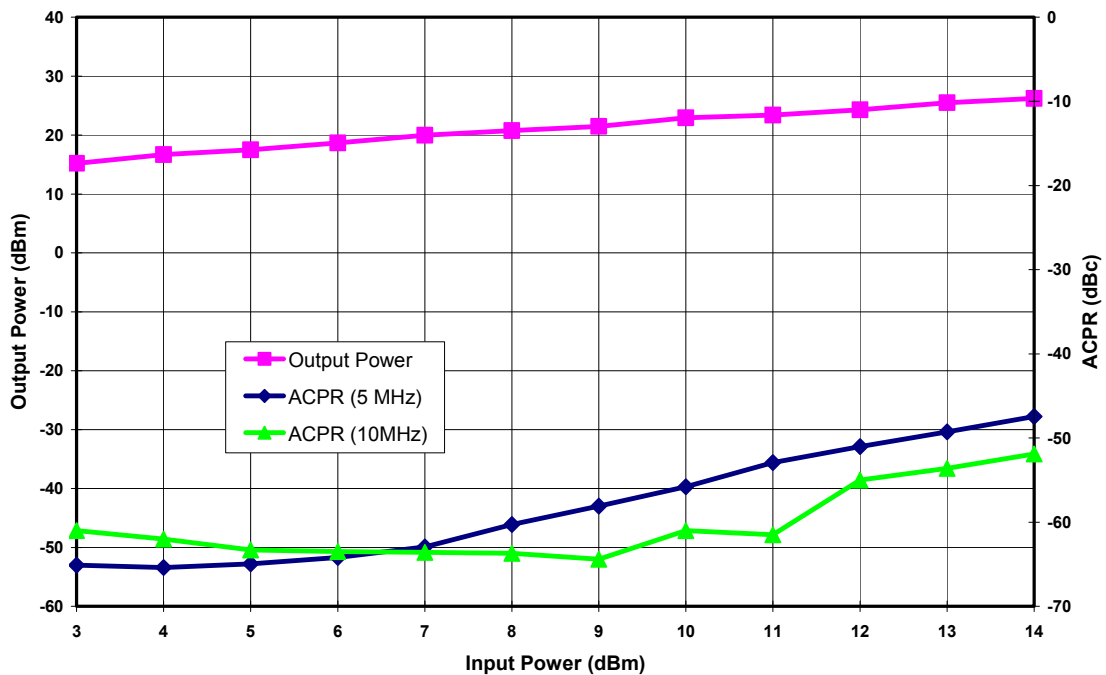


• RF PERFORMANCE OVER FREQUENCY:

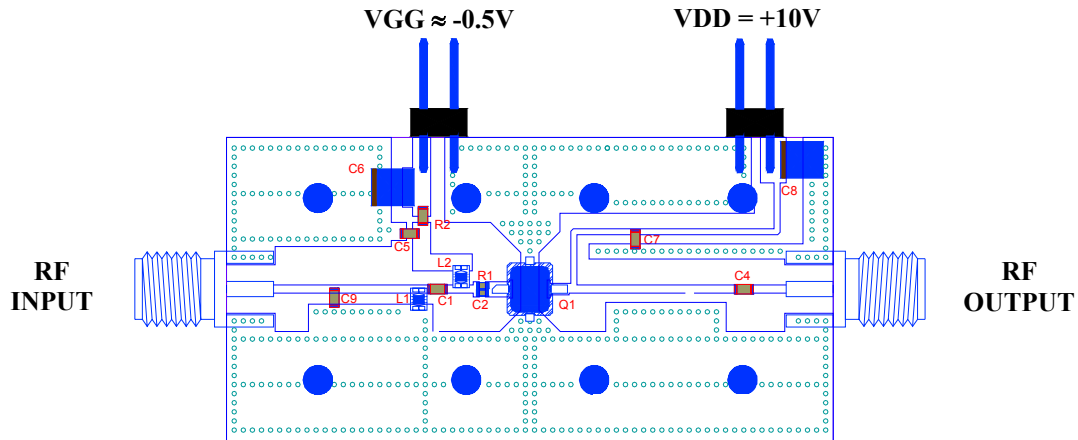
FPD1000AS at VDS = 10V and IDS = 200mA



**FPD1000AS WCDMA ACPR 1900 MHz
DOWNLINK Pk/Avg = 9dB 0.01%**



- STANDARD EVALUATION BOARD (1.70–1.85 GHz):
See Website for complete list of Evaluation Boards



NOTE: AutoCAD™ drawing available on Website. (Model EL-BD-000011-006-A)

BILL OF MATERIALS

Designator	Manufacturer's Part Number	Description	Quantity
C1	ATC600S3R9CW250	Capacitor, 3.9 pF, 0603, ATC 600, tol. $\pm 0.25\text{pF}$	1
C2	ATC600S5R6CW250	Capacitor, 5.6 pF, 0603, ATC 600, tol. $\pm 0.25\text{pF}$	1
C3		Deleted	
C4	ATC600S330JW250	Capacitor, 33 pF, 0603, ATC 600, tol. $\pm 5\%$	1
C5	ATC600S330JW250	Capacitor, 33 pF, 0603, ATC 600, tol. $\pm 5\%$	1
C6	T491B105M035AS7015	Capacitor, 1 mF, SMD-B, Kemet, tol. $\pm 20\%$	1
C7	ATC600S680JW250	Capacitor, 68 pF, 0603, ATC 600	1
C8	T491B105M035AS7015	Capacitor, 1 mF, SMD-B, Kemet, tol. $\pm 20\%$	1
C9	ATC600S2R0BW250	Capacitor, 2 pF, 0603, ATC 600, tol. $\pm 0.1\text{pF}$	1
L1	0604HQ-1N1	Inductor, 1.1 nH, Coilcraft High Q Surface	1
L2	0604HQ-1N1	Inductor, 1.1 nH, Coilcraft High Q Surface	1
R1	RCI-0402-27R0J	Resistor, 27 W, 0402, IMS, tol. $\pm 5\%$	1
R2	RCI-0603-12R0J	Resistor, 12 W, 0603, IMS, tol. $\pm 5\%$	1
Q1	FPD1000AS	1w Packaged Power pHEMT, Filtronic	1
	PC-SP-000010-006	PCB, Rogers R04003, 0.012"(0.3mm), 0.5oz. Cu	1
	TF-SP-000012	Carrier	1
	142-0711-841	Connector, RF, SMA End Launch, Jack Assy,	2
	AMP-103185-2	Connector, DC, 0.100 on center, 0.025 sq. posts,	2
	TF-SP-000003	Center Block for P100 Package	1
		Screw, #0-80	8

NOTE: 10-12 mil (0.3mm) plated thru vias used; vias under Q1 should be filled with Dupont CB100 conductive via plugging material in order to achieve optimal heatsinking.