FAIRCHILD
SEMICONDUCTOR TM

January 1999

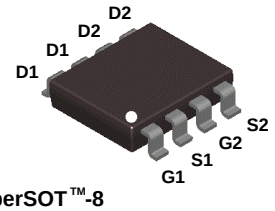
NDH8321C
Dual N & P-Channel Enhancement Mode Field Effect Transistor

General Description

These dual N- and P -Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

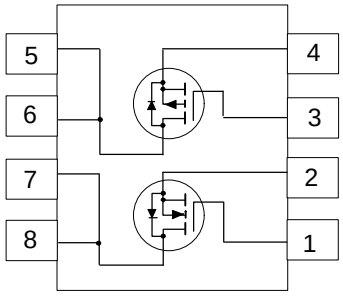
Features

- N-Ch 3.8 A, 20 V, $R_{DS(ON)}$=0.035 Ω @ V_{GS}= 4.5 V
  $R_{DS(ON)}$=0.045 Ω @ V_{GS}=2.7 V
  P-Ch -2.7 A, -20V, $R_{DS(ON)}$=0.07Ω @ V_{GS}= -4.5 V
  $R_{DS(ON)}$=0.095 Ω @ V_{GS}= -2.7 V.
- Proprietary SuperSOT™-8 package design using copper lead frame for superior thermal and electrical capabilities.
- High density cell design for extremely low $R_{DS(ON)}$.
- Exceptional on-resistance and maximum DC current capability.



SuperSOT™-8

Mark: .8321C



Absolute Maximum Ratings T_A= 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V_{DSS}	Drain-Source Voltage	20	-20	V
V_{GSS}	Gate-Source Voltage	±8	±8	V
I_D	Drain Current - Continuous (Note 1)	3.8	-2.7	A
	- Pulsed	15	-10	
P_D	Power Dissipation for Single Operation (Note 1)	0.8		W
T_J,T_{STG}	Operating and Storage Temperature Range	-55 to 150		°C
THERMAL CHARACTERISTICS				
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	156		°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	40		°C/W

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	N-Ch	20			V
		V_{GS} = 0 V, I_D = -250 µA	P-Ch	-20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V	N-Ch			1	µA
		T_J = 55°C				10	µA
		V_{DS} = -16 V, V_{GS} = 0 V	P-Ch			-1	µA
		T_J = 55°C				-10	µA
I_{GSSF}	Gate - Body Leakage, Forward	V_{GS} = 8 V, V_{DS} = 0 V	All			100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	V_{GS} = -8 V, V_{DS} = 0 V	All			-100	nA
ON CHARACTERISTICS (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	N-Ch	0.4	0.7	1	V
		T_J = 125°C		0.3	0.45	0.8	
		V_{DS} = V_{GS}, I_D = -250 µA	P-Ch	-0.4	-0.7	-1	
		T_J = 125°C		-0.3	-0.5	-0.8	
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS} = 4.5 V, I_D = 3.8 A	N-Ch		0.029	0.035	Ω
		T_J = 125°C			0.043	0.063	
		V_{GS} = 2.7 V, I_D = 3.3 A			0.036	0.045	
		V_{GS} = -4.5 V, I_D = -2.7 A	P-Ch		0.061	0.07	
		T_J = 125°C			0.087	0.125	
		V_{GS} = -2.7 V, I_D = -2.3A			0.082	0.095	
$I_{D(on)}$	On-State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	N-Ch	15			A
		V_{GS} = 2.7 V, V_{DS} = 5 V		5			
		V_{GS} = -4.5 V, V_{DS} = -5 V	P-Ch	-10			
		V_{GS} = -2.7 V, V_{DS} = -5 V		-3			
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 3.8 A	N-Ch		15		S
		V_{DS} = -5 V, I_D = -2.7 A	P-Ch		8		
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	N-Channel V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		700		pF
			P-Ch		865		
C_{oss}	Output Capacitance	P-Channel V_{DS} = -10 V, V_{GS} = 0 V, f = 1.0 MHz	N-Ch		370		pF
			P-Ch		415		
C_{rss}	Reverse Transfer Capacitance		N-Ch		145		pF
			P-Ch		150		

Electrical Characteristics (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Type	Min	Typ	Max	Units
SWITCHING CHARACTERISTICS (Note 2)							
$t_{D(on)}$	Turn - On Delay Time	N-Channel V_{DD} = 5 V, I_D = 1 A, V_{GEN} = 4.5 V, R_{GEN} = 6 Ω	N-Ch		8	15	ns
			P-Ch		11	22	
t_r	Turn - On Rise Time	P-Channel V_{DD} = -5 V, I_D = -1 A, V_{GEN} = -4.5 V, R_{GEN} = 6 Ω	N-Ch		22	40	ns
			P-Ch		25	50	
$t_{D(off)}$	Turn - Off Delay Time		N-Ch		48	90	ns
			P-Ch		78	150	
t_f	Turn - Off Fall Time		N-Ch		23	40	ns
			P-Ch		55	100	
Q_g	Total Gate Charge	N-Channel V_{DS} = 10 V, I_D = 3.8 A, V_{GS} = 4.5 V	N-Ch		19.6	28	nC
			P-Ch		16	23	
Q_{gs}	Gate-Source Charge	P-Channel V_{DS} = -10 V, I_D = -2.7 A, V_{GS} = -4.5 V	N-Ch		2.5		nC
			P-Ch		2.4		
Q_{gd}	Gate-Drain Charge		N-Ch		6.5		nC
			P-Ch		5.1		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS							
I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			0.67	A
			P-Ch			-0.67	
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.67 A (Note2)	N-Ch		0.65	1.2	V
		V_{GS} = 0 V, I_S = -0.67 A (Note2)	P-Ch		-0.7	-1.2	

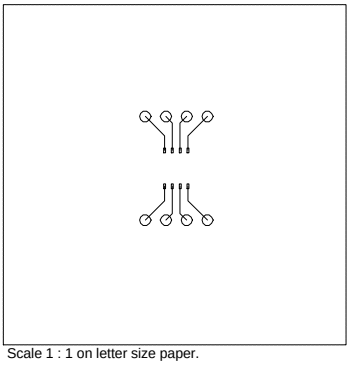
Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

$$P_D(t) = \frac{T_J - T_A}{R_{\theta JA}(t)} = \frac{T_J - T_A}{R_{\theta JC} + R_{\theta CA}(t)} = I_D^2(t) \times R_{DS(ON)@T_J}$$

Typical $R_{\theta JA}$ for single device operation using the board layout shown below on 4.5"x5" FR-4 PCB in a still air environment:

156°C/W when mounted on a 0.0025 in^2 pad of 2oz copper.



Scale 1 : 1 on letter size paper.

2. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2.0%.

Typical Electrical Characteristics: N-Channel

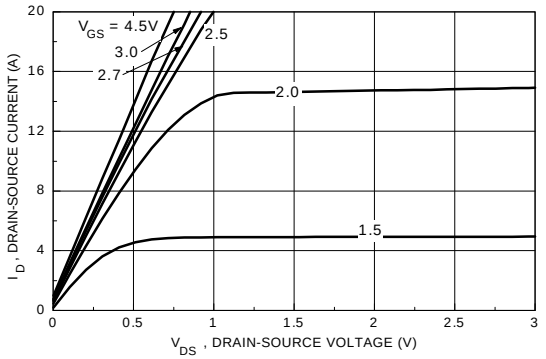


Figure 1. N-Channel On-Region Characteristics.

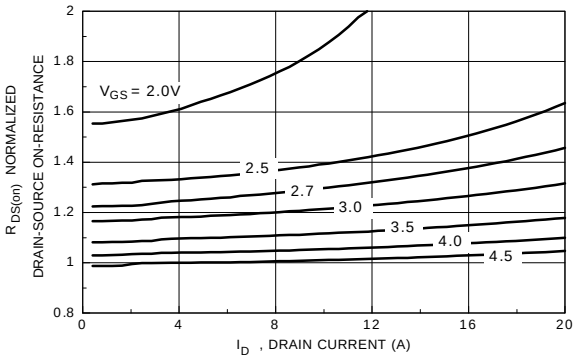


Figure 2. N-Channel On-Resistance Variation with Gate Voltage and Drain Current.

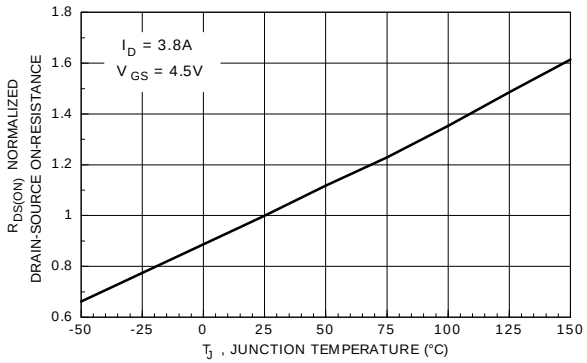


Figure 3. N-Channel On-Resistance Variation with Temperature.

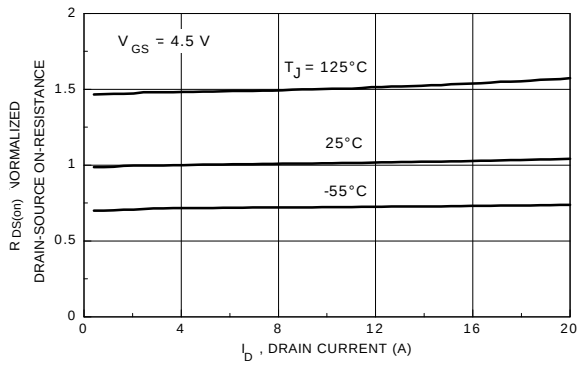


Figure 4. N-Channel On-Resistance Variation with Drain Current and Temperature.

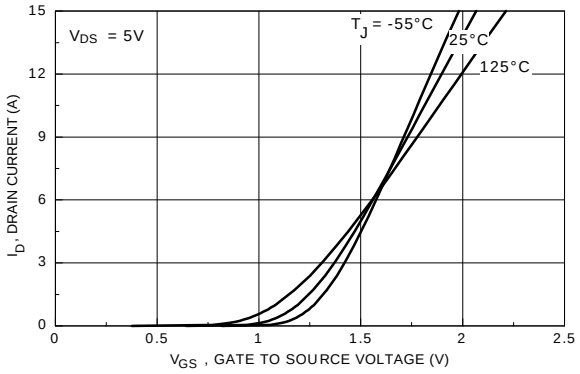


Figure 5. N-Channel Transfer Characteristics.

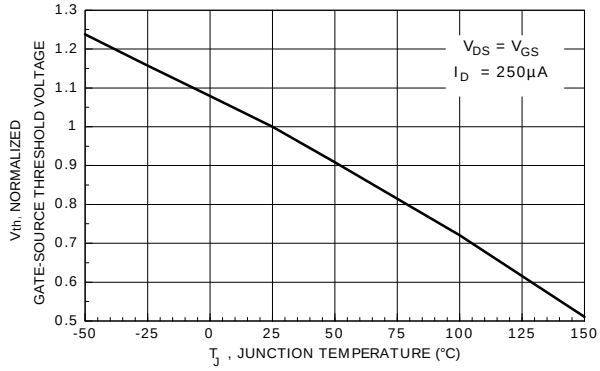


Figure 6. N-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: N-Channel (continued)

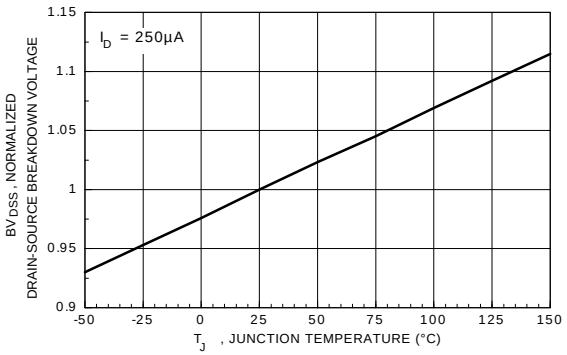


Figure 7. N-Channel Breakdown Voltage Variation with Temperature.

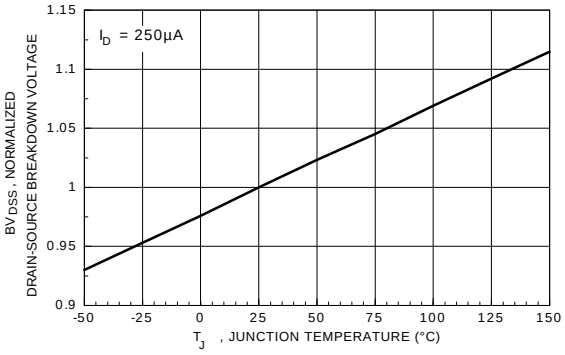


Figure 8. N-Channel Body Diode Forward Voltage Variation with Current and Temperature.

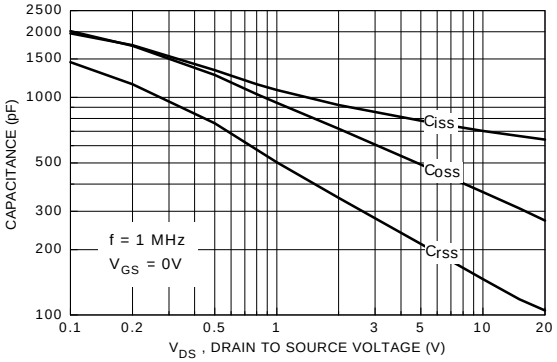


Figure 9. N-Channel Capacitance Characteristics.

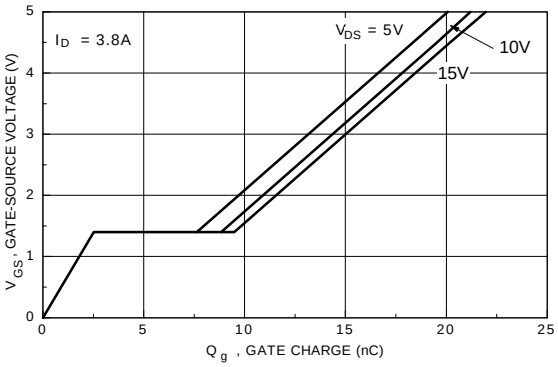


Figure 10. N-Channel Gate Charge Characteristics.

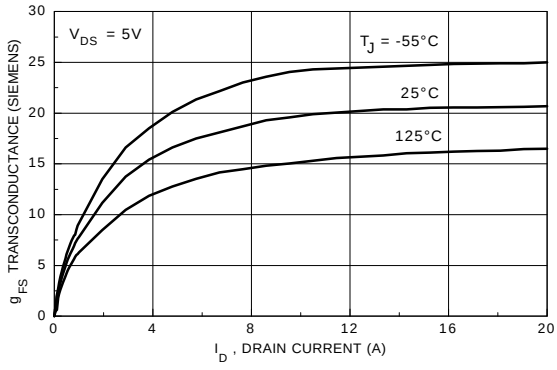


Figure 11. N-Channel Transconductance Variation with Drain Current and Temperature.

Typical Electrical Characteristics: P-Channel (continued)

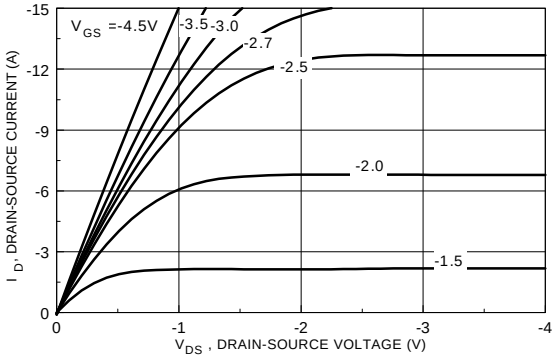


Figure 12. P-Channel On-Region Characteristics.

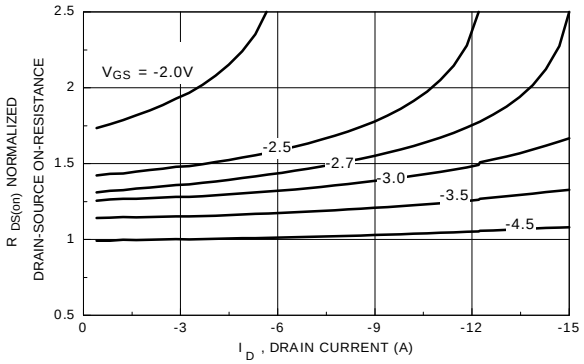


Figure 13. P-Channel On-Resistance Variation with Gate Voltage and Drain Current.

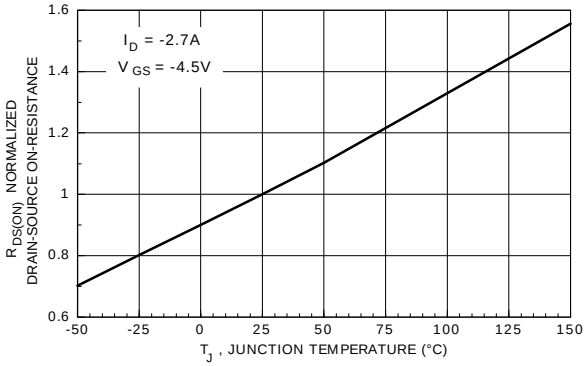


Figure 14. P-Channel On-Resistance Variation with Temperature.

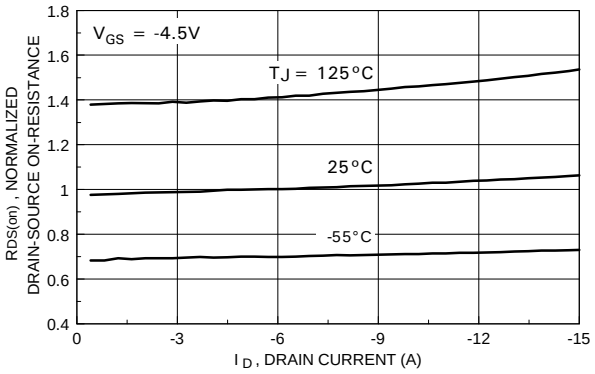


Figure 15. P-Channel On-Resistance Variation with Drain Current and Temperature.

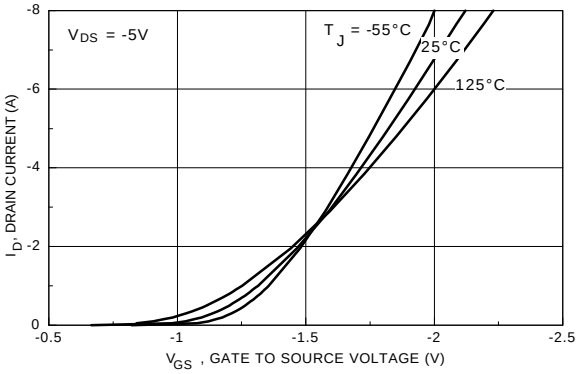


Figure 16. P-Channel Transfer Characteristics.

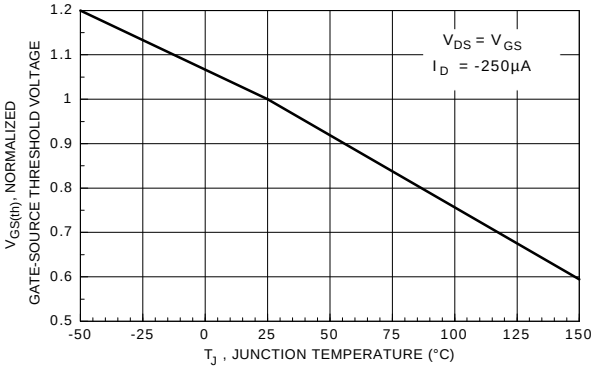


Figure 17. P-Channel Gate Threshold Variation with Temperature.

Typical Electrical Characteristics: P-Channel (continued)

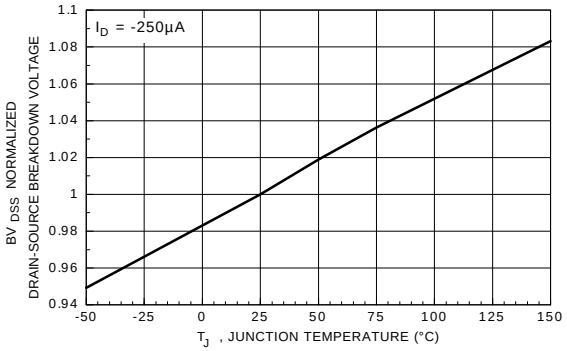


Figure 18. P-Channel Breakdown Voltage Variation with Temperature.

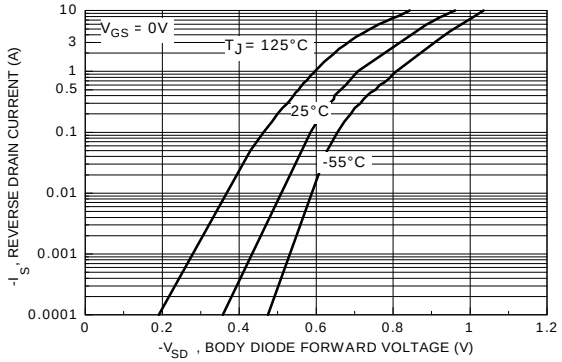


Figure 19. P-Channel Body Diode Forward Voltage Variation with Current and Temperature.

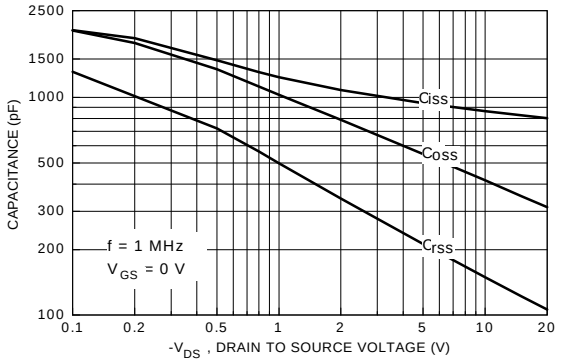


Figure 20. P-Channel Capacitance Characteristics.

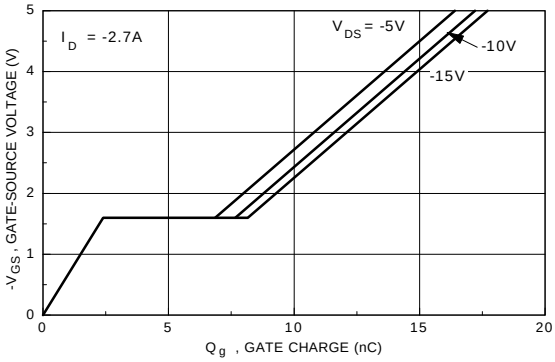


Figure 21. P-Channel Gate Charge Characteristics.

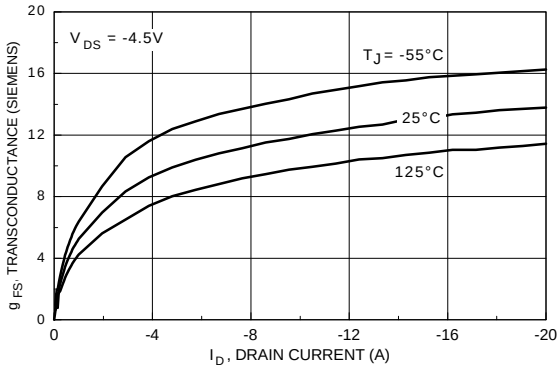


Figure 22. P-Channel Transconductance Variation with Drain Current and Temperature.

Typical Thermal Characteristics: N & P-Channel

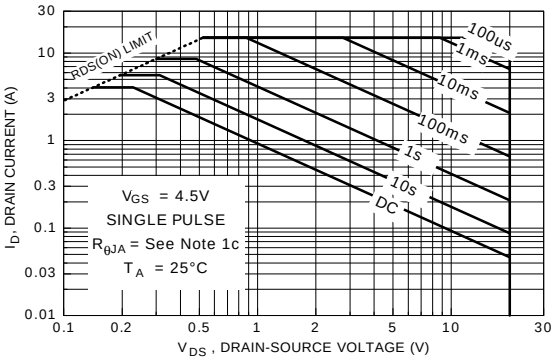


Figure 23. N-Channel Maximum Safe Operating Area.

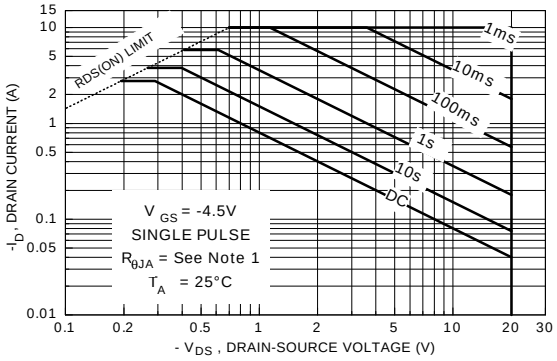


Figure 24. P-Channel Maximum Safe Operating Area.

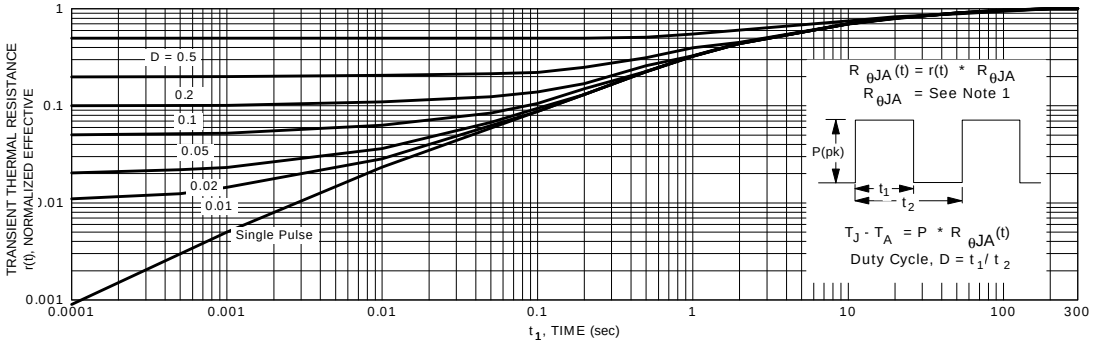


Figure 25. Transient Thermal Response Curve.

Note: Thermal characterization performed using the conditions described in note1 . Transient thermal response will change depending on the circuit board design.

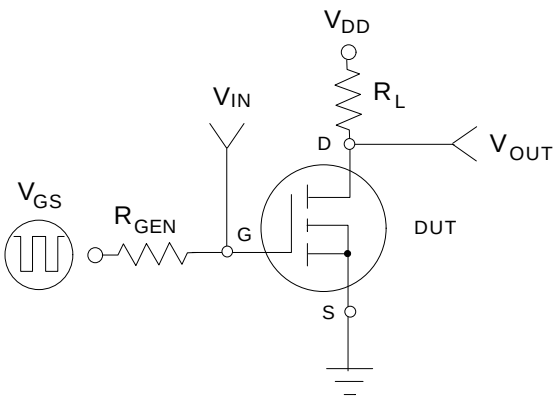


Figure 26. N or P-Channel Switching Test Circuit.

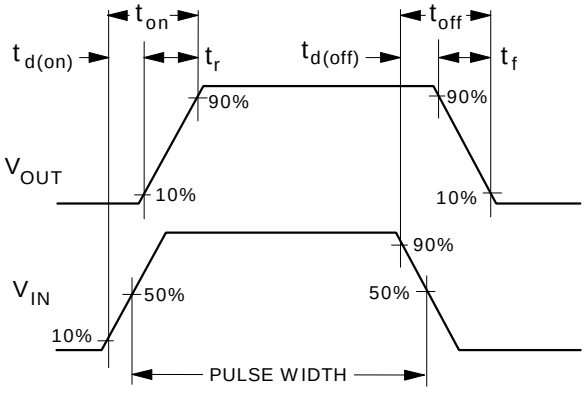
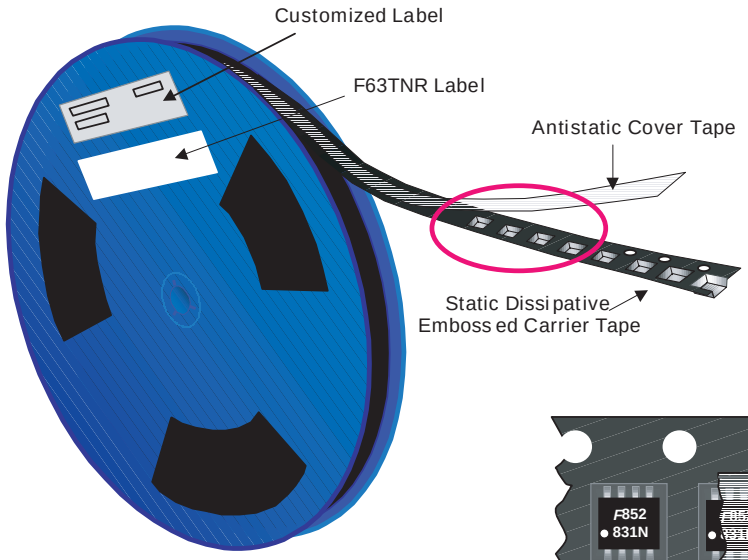


Figure 27. N or P-Channel Switching Waveforms.

SuperSOT™-8 Tape and Reel Data and Package Dimensions

FAIRCHILD SEMICONDUCTOR™

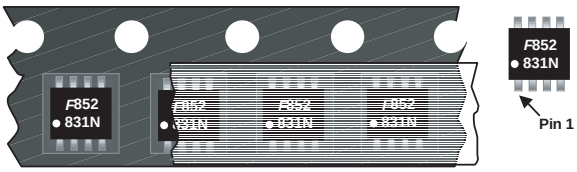
SSOT-8 Packaging Configuration: Figure 1.0



Packaging Description:

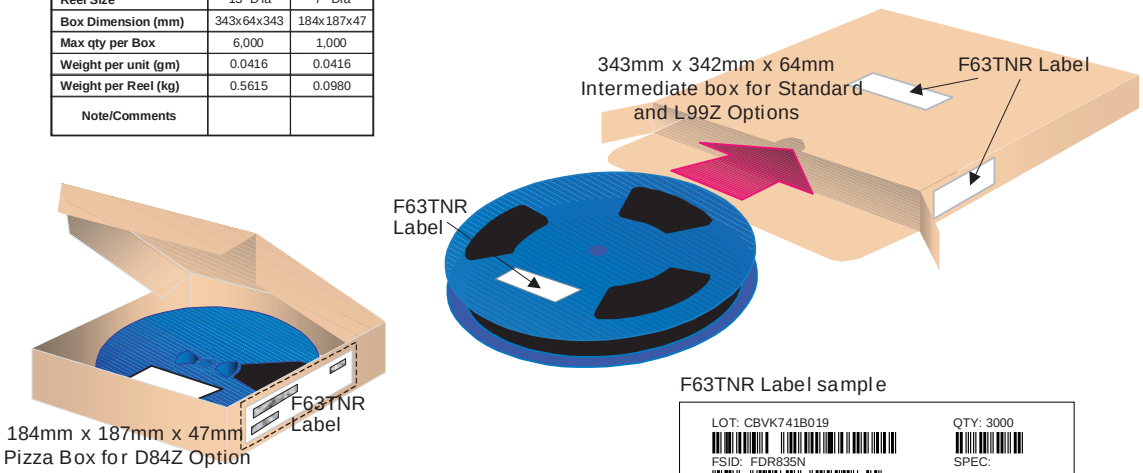
SSOT-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 3,000 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

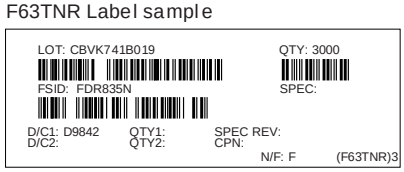


SSOT-8 Unit Orientation

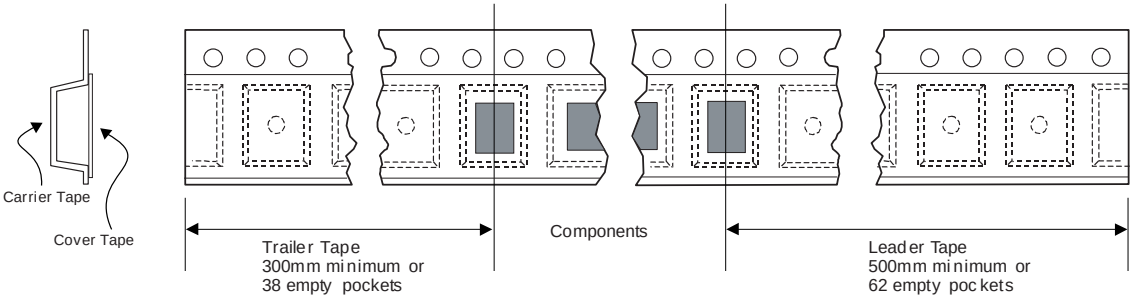
SSOT-8 Packaging Information		
Packaging Option	Standard (no flow code)	D84Z
Packaging type	TNR	TNR
Qty per Reel/Tube/Bag	3,000	500
Reel Size	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	184x187x47
Max qty per Box	6,000	1,000
Weight per unit (gm)	0.0416	0.0416
Weight per Reel (kg)	0.5615	0.0980
Note/Comments		



F63TNR Label sample



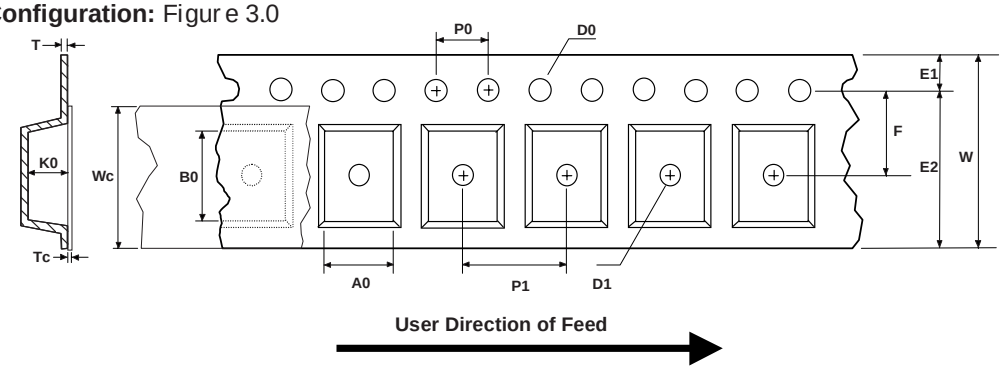
SSOT-8 Tape Leader and Trailer Configuration: Figure 2.0



SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SSOT-8 Embossed Carrier Tape

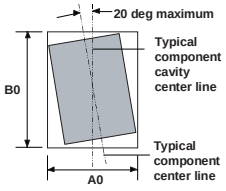
Configuration: Figure 3.0



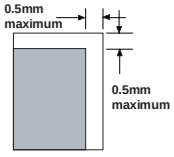
Dimensions are in millimeter														
Pkg type	**A0**	**B0**	**W**	**D0**	**D1**	**E1**	**E2**	**F**	**P1**	**P0**	**K0**	**T**	**Wc**	**Tc**
SSOT-8 (12mm)	4.47 +/-0.10	5.00 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.50 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	1.37 +/-0.10	0.280 +/-0.150	9.5 +/-0.025	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).

Sketch A (Side or Front Sectional View)
Component Rotation

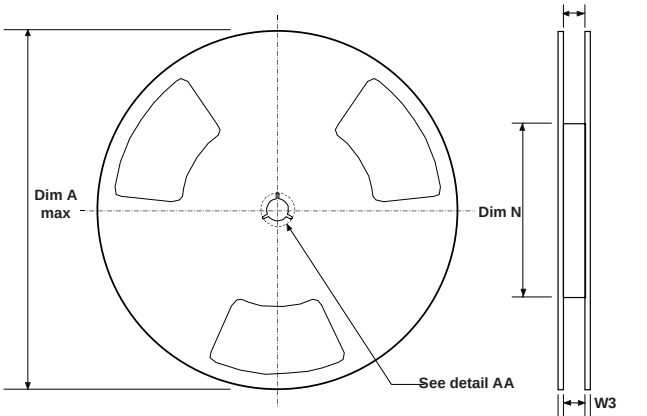


Sketch B (Top View)
Component Rotation

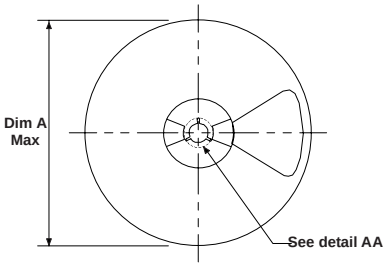


Sketch C (Top View)
Component lateral movement

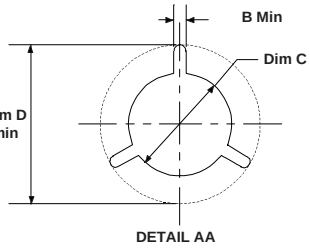
SSOT-8 Reel Configuration: Figure 4.0



13" Diameter Option



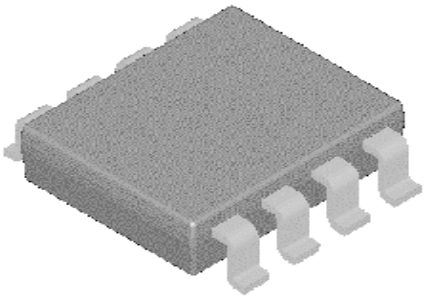
7" Diameter Option

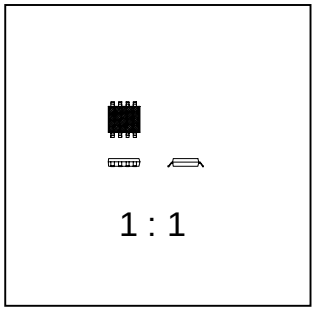


Dimensions are in inches and millimeters									
Tape Size	**Reel Option**	**Dim A**	**Dim B**	**Dim C**	**Dim D**	**Dim N**	**Dim W1**	**Dim W2**	**Dim W3 (LSL-USL)**
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	5.906 150	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 – 0.606 11.9 – 15.4

SuperSOT™-8 Tape and Reel Data and Package Dimensions, continued

SuperSOT™-8 (FS PKG Code 34, 35)

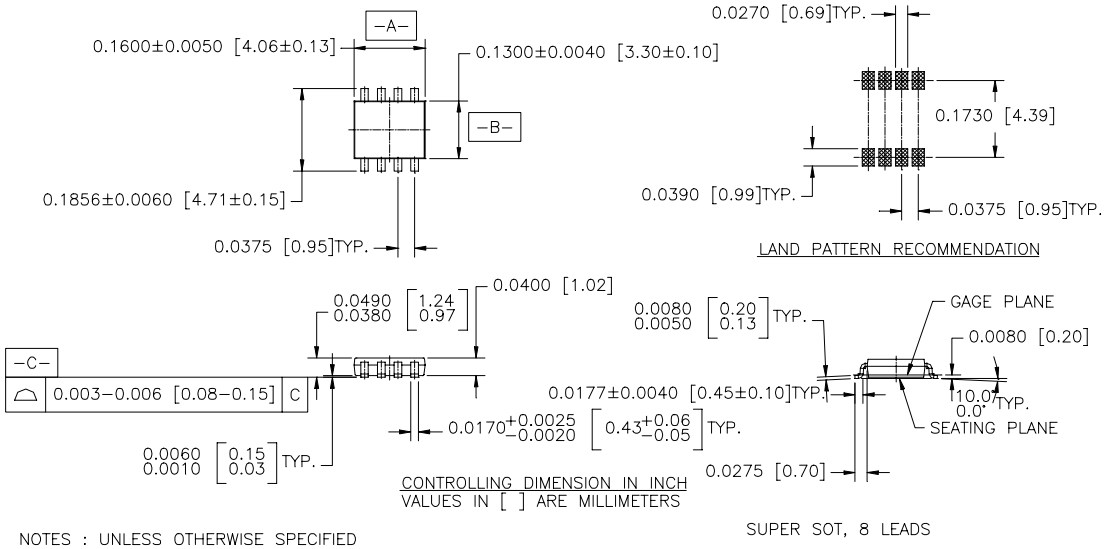




Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0416



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2. NO JEDEC REGISTRATION AS JAN. 1996

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