

# KM4170, KM4270, KM4470

## Low Cost, +2.7V & +5V, Rail-to-Rail I/O Amplifiers

### Features at 2.7V

- 136 $\mu$ A supply current per amplifier
- 4.9MHz bandwidth
- Output swings to within 20mV of either rail
- Input voltage range exceeds the rail by >250mV
- 5.3V/ $\mu$ s slew rate
- 16mA output current
- 21nV/ $\sqrt{\text{Hz}}$  input voltage noise
- KM4170:
  - directly replaces OPA340, OPA343, and TLV2461 in single supply applications and available in SC70-5 and SOT23-5 package options
- KM4270:
  - directly replaces MAX4126, OPA2340, LMV822 and TLV2462 in single supply applications and available in SOIC-8 and MSOP-8 package options
- KM4470:
  - directly replaces MAX4129, OPA4340, LMV824 and TLV2464 in single supply applications and available in TSSOP-14 package option

### Applications

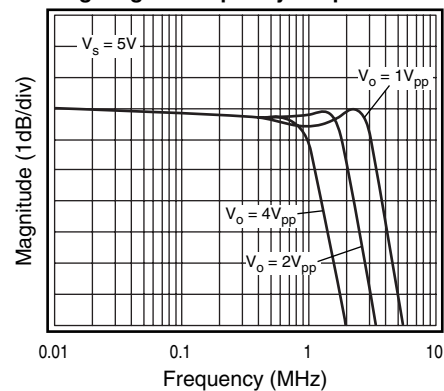
- Portable/battery-powered applications
- PCMCIA, USB
- Mobile communications, cellular phones, pagers
- Notebooks and PDA's
- Sensor Interface
- A/D buffer
- Active filters
- Signal conditioning
- Portable test instruments

### Description

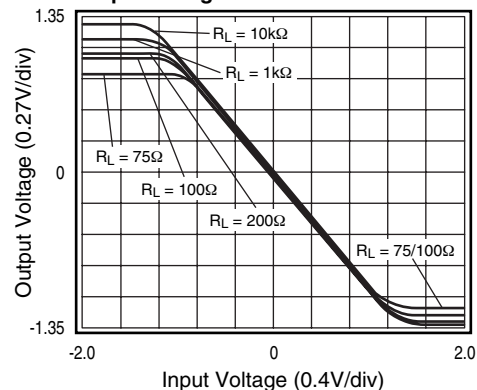
The KM4170 (single), KM4270 (dual), and KM4470 (quad) are ultra-low cost, low power, voltage feedback amplifiers. At 5V, the KM4X70 family uses only 160 $\mu$ A of supply current per amplifier and are designed to operate from a supply range of 2.5V to 5.5V ( $\pm 1.25$  to  $\pm 2.75$ ). The input voltage range exceeds the negative and positive rails.

The KM4X70 family of amplifiers offer high bipolar performance at a low CMOS prices. They offer superior dynamic performance with 4.9MHz small signal bandwidths and 5.3V/ $\mu$ s slew rates. The combination of low power, high bandwidth, and rail-to-rail performance make the KM4X70 amplifiers well suited for battery-powered communication/computing systems.

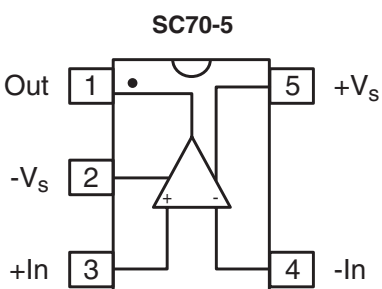
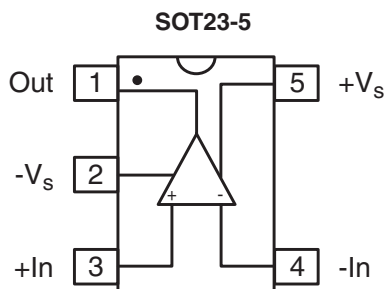
Large Signal Frequency Response



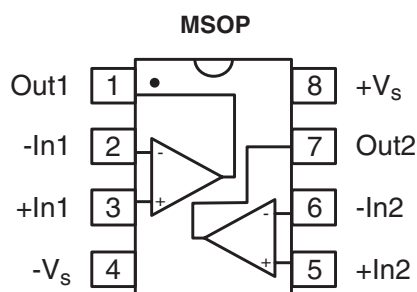
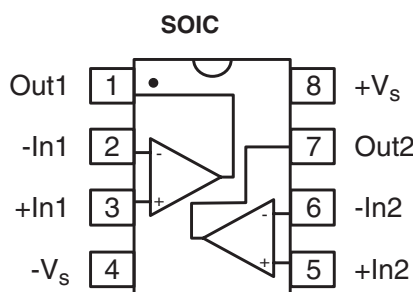
Output Swing vs. Load



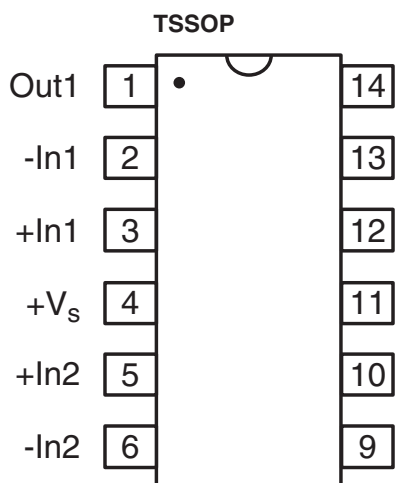
### KM4170



### KM4270



### KM4470



## Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltages	0	+6	V
Maximum Junction Temperature	–	+175	°C
Storage Temperature Range	-65	+150	°C
Lead Temperature, 10 seconds	–	+260	°C
Operating Temperature Range, recommended	-40	+85	°C
Input Voltage Range	$-V_S - 0.5$	$+V_S + 0.5$	V
$I_{out}$ Continuous	-30	+30	mA

## Electrical Specifications

( $V_S = +2.7V$ ,  $G = 2$ ,  $R_L = 10k\Omega$  to  $V_S/2$ ,  $R_f = 5k\Omega$ ; unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>AC Performance</b>					
-3dB Bandwidth <sup>1</sup>	$G = +1$ , $V_O = 0.02V_{pp}$		4.9		MHz
	$G = +2$ , $V_O = 0.2V_{pp}$		3.7		MHz
Full Power Bandwidth	$G = +2$ , $V_O = 2V_{pp}$		1.4		MHz
Gain Bandwidth Product			2.2		MHz
Rise and Fall Time	1V step		163		ns
Overshoot	1V step		<1		%
Slew Rate	1V step		5.3		V/ $\mu$ s
2nd Harmonic Distortion	$1V_{pp}$ , 10kHz		-72		dBc
3rd Harmonic Distortion	$1V_{pp}$ , 10kHz		-72		dBc
THD	$1V_{pp}$ , 10kHz		0.03		%
Input Voltage Noise	>10kHz		21		nV/ $\sqrt{Hz}$
<b>DC Performance</b>					
Input Offset Voltage <sup>2</sup>		-6	0.5	+6	mV
Average Drift			5		$\mu$ V/°C
Input Bias Current <sup>2</sup>			90	420	nA
Average Drift			32		pA/°C
Power Supply Rejection Ratio <sup>2</sup>	DC	55	83		dB
Open Loop Gain	$R_L = 10k\Omega$		90		dB
Quiescent Current Per Channel <sup>2</sup>			136	190	$\mu$ A
<b>Input Characteristics</b>					
Input Resistance			12		M $\Omega$
Input Capacitance			2		pF
Input Common Mode Voltage Range			-0.25 to 2.95		V
Common Mode Rejection Ratio <sup>2</sup>	DC, $V_{cm} = 0V$ to $V_S$	55	81		dB
<b>Output Characteristics</b>					
Output Voltage Swing <sup>2</sup>	$R_L = 10k\Omega$ to $V_S/2$	0.06 to 2.64	0.02 to 2.68		V
	$R_L = 1k\Omega$ to $V_S/2$		0.05 to 2.63		V
	$R_L = 200\Omega$ to $V_S/2$		0.11 to 2.52		V
Output Current			$\pm 16$		mA
Power Supply Operating Range		2.5	2.7	5.5	V

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

### Notes:

- For  $G = +1$ ,  $R_f = 0$ .
- For  $R_L = 10k\Omega$ , KM4170, KM4270, and KM4470 are 100% tested at 25°C.

## Electrical Specifications

( $V_S = +5V$ ,  $G = 2$ ,  $R_L = 10k\Omega$  to  $V_S/2$ ,  $R_f = 5k\Omega$ ; unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>AC Performance</b>					
-3dB Bandwidth <sup>1</sup>	$G = +1$ , $V_O = 0.02V_{pp}$		4.3		MHz
	$G = +2$ , $V_O = 0.2V_{pp}$		3.0		MHz
Full Power Bandwidth	$G = +2$ , $V_O = 2V_{pp}$		2.3		MHz
Gain Bandwidth Product			2.0		MHz
Rise and Fall Time	1V step		110		ns
Overshoot	1V step		<1		%
Slew Rate	1V step		9		V/ $\mu$ s
2nd Harmonic Distortion	1V <sub>pp</sub> , 10kHz		-73		dBc
3rd Harmonic Distortion	1V <sub>pp</sub> , 10kHz		-75		dBc
THD	1V <sub>pp</sub> , 10kHz		0.03		%
Input Voltage Noise	>10kHz		22		nV/ $\sqrt{Hz}$
<b>DC Performance</b>					
Input Offset Voltage <sup>2</sup>		-8	1.5	+8	mV
Average Drift			15		$\mu$ V/ $^{\circ}$ C
Input Bias Current <sup>2</sup>			90	450	nA
Average Drift			40		pA/ $^{\circ}$ C
Power Supply Rejection Ratio <sup>2</sup>	DC	40	60		dB
Open Loop Gain	$R_L = 10k\Omega$		80		dB
Quiescent Current Per Channel <sup>2</sup>			160	235	$\mu$ A
<b>Input Characteristics</b>					
Input Resistance			12		M $\Omega$
Input Capacitance			2		pF
Input Common Mode Voltage Range			-0.25 to 5.25		V
Common Mode Rejection Ratio <sup>2</sup>	DC, $V_{cm} = 0V$ to $V_S$	58	85		dB
<b>Output Characteristics</b>					
Output Voltage Swing <sup>2</sup>	$R_L = 10k\Omega$ to $V_S/2$	0.08 to 4.92	0.04 to 4.96		V
	$R_L = 1k\Omega$ to $V_S/2$		0.07 to 4.9		V
	$R_L = 200\Omega$ to $V_S/2$		0.14 to 4.67		V
Output Current			$\pm 30$		mA
Power Supply Operating Range		2.5	2.7	5.5	V

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

### Notes:

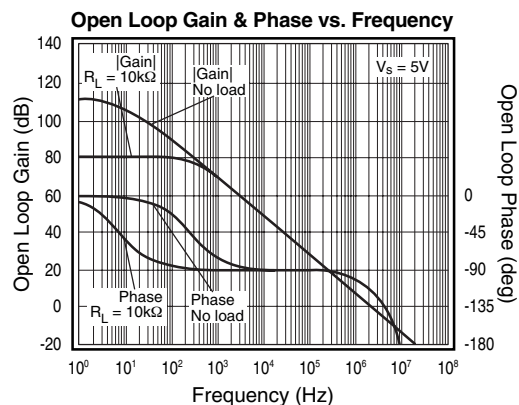
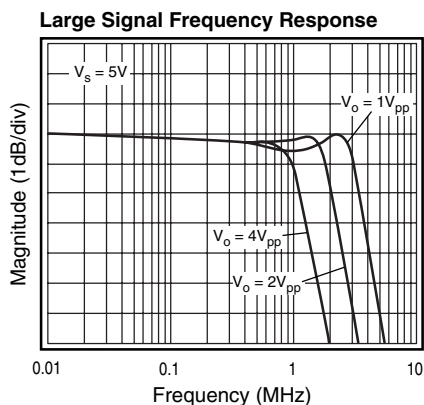
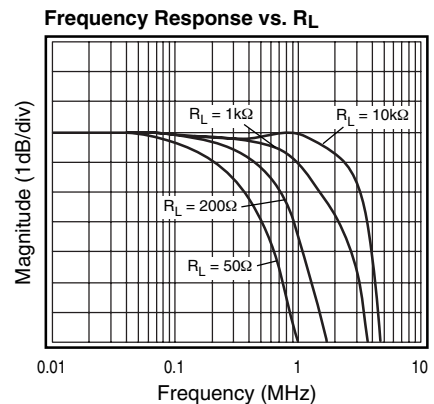
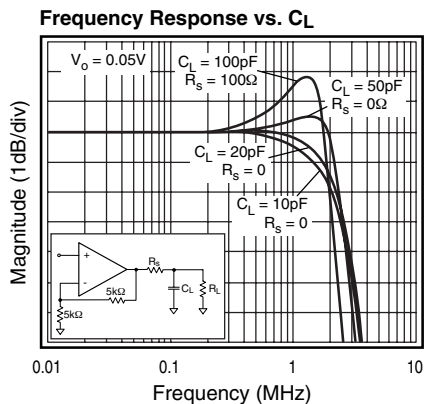
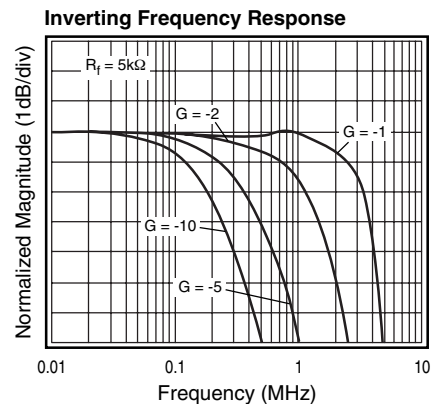
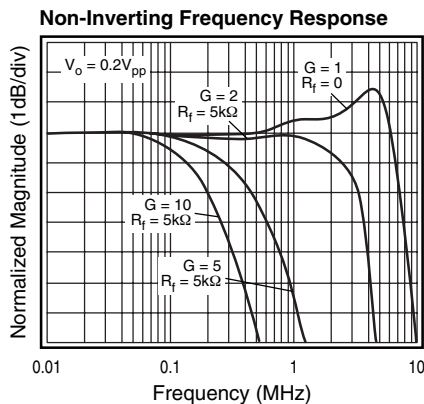
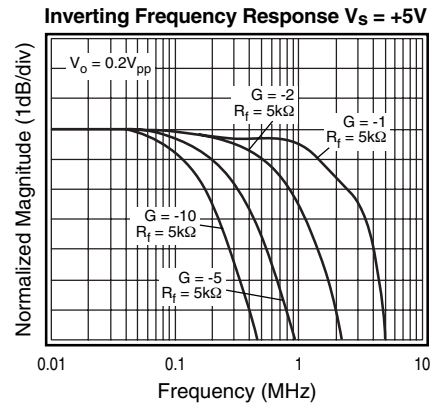
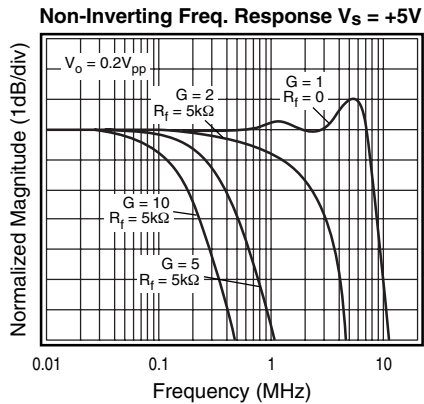
- For  $G = +1$ ,  $R_f = 0$ .
- For  $R_L = 10k\Omega$ , KM4170 is 100% tested at 25 $^{\circ}$ C.

## Package Thermal Resistance

Package	$\theta_{JA}$
5 lead SOT23	256 $^{\circ}$ C/W
5 lead SC70	331.4 $^{\circ}$ C/W
8 lead SOIC	152 $^{\circ}$ C/W
8 lead MSOP	206 $^{\circ}$ C/W
14 lead TSSOP	100 $^{\circ}$ C/W

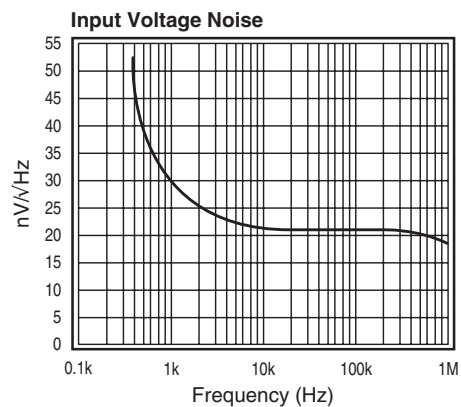
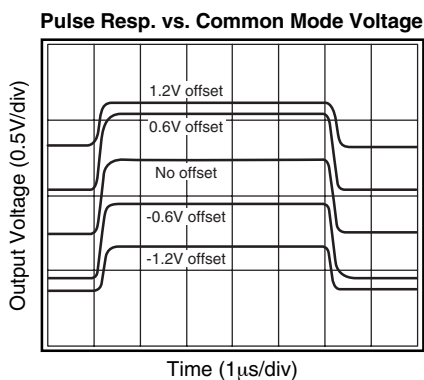
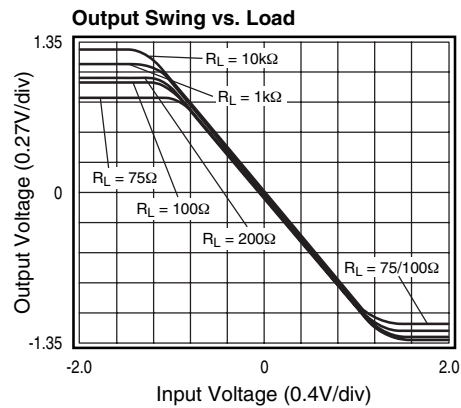
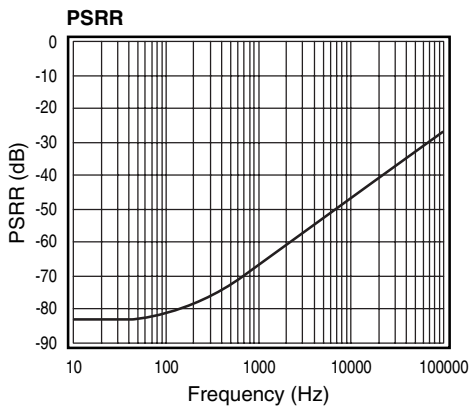
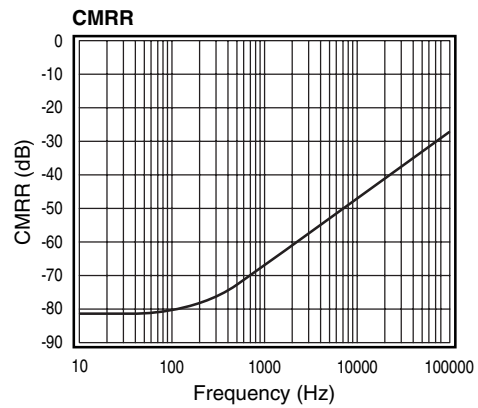
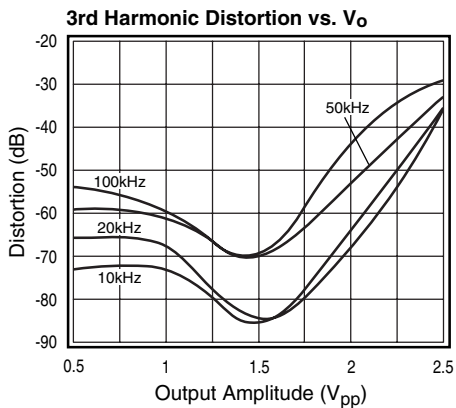
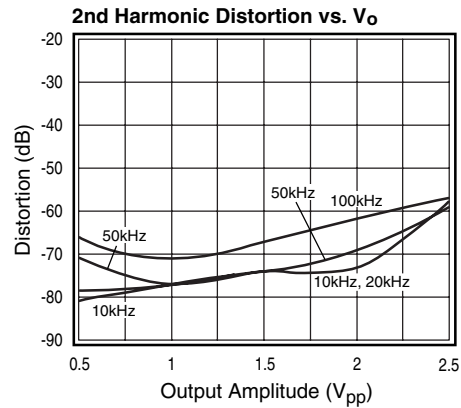
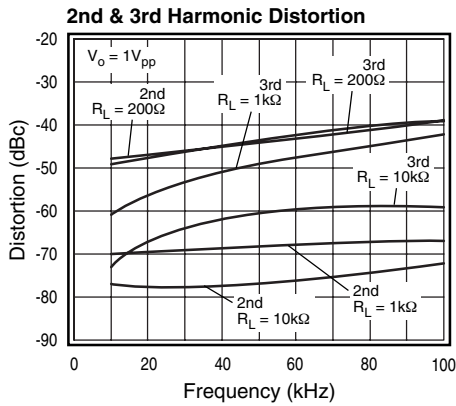
# Typical Operating Characteristics

( $V_S = +2.7V$ ,  $G = 2$ ,  $R_L = 10k\Omega$  to  $V_S/2$ ,  $R_f = 5k\Omega$ ; unless otherwise noted)



# Typical Operating Characteristics

( $V_S = +2.7V$ ,  $G = 2$ ,  $R_L = 10k\Omega$  to  $V_S/2$ ,  $R_f = 5k\Omega$ ; unless otherwise noted)



## Application Information

### General Description

The KM4X70 family of amplifiers are single supply, general purpose, voltage-feedback amplifiers. They are fabricated on a complementary bipolar process, feature a rail-to-rail input and output, and are unity gain stable.

The typical non-inverting circuit schematic is shown in Figure 1.

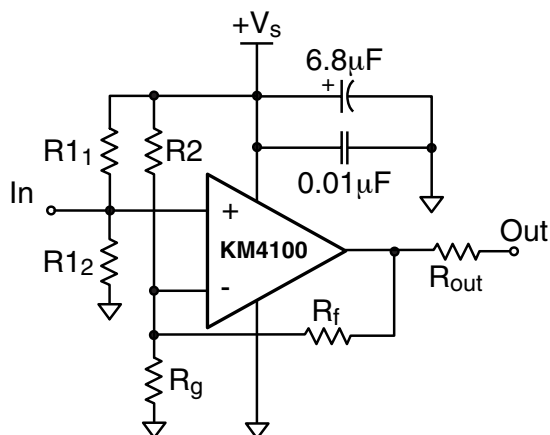


Figure 1: Typical Non-inverting Configuration

### Input Common Mode Voltage

The common mode input range extends to 250mV below ground and to 250mV above  $V_s$ , in single supply operation. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition. If the absolute maximum input voltage (700mV beyond either rail) is exceeded, externally limit the input current to  $\pm 5\text{mA}$  as shown in Figure 2.

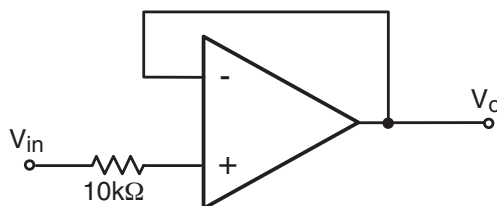


Figure 2: Circuit for Input Current Protection

### Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some performance degradation will occur. If the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

### Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The KM4X70 will typically recover in less than 50ns from an overdrive condition. Figure 3 shows the KM4X70 amplifier family in an overdriven condition.

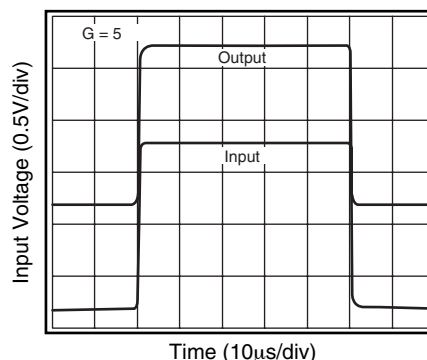


Figure 3: Overdrive Recovery

### Driving Capacitive Loads

The *Frequency Response vs.  $C_L$*  plot, illustrates the response of the KM4X70 amplifier family. A small series resistance ( $R_s$ ) at the output of the amplifier, illustrated in Figure 4, will improve stability and settling performance.  $R_s$  values in the *Frequency Response vs.  $C_L$*  plot were chosen to achieve maximum bandwidth with less than 2dB of peaking. For maximum flatness, use a larger  $R_s$ . Capacitive loads larger than 50pF require the use of  $R_s$ .

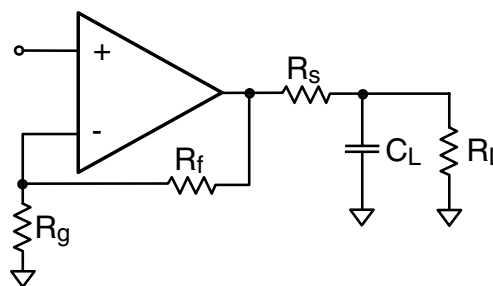


Figure 4: Typical Topology for driving a capacitive load

Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the KM4X70 amplifier family requires a 510Ω series resistor to drive a 100pF load.

### Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8 $\mu$ F and 0.01 $\mu$ F ceramic capacitors
- Place the 6.8 $\mu$ F capacitor within 0.75 inches of the power pin
- Place the 0.01 $\mu$ F capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 6 for more information.

When evaluating only one channel, complete the following on the unused channel:

1. Ground the non-inverting input
2. Short the output to the inverting input

### Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

Eval Bd	Description	Products
KEB002	Single Channel, Dual Supply, 5 and 6 lead SOT23	KM4170IT5
KEB011	Single Channel, Dual Supply, 5 and 6 lead SC70	KM4170IS5
KEB006	Dual Channel, Dual Supply, 8 lead SOIC	KM4270IC8
KEB010	Dual Channel, Dual Supply, 8 lead MSOP	KM4270IM8
KEB012	Quad Channel, Dual Supply, 14 lead TSSOP	KM4470IP14

Evaluation board schematics are shown in Figures 5a, 5b, 5c and layouts are shown in Figure 6a through Figure 6l.

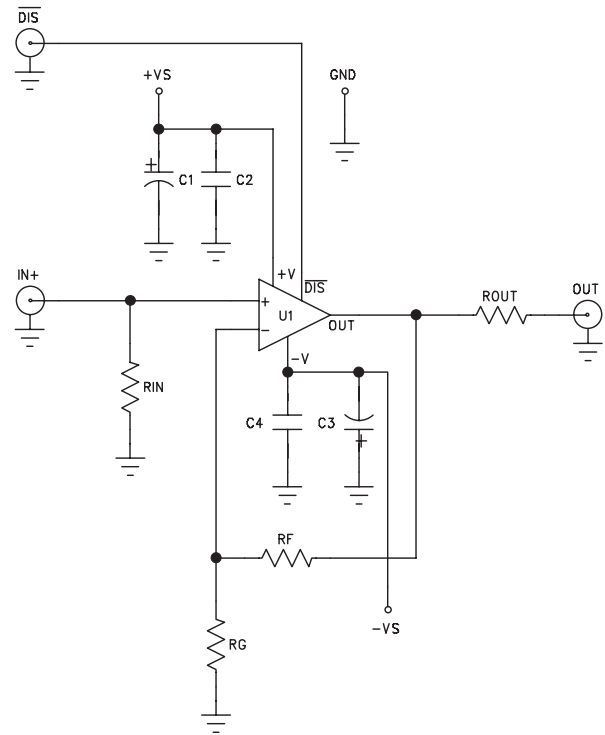


Figure 5a: KM4170 Evaluation Board Schematic

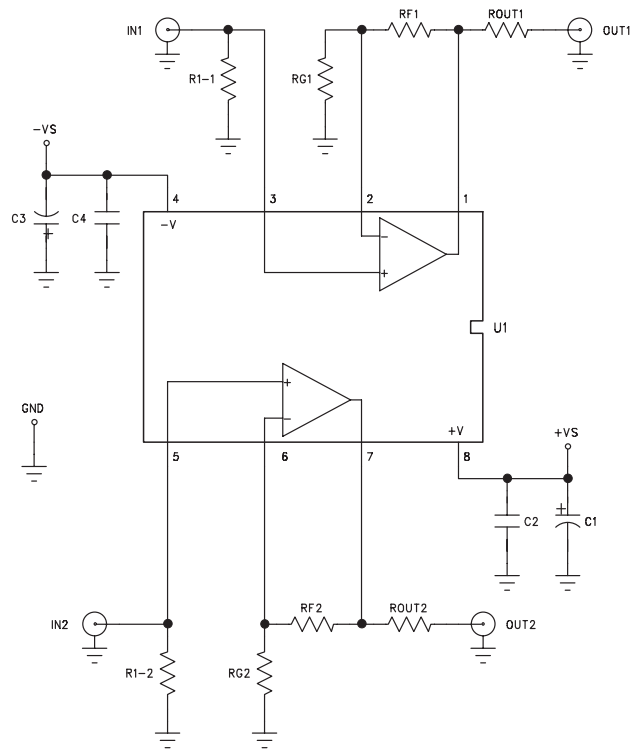


Figure 5b: KM4270 Evaluation Board Schematic



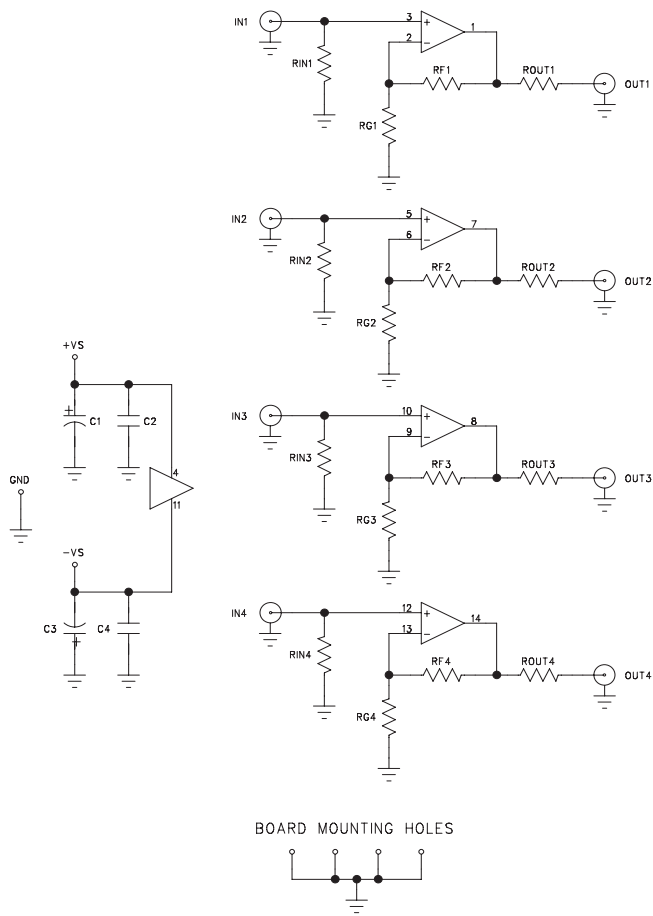


Figure 5c: KM4470 Evaluation Board Schematic

KM4170 Evaluation Board Layout

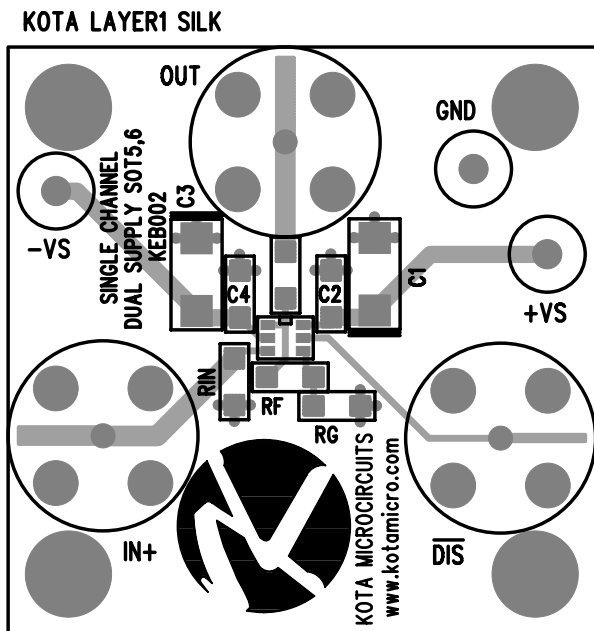


Figure 6a: KEB002 (top side)

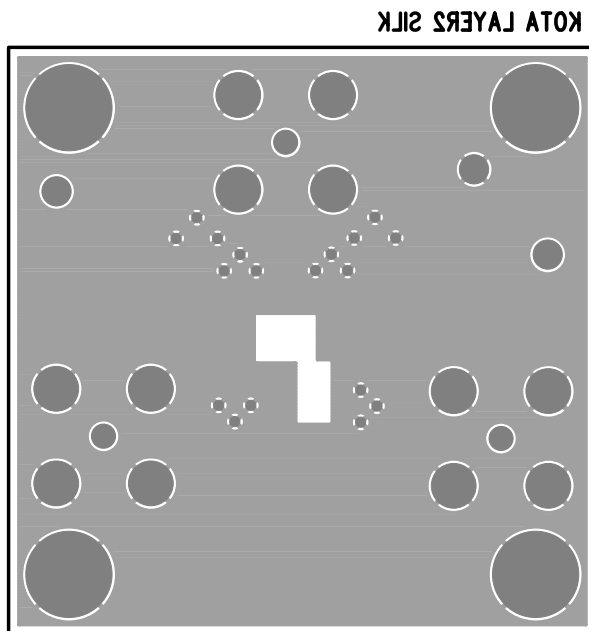


Figure 6b: KEB002 (bottom side)

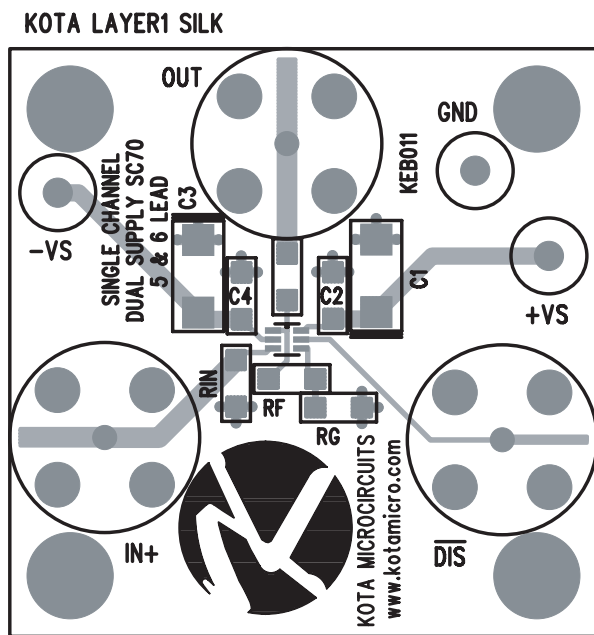


Figure 6c: KEB011 (top side)

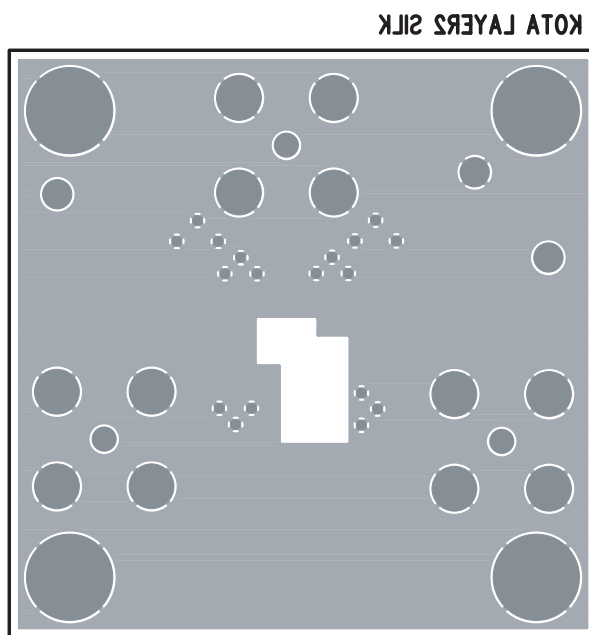


Figure 6d: KEB011 (bottom side)

### KM4270 Evaluation Board Layout

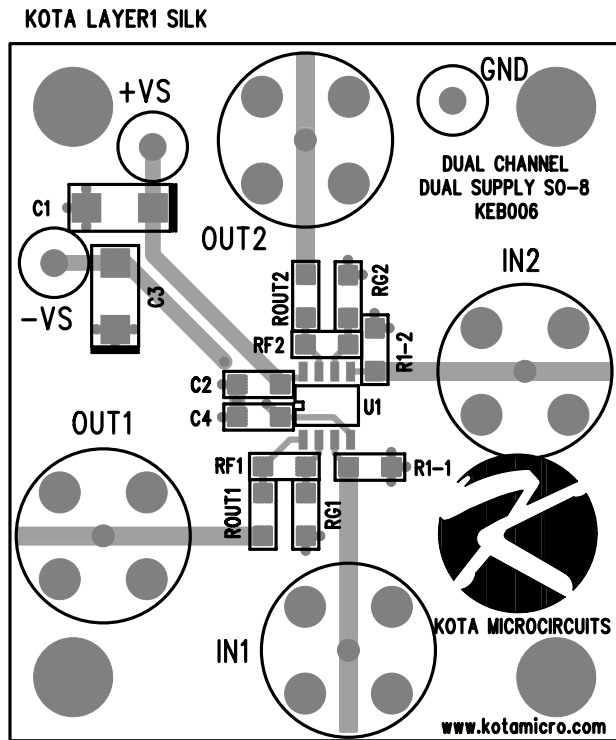


Figure 6e: KEB006 (top side)

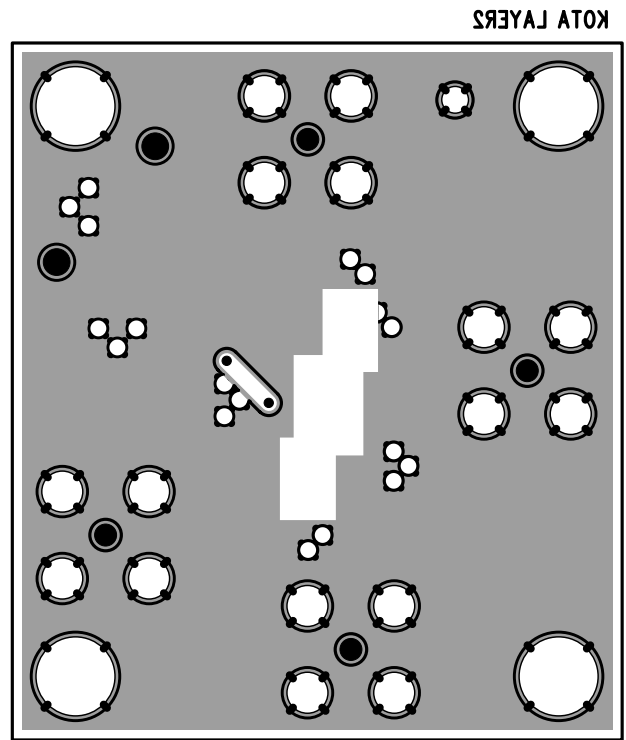


Figure 6f: KEB006 (bottom side)

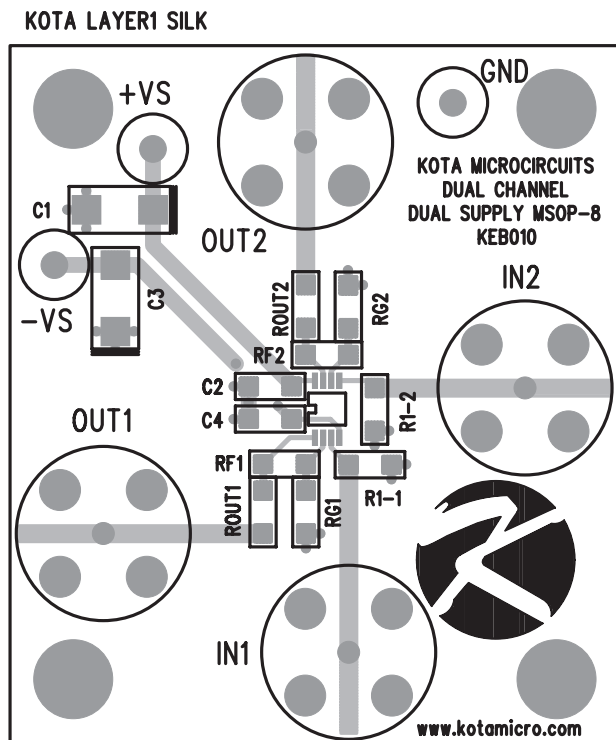


Figure 6g: KEB010 (top side)

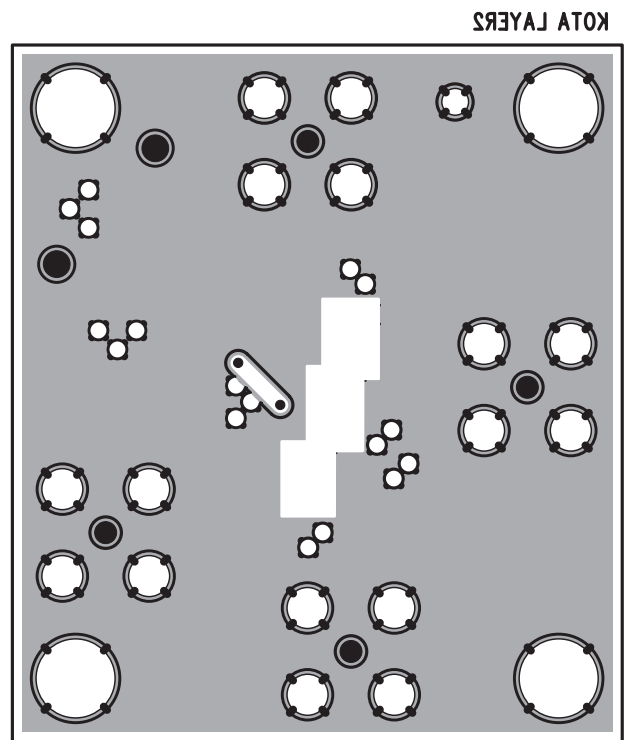


Figure 6h: KEB010 (bottom side)

### KM4470 Evaluation Board Layout

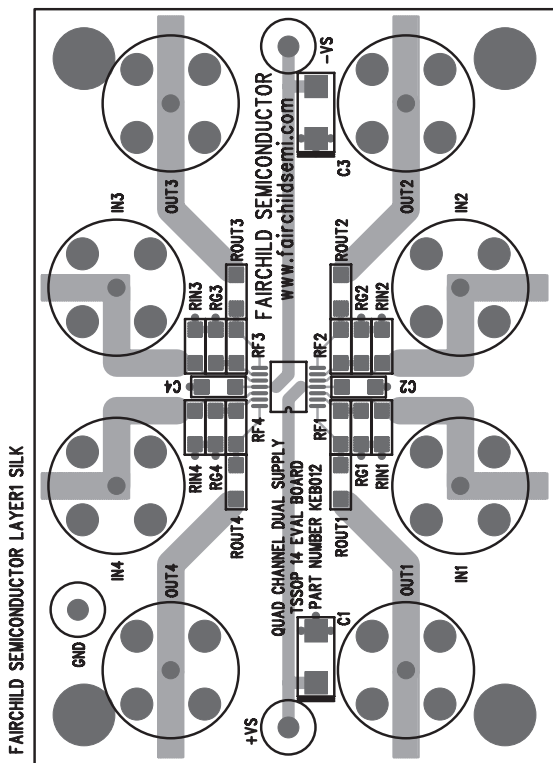


Figure 6i: KEB012 (top side)

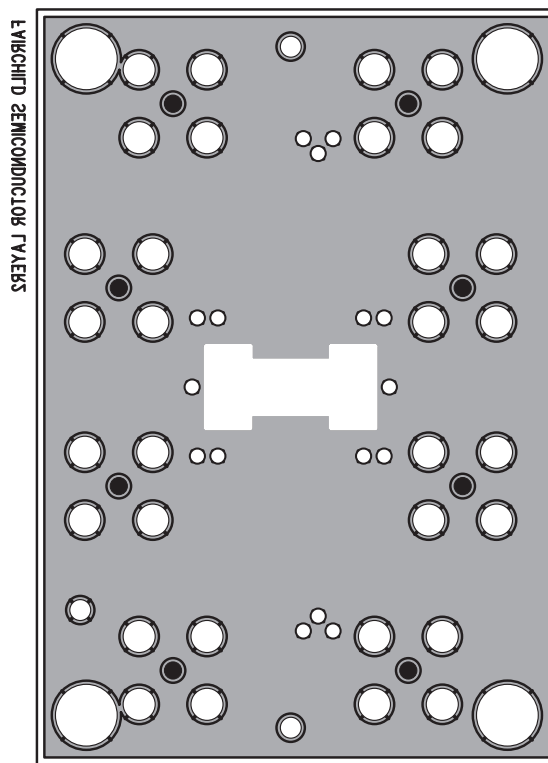


Figure 6j: KEB012 (bottom side)

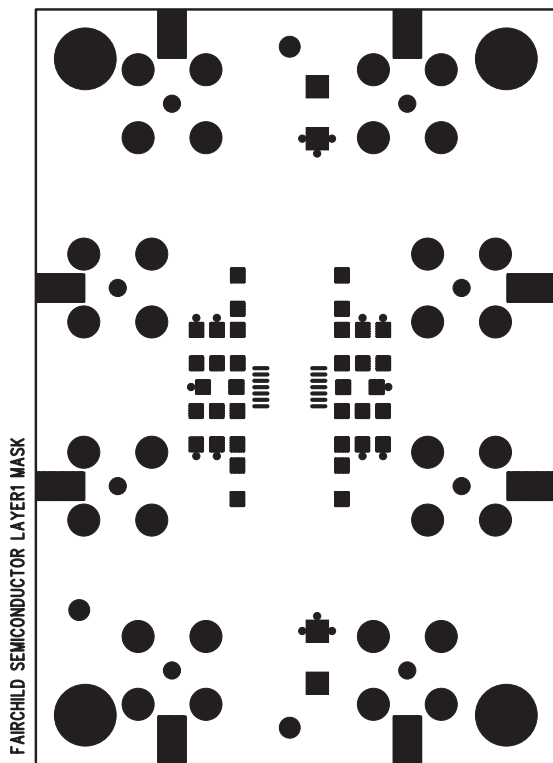


Figure 6k: KEB012 (layer1 mask)

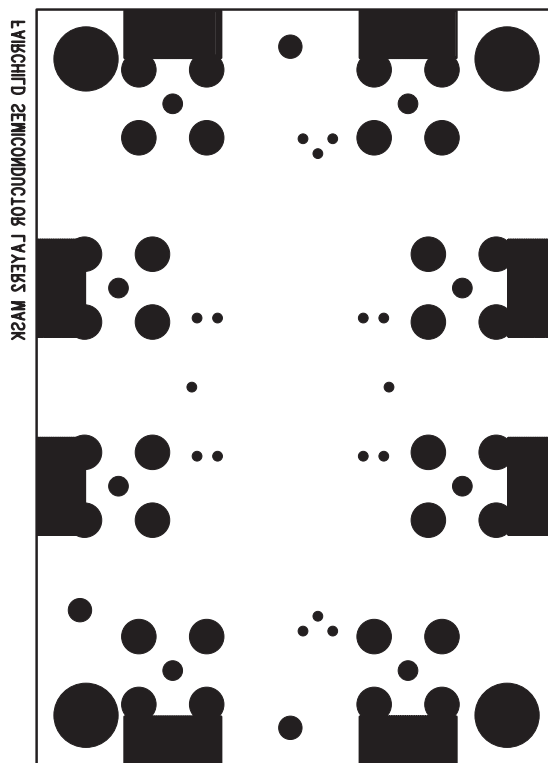
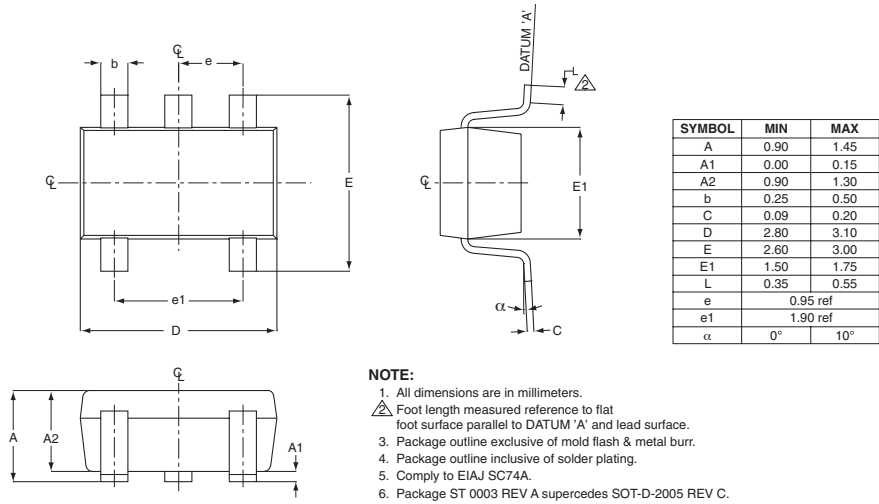


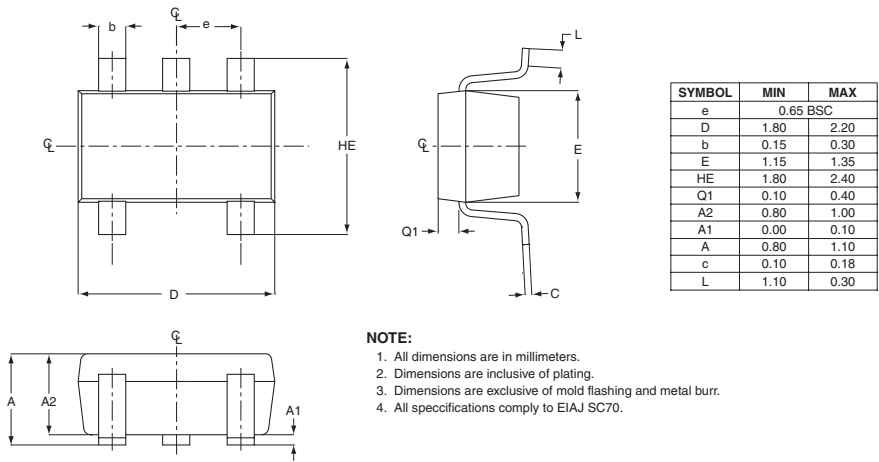
Figure 6l: KEB012 (layer2 mask)

# KM4170 Package Dimensions

## SOT23-5

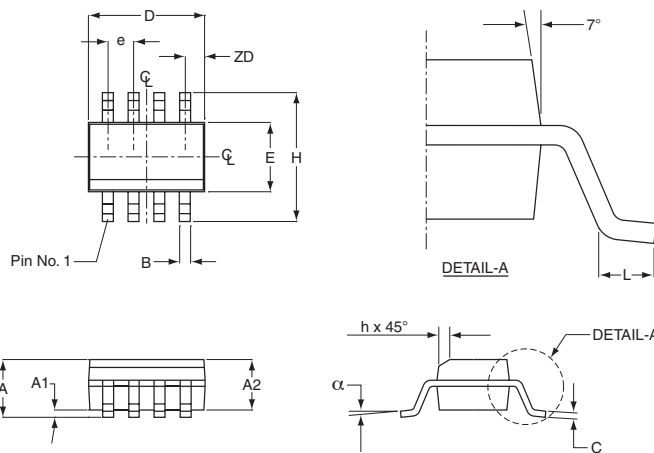


## SC70



# KM4270 Package Dimensions

## SOIC

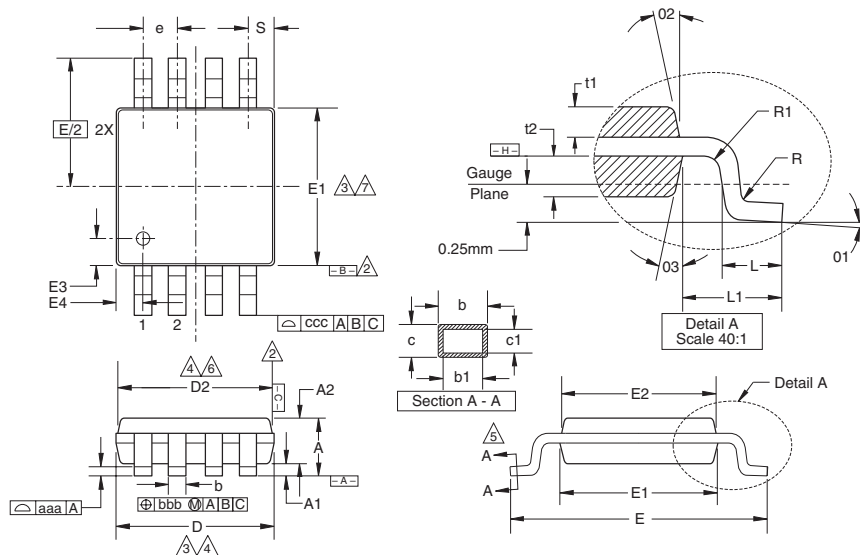


SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.53 ref	
A2	1.37	1.57

**NOTE:**

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:  
 (2.1) Top: matte (charmillies #18-30).  
 (2.2) All sides: matte (charmillies #18-30).  
 (2.3) Bottom: smooth or matte (charmillies #18-30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed 0.152mm (.006) per side(d).

## MSOP



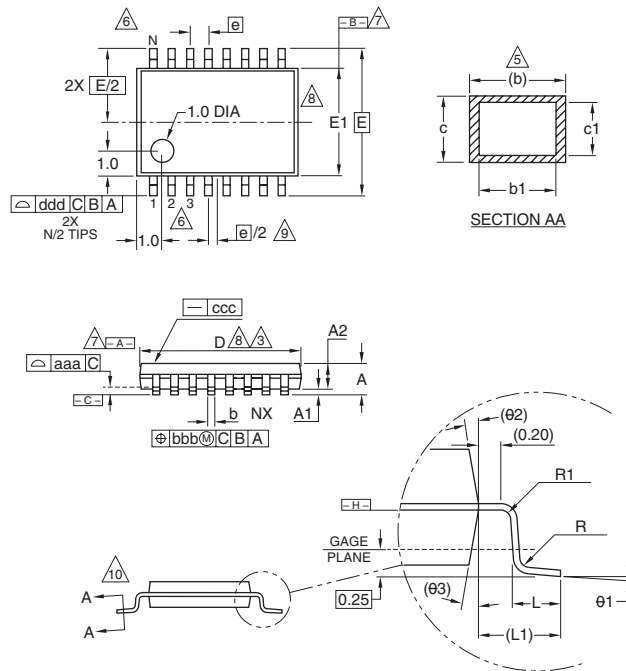
MSOP-8		
SYMBOL	MIN	MAX
A	1.10	-
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	+0.15/-0.06
R1	0.15	+0.15/-0.06
t1	0.31	±0.08
t2	0.41	±0.08
b	0.33	+0.07/-0.08
b1	0.30	±0.05
c	0.18	±0.05
c1	0.15	+0.03/-0.02
01	3.0°	±3.0°
02	12.0°	±3.0°
03	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	-
aaa	0.10	-
bbb	0.08	-
ccc	0.25	-
e	0.65 BSC	-
S	0.525 BSC	-

**NOTE:**

1. All dimensions are in millimeters (angle in degrees), unless otherwise specified.
- ▲ Datums  $\overline{B}$  and  $\overline{C}$  to be determined at datum plane  $\overline{H}$ .
- ▲ Dimensions "D" and "E1" are to be determined at datum  $\overline{H}$ .
- ▲ Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.
- ▲ Cross sections A - A to be determined at 0.13 to 0.25mm from the leadtip.
- ▲ Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.
- ▲ Dimension "E1" and "E2" does not include interlead flash or protrusion.

# KM4470 Package Dimensions

## TSSOP



TSSOP-14			
SYMBOL	MIN	NOM	MAX
A	-	-	1.10
A1	0.05	-	0.15
A2	0.85	0.90	0.95
L	0.50	0.60	0.75
R	0.09	-	-
R1	0.09	-	-
b	0.19	-	0.30
b1	0.19	0.22	0.25
c	0.09	-	0.20
c1	0.09	-	0.16
theta1	0°	-	8°
L1	1.0 REF		
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.20		
e	0.65 BSC		
theta2	12° REF		
theta3	12° REF		
D	4.90	5.00	5.10
E1	4.30	4.40	4.50
E	6.4 BSC		
e	0.65 BSC		
N	14		

### NOTES:

- All dimensions are in millimeters (angle in degrees).
- Dimensioning and tolerancing per ASME Y14.5-1994.
- Dimensions "D" does not include mold flash, protusions or gate burrs. Mold flash protusions or gate burrs shall not exceed 0.15 per side .
- Dimension "E1" does not include interlead flash or protusion. Interlead flash or protusion shall not exceed 0.25 per side.
- Dimension "b" does not include dambar protusion. Allowable dambar protusion shall be 0.08mm total in excess of the "b" dimension at maximum material condition. Dambar cannot be located on the lower radius of the foot. Minimum space between protusion and adjacent lead is 0.07mm for 0.5mm pitch packages.
- Terminal numbers are shown for reference only.
- Datums [A] and [B] to be determined at datum plane [H].
- Dimensions "D" and "E1" to be determined at datum plane [H].
- This dimensions applies only to variations with an even number of leads per side. For variation with an odd number of leads per side, the "center" lead must be coincident with the package centerline, Datum A.
- Cross sections A - A to be determined at 0.10 to 0.25mm from the leadtip.

## Ordering Information

Model	Part Number	Package	Container	Pack Qty
KM4170	KM4170IT5TR3	SOT23-5	Reel	3000
KM4170	KM4170IS5TR3	SC70-5	Reel	3000
KM4270	KM4270IC8TR3	SOIC-8	Reel	2500
KM4270	KM4270IM8TR3	MSOP-8	Reel	3000
KM4470	KM4470IP14TR3	TSSOP-14	Reel	2500

Temperature range for all parts: -40°C to +85°C.

---

### DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICES TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

### LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.