



May 2000

QFET™

FQS4903

500V Dual N-Channel MOSFET

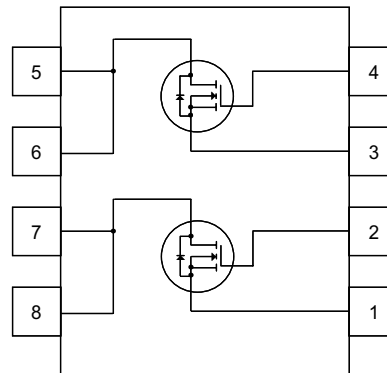
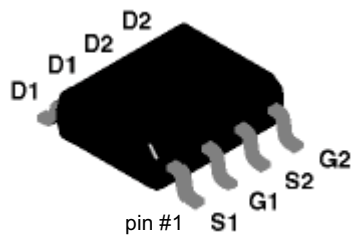
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- 0.37A, 500V, $R_{DS(on)} = 6.2\Omega @ V_{GS} = 10V$
- Low gate charge (typical 6.3 nC)
- Low Crss (typical 4.5 pF)
- Fast switching
- Improved dv/dt capability



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	FQS4903	Units
V _{DSS}	Drain-Source Voltage	500	V
I _D	Drain Current - Continuous (T _A = 25°C)	0.37	A
		0.234	A
I _{DM}	Drain Current - Pulsed (Note 1)	1.48	A
V _{GSS}	Gate-Source Voltage	± 25	V
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P _D	Power Dissipation (T _A = 25°C)	2.0	W
		1.3	W
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R _{θJA}	Thermal Resistance, Junction-to-Ambient	--	62.5	°C/W

Electrical Characteristics T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	500	--	--	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.49	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 400 V, T _C = 125°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 25 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -25 V, V _{DS} = 0 V	--	--	-100	nA

On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 0.185 A	--	4.7	6.2	Ω
g _{FS}	Forward Transconductance	V _{DS} = 35 V, I _D = 0.185 A (Note 3)	--	0.13	--	S

Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	155	200	pF
C _{oss}	Output Capacitance		--	25	35	pF
C _{rss}	Reverse Transfer Capacitance		--	4.5	6.0	pF

Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 0.37 A, R _G = 25 Ω (Note 3,4)	--	5.5	20	ns
t _r	Turn-On Rise Time		--	20	50	ns
t _{d(off)}	Turn-Off Delay Time		--	20	50	ns
t _f	Turn-Off Fall Time		--	45	100	ns
Q _g	Total Gate Charge	V _{DS} = 400 V, I _D = 0.37 A, V _{GS} = 10 V (Note 3,4)	--	6.3	8.2	nC
Q _{gs}	Gate-Source Charge		--	0.56	--	nC
Q _{gd}	Gate-Drain Charge		--	3.63	--	nC

Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current	--	--	0.37	A	
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current	--	--	1.48	A	
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 0.37 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 0.37 A, di _F / dt = 100 A/μs (Note 3)	--	100	--	ns
Q _{rr}	Reverse Recovery Charge		--	0.175	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. I_{SD} ≤ 0.37A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
3. I_{SD} ≤ 0.37A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

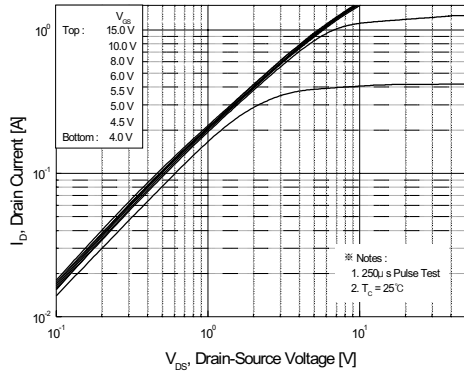


Figure 1. On-Region Characteristics

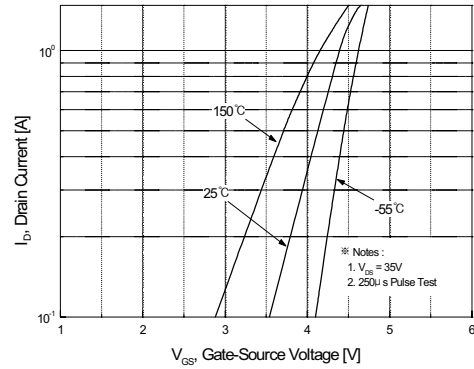


Figure 2. Transfer Characteristics

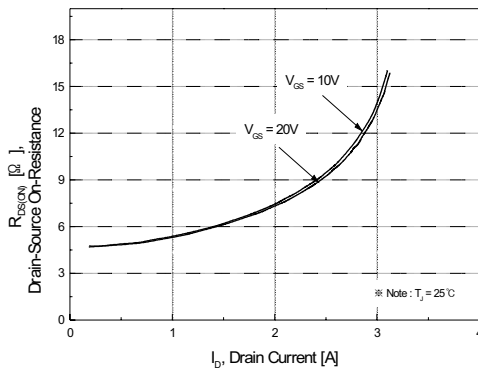


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

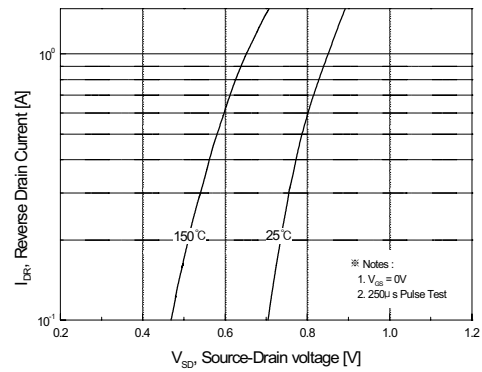


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

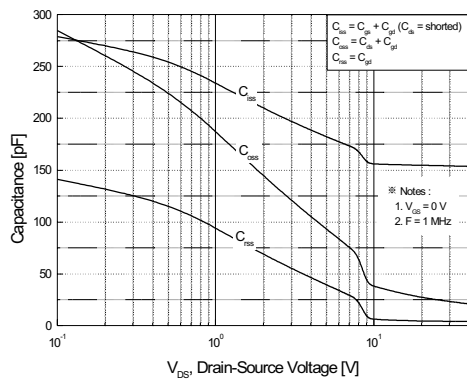


Figure 5. Capacitance Characteristics

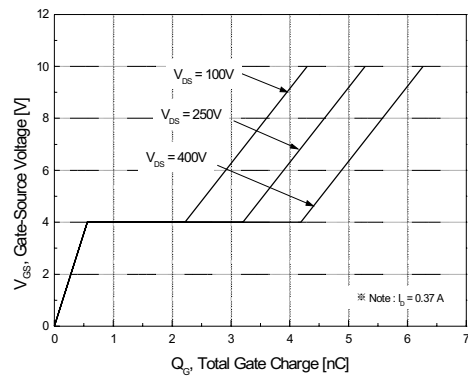


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

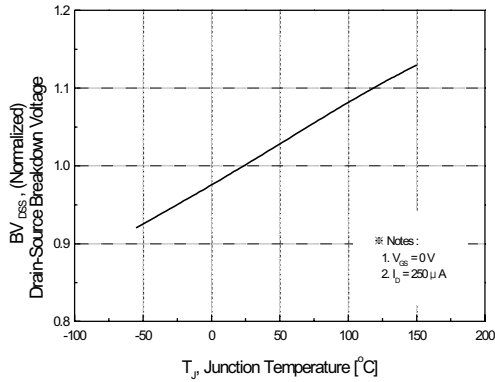


Figure 7. Breakdown Voltage Variation vs. Temperature

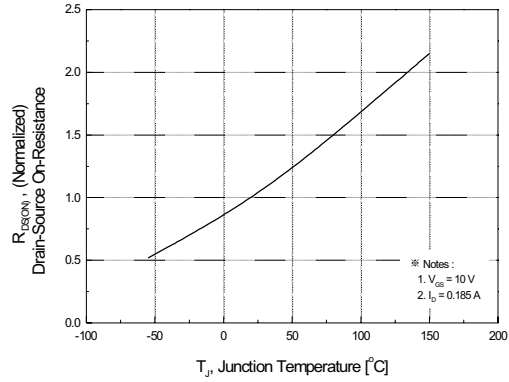


Figure 8. On-Resistance Variation vs. Temperature

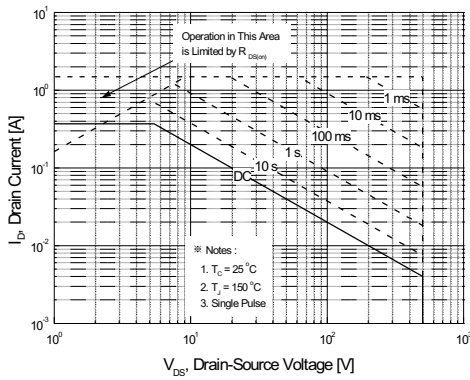


Figure 9. Maximum Safe Operating Area

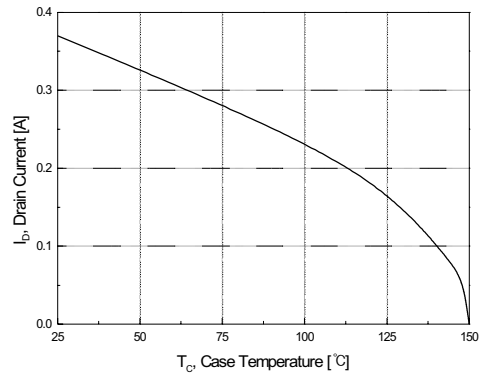


Figure 10. Maximum Drain Current vs. Case Temperature

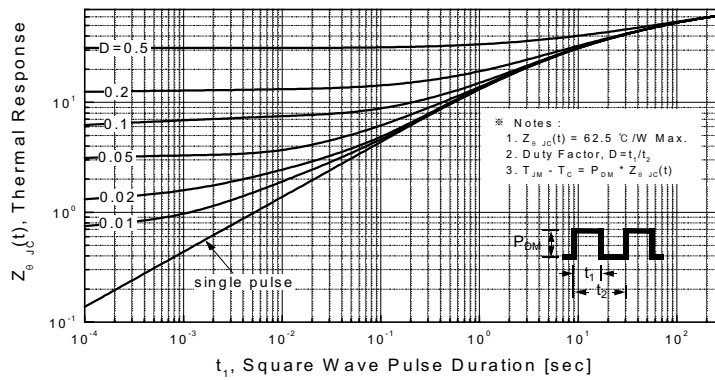
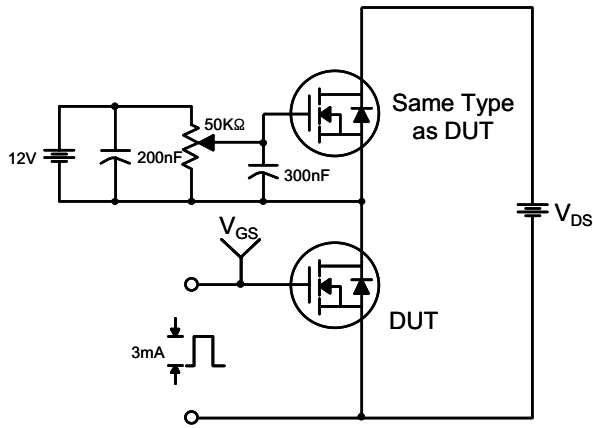


Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

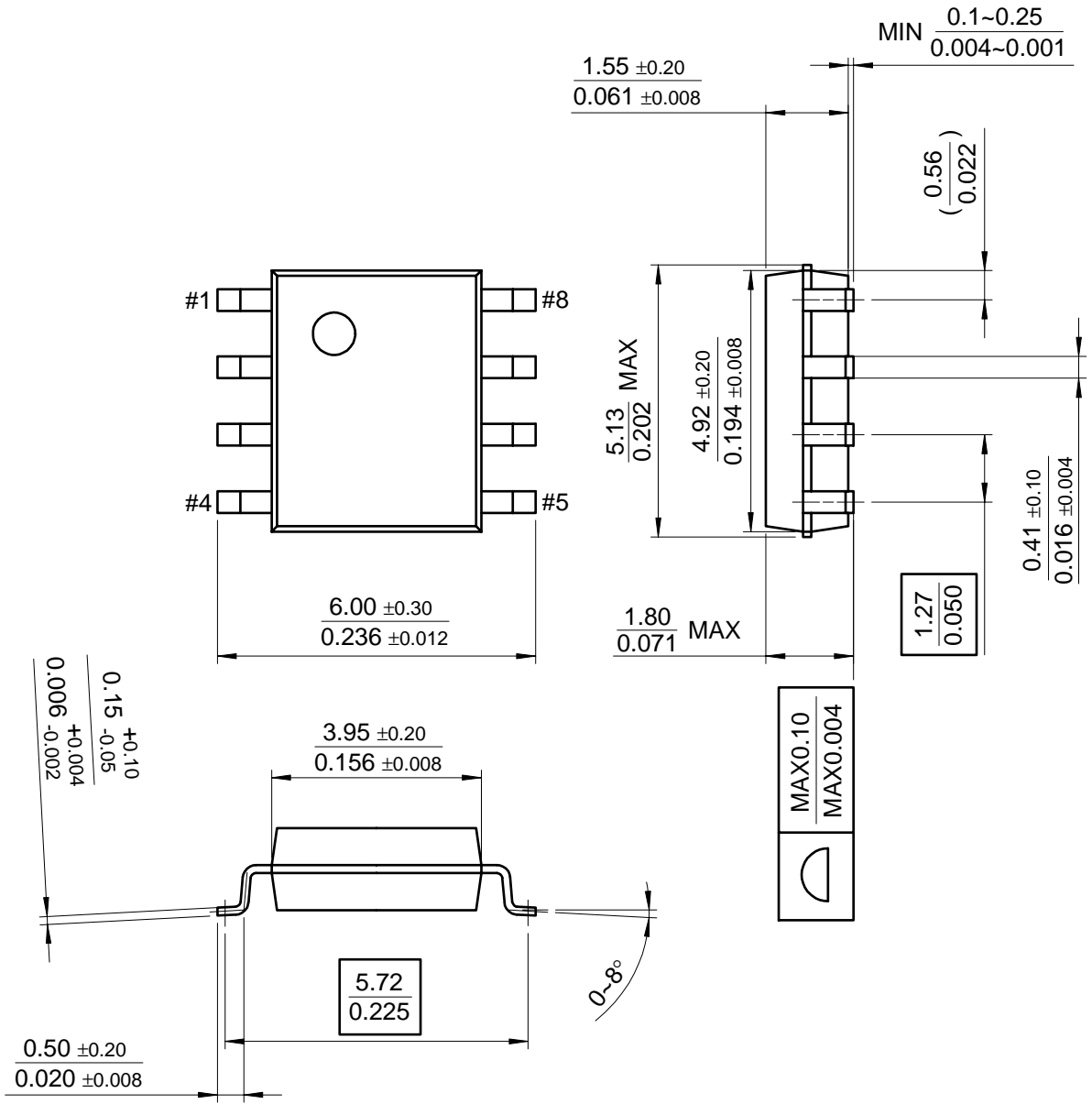


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

8SOP



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