FAIRCHILD SEMICONDUCTOR®

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FIN24
μSerDes™
Low Voltage 24-Bit Bi-Directional Serializer/Deserializer (Preliminary)

General Description

The FIN24 allows for a pair of SerDes to interleave data from two different data sources going opposite directions or standard bi-directional interface operation. The bi-directional data flow is controlled through use of a direction (DIRI) control terminal. The devices can be configured to operate in a unidirectional mode by only hardwiring the DIRI terminal. An option for 2 or 4 unidirectional control terminals can be selected by using the S1 and S2 mode control terminals. An Internal PLL generates the required bit clock frequency for transfer across the serial link. Options exist for dual or single PLL operation dependent upon system operational parameters. The device has been designed for low power operation and utilizes Fairchild Low Power LVDS interface. The device also supports an ultra low power Power-Down mode for conserving power in battery operated applications.

Features

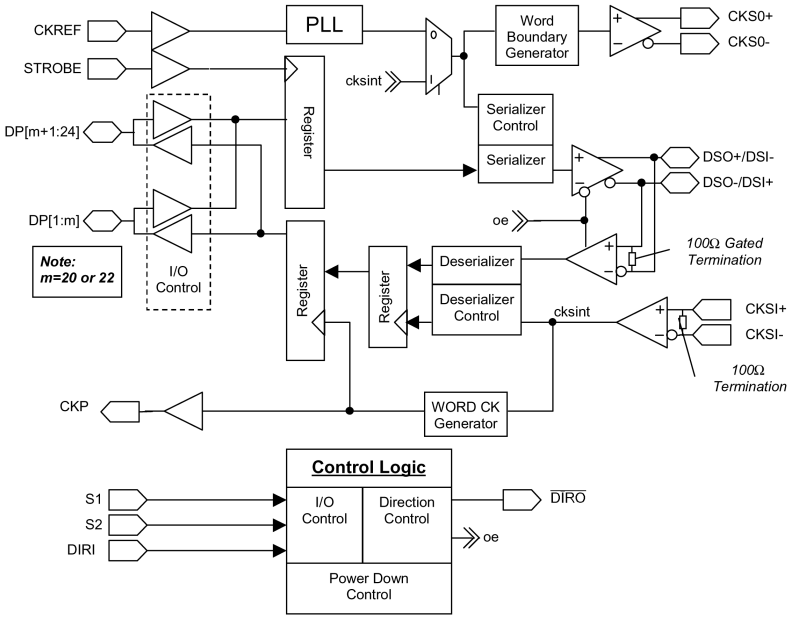
- Low power consumption
- Low power standards based LVDS differential interface
- LVCMOS parallel I/O interface
  - 2 mA source/sink current
  - Over-voltage tolerant control signals
- I/O Power Supply range between 1.65V and 3.6V
- Analog Power Supply range of 2.775V ± 5%
- Multi-Mode operation allows for a single device to operate as Serializer or Deserializer
- Internal PLL with no external components
- Standby Power-Down mode support
- Built in differential termination
- Selectable unidirectional control terminals
- Serialized data rate up to 780Mb/s
- Small footprint 40-terminal MLP packaging

Ordering Code:

Order Number	Package Number	Package Description
FIN24GFX (Preliminary)	BGA42A	Pb-Free 42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide
FIN24MLX	MLP040A	Pb-Free 40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square

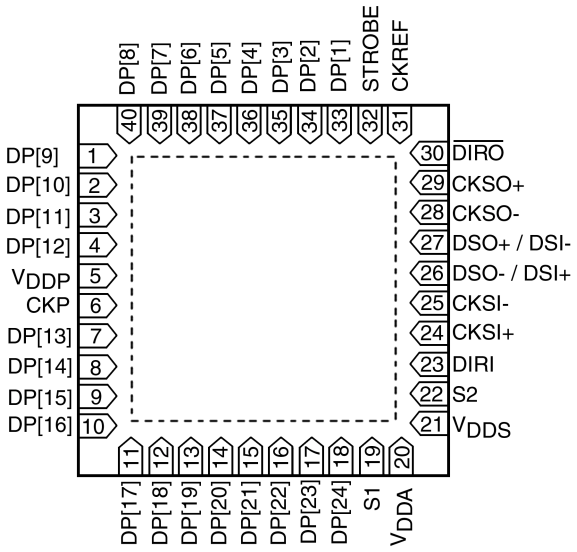
Pb-Free package per JEDEC J-STD-020B.
BGA and MLP packages available in Tape and Reel only.

Functional Block Diagram



Connection Diagram

Terminal Assignments for MLP



(Top View)

Terminal Description

Terminal Name	I/O Type	Number of Terminals	Description of Signals
DP[1:20]	I/O	20	LVCMOS Parallel I/O. Direction controlled by DIRI Terminal
DP[21:24]	I or O	4	LVCMOS Parallel Unidirectional Inputs or Outputs Dependent on State of S1, S2 Terminals
CKREF	IN	1	LVCMOS Clock Input and PLL Reference
STROBE	IN	1	LVCMOS Strobe Signal for Latching Data into the Serializer
CKP	OUT	1	LVCMOS Word Clock Output
DSO+ / DSI– DSO– / DSI+	DIFF-I/O	2	LpLVDS Differential Serial I/O Data Signals (Note 1) DSO: Refers to output signal pair DSO(I)+: Positive signal of DSO(I) pair DSI: Refers to input signal pair DSO(I)–: Negative signal of DSO(I) pair
CKSI+, SKSI–	DIFF-IN	2	LpLVDS Differential Deserializer Input Bit Clock CKSI: Refers to signal pair CKSI+: Positive signal of CKSI pair CKSI–: Negative signal of CKSI pair
CKSO+, SKSO–	DIFF-OUT	2	LpLVDS Differential Serializer Output Bit Clock CKSO: Refers to signal pair CKSO+: Positive signal of CKSO pair CKSO–: Negative signal of CKSO pair
S1	IN	1	LVCMOS Mode Selection Pins used to define mode of operation for some terminals. The control terminals, DP[21:24] can be set as 4 terminals in the same direction or two in each direction.
S2	IN	1	
DIRI	IN	1	LVCMOS Control Input Used to control direction of Data Flow
$\overline{\text{DIRO}}$	OUT	1	LVCMOS Control Output Inversion of DIRI
V_{DDP}	Supply	1	Power Supply for Parallel I/O and Translation Circuitry
V_{DDS}	Supply	1	Power supply for core circuitry and serial I/O
V_{DDA}	Supply	1	Power Supply for Analog PLL Circuitry
GND	Supply	0	Use Bottom Ground Plane for Ground Signals

Note 1: The DSO/DSI serial port terminals have been arranged such that when one device is rotated 180 degrees wrt the other device the serial connections will properly align without the need for any traces or cable signals to cross. Other layout orientations may require that traces or cables cross.

Control Logic Circuitry

The FIN24 has 4 signals that are selectable as 2 unidirectional inputs and 2 unidirectional outputs, or as 4 unidirectional inputs or 4 unidirectional outputs. These are often used by applications for control signals. The mode signals S1 and S2 determine the direction of the DP[21:24] data signals. The 00 state also provides for a power-down state where all functionality of the device is disabled or reset. The DIRI terminal controls whether the device is a serializer or deserializer. When DIRI is asserted LOW, the device is configured as a 24-bit deserializer. When the DIRI terminal is asserted HIGH, the device will be configured as a 24-bit serializer. Changing the state on the DIRI signal will reverse the direction of the I/O signals and generate the opposite state signal on $\overline{\text{DIRO}}$. For unidirectional operation the DIRI terminal should be hardwired to the HIGH or LOW state and the $\overline{\text{DIRO}}$ terminal should be left floating. For bidirectional operation the DIRI of the master device will be driven by the system and the $\overline{\text{DIRO}}$ signal of the master will be used to drive the DIRI of the slave device.

When a device with dedicated data outputs turns from a deserializer to a serializer the dedicated outputs will remain at the last logical value asserted. This value will only change if the device is once again turned around into a deserializer and the values are overwritten.

When operating the SerDes in pairs, not all operating modes are compatible. Regardless of the mode of operation the serializer is always sending 24 bits of data and 2 word boundary bits. The deserializer is always receiving 24 bits of data and 2 word boundary bits. For some modes of operation not all of the data bits are valid due to some pins being dedicated inputs or outputs. A value of “0” will be sent for all invalid data bits.

4-Bit Control Mode: When operating in 4-bit control mode the master device must be configured as MODE 2. (S2 = 1, S1 = 0) and the slave device must be configured as MODE 1 (S2 = 0, S1 = 1). When operating in this mode 24 data and control bits can be sent from the master to the slave and 20 data bits can be sent from the slave to the master. Unidirectional control signals should be connected to DP[21:24].

2-Bit Control Mode: When operating in 2-bit control mode both devices must be configured in MODE 3 (S2 = S1 = “1”). In this mode of operation 22 bits can be sent in either direction. When operating in a 2-bit control mode serialized bits 21 and 22 will appear on outputs 23 and 24 of the deserializer.

TABLE 1. Control Logic Circuitry

Mode Number	S2	S1	DIRI	Description
0	0	0	x	Power-Down State. The device will be powered down and disabled regardless of all other signals.
1	0	1	0	4-Bit Unidirectional Control Mode Device operating as a Deserializer DP[21:24] are outputs
	0	1	1	4-Bit Unidirectional Control Mode Device operating as a Serializer DP[21:24] are outputs
2	1	0	0	4-Bit Unidirectional Control Mode Device operating as a Deserializer DP[21:24] are inputs
	1	0	1	4-Bit Unidirectional Control Mode Device operating as a Serializer DP[21:24] are inputs
3	1	1	0	2-Bit Unidirectional Control Mode, Deserializer DP[21:22] are inputs DP[23:24] outputs
	1	1	1	Unidirectional Control Mode, Serializer DP[21:22] are inputs DP[23:24] outputs

Power-Down Mode: (Mode 0)

Mode 0 is used for powering down and resetting the device. When both of the mode signals are driven to a LOW state the PLL and references will be disabled, differential input buffers will be shut off, differential output buffers will be placed into a HIGH Impedance state, LVCMOS outputs will be placed into a HIGH Impedance state and LVCMOS inputs will be driven to a valid level internally. Additionally all internal circuitry will be reset. The loss of CKREF state is also enabled to insure that the PLL will only power-up if there is a valid CKREF signal.

In a typical application the device will only change between the power-down mode and the selected mode of operation. This allows for system level power-down functionality to be implemented via a single wire for a SerDes pair. The S1 and S2 selection signals that have their operating mode driven to a “logic 0” should be hardwired to GND. The S1 and S2 signals that have their operating mode driven to a “logic 1” should be connected to a system level power-down signal.

Serializer Operation

The serializer configuration is described in the following sections. The basic serialization circuitry works essentially identical in these modes but the actual data and clock streams will differ dependent on if CKREF is the same as the STROBE signal or not. When it is stated that CKREF equals STROBE this means that the CKREF and STROBE signals are hardwired together as one signal. When it is stated that CKREF does not equal STROBE then each signal is distinct and CKREF must be running at a frequency high enough to avoid any loss of data condition. CKREF must never be a lower frequency than STROBE.

Serializer Operation: (Figure 1)
DIRI equals 1
CKREF equals STROBE

The PLL must receive a stable CKREF signal in order to achieve lock prior to any valid data being sent. The CKREF signal can be used as the data STROBE signal provided that data can be ignored during the PLL lock phase.

Once the PLL is stable and locked the device can begin to capture and serialize data. Data will be captured on the rising edge of the STROBE signal and then serialized. The serialized data stream is synchronized and sent source synchronously with a bit clock with an embedded word boundary. Serialized data is sent at 26 times the CKREF clock rate. Two additional data bits are sent that define the word boundary. When operating in this mode the internal deserializer circuitry is disabled including the serial clock, serial data input buffers, the bidirectional parallel outputs and the CKP word clock. The CKP word clock will be driven HIGH.

Serializer Operation: (Figure 2)
DIRI equals 1
CKREF does not equal STROBE

If the same signal is not used for CKREF and STROBE, then the CKREF signal must be run at a higher frequency than the STROBE rate in order to serialize the data correctly. The actual serial transfer rate will remain at 26 times the CKREF frequency. A data bit value of zero will be sent when no valid data is present in the serial bit stream. The operation of the serializer will otherwise remain the same.

The exact frequency that the reference clock needs to run at will be dependent upon the stability of the CKREF and STROBE signal. If the source of the CKREF signal implements spread spectrum technology then the maximum frequency of this spread spectrum clock should be used in calculating the ratio of STROBE frequency to the CKREF frequency. Similarly if the STROBE signal has significant cycle-to-cycle variation then the maximum cycle-to-cycle time needs to be factored into the selection of the CKREF frequency.

Serializer Operation: (Figure 3)
DIRI equals 1
No CKREF

A third method of serialization can be done by providing a free running bit clock on the CKSI signal. This mode is enabled by grounding the CKREF signal and driving the DIRI signal HIGH.

At power-up the device is configured to accept a serialization clock from CKSI. If a CKREF is received then the device will enable the CKREF serialization mode. The device will remain in this mode even if CKREF is stopped. To re-enable this mode the device must be powered down and then powered back up with “logic 0” on CKREF.

Serializer Operation (Continued)

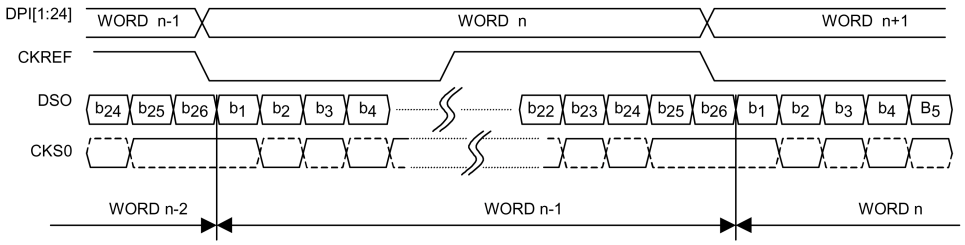


FIGURE 1. Serializer Timing Diagram (CKREF equals STROBE)

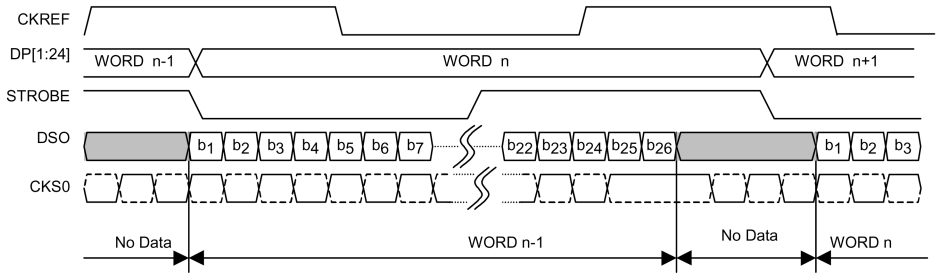


FIGURE 2. Serializer Timing Diagram (CKREF does not equal STROBE)

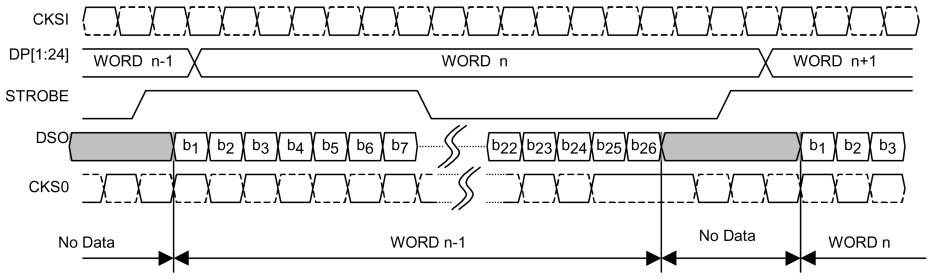


FIGURE 3. Serializer Timing Diagram Using Provided Bit Clock (No CKREF)

Deserializer Operation Mode

The operation of the deserializer is only dependent upon the data received on the DSI data signal pair and the CKSI clock signal pair. The following two sections describe the operation of the deserializer under two distinct serializer source conditions. References to the CKREF and STROBE signals refer to the signals associated with the serializer device used in generating the serial data and clock signals that are inputs to the deserializer.

When operating in this mode the internal serializer circuitry is disabled including the parallel data input buffers. If there is a CKREF signal provided then the CKSO serial clock will continue to transmit bit clocks.

Deserializer Operation:
DIRI equals 0
(Serializer Source: CKREF equals STROBE)

When the DIRI signal is asserted LOW the device will be configured as a deserializer. Data will be captured on the serial port and deserialized through use of the bit clock sent with the data. The word boundary is defined in the actual clock and data signal. Parallel data will be generated at the time the word boundary is detected. The falling edge of CKP will occur approximately 6 bit times after the next falling edge of CKSI. The rising edge of CKP will go HIGH approximately 13 bit times after CKP goes LOW. When no embedded word boundary occurs then no pulse on CKP will be generated and CKP will remain HIGH.

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Deserializer Operation:
DIRI equals 0
(Serializer Source: CKREF does not equal STROBE)

The logical operation of the deserializer remains the same regardless of if the CKREF is equal in frequency to the STROBE or at a higher frequency than the STROBE. The actual serial data stream presented to the deserializer will however be different because it will have non-valid data bits sent between words. The duty cycle of CKP will vary based on the ratio of the frequency of the CKREF signal to the STROBE signal. The frequency of the CKP signal will be equal to the STROBE frequency. The falling edge of CKP will occur 6 bit times after the data transition. The LOW time of the CKP signal will be equal to ½ (13 bit times) of the CKREF period. The CKP HIGH time will be equal to STROBE period –½ of the CKREF period. Figure 5 is representative of a waveform that could be seen when CKREF is not equal to STROBE. If CKREF was significantly faster then additional non-valid data bits would occur between data words.

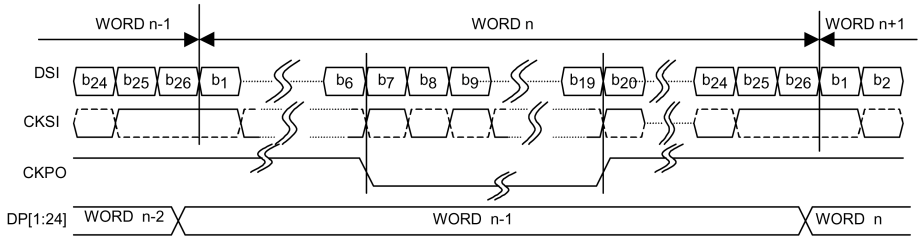


FIGURE 4. Deserializer Timing Diagram
(Serializer Source: CKREF equals STROBE)

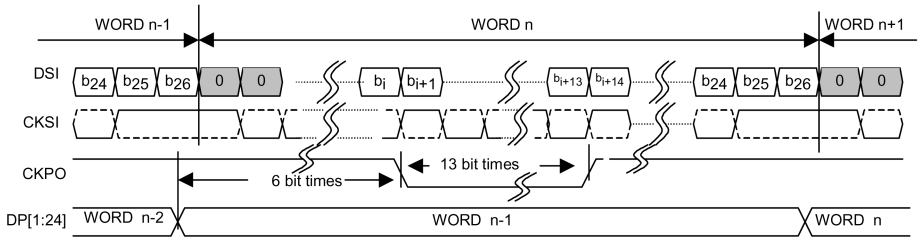


FIGURE 5. Deserializer Timing Diagram
(Serializer Source: CKREF does not equal STROBE)

Embedded Word Clock Operation

The FIN24 sends and receives serial data source synchronously with a bit clock. The bit clock has been modified to create a word boundary at the end of each data word. The word boundary has been implemented by skipping a LOW clock pulse. This appears in the serial clock stream as three consecutive bit times where signal CKSO remains HIGH.

In order to implement this sort of scheme two extra data bits are required. During the word boundary phase the data will toggle either HIGH-then-LOW or LOW-then-HIGH dependent upon the last bit of the actual data word. Table 2 provides some examples showing the actual data word and the data word with the word boundary bits added. Note that a 24-bit word will be extended to 26 bits during serial transmission. Bit 25 and Bit 26 are defined with-respect-to Bit 24. Bit 25 will always be the inverse of Bit 24 and Bit 26 will always be the same as Bit 24. This insures that a "0" → "1" and a "1" → "0" transition will always occur during the embedded word phase where CKSO is HIGH.

The serializer generates the word boundary data bits and the boundary clock condition and embeds them into the serial data stream. The deserializer looks for the end of the word boundary condition to capture and transfer the data to the parallel port. The deserializer only uses the embedded word boundary information to find and capture the data. These boundary bits are then stripped prior to the word being sent out of the parallel port.

TABLE 2. Word Boundary Data Bits

24-Bit Data Words		24-Bit Data Word with Word Boundary	
Hex	**Binary**	**Hex**	**Binary**
FFFFFFh	1111 1111 1111 1111 1111 1111b	2FFFFFFh	10 1111 1111 1111 1111 1111 1111b
555555h	0101 0101 0101 0101 01010 0101b	1555555h	01 0101 0101 0101 0101 0101 0101b
xxxxxxh	0xxx xxxx xxxx xxxx xxxx xxxxb	1xxxxxxh	01 0xxx xxxx xxxx xxxx xxxx xxxxb
xxxxxxh	1xxx xxxx xxxx xxxx xxxx xxxxb	2xxxxxxh	10 1xxx xxxx xxxx xxxx xxxx xxxxb

LVCMOS Data I/O (Figure 6)

The LVCMOS input buffers have a nominal threshold value equal to ½ of V_{DDP}. The input buffers are only operational when the device is operating as a serializer. When the device is operating as a deserializer the inputs are gated off to conserve power.

The LVCMOS 3-STATE output buffers are rated for a source/sink current of 2mAs at 1.8V. The outputs are active when the DIRI signal is asserted LOW. When the DIRI signal is asserted HIGH the bi-directional LVCMOS I/Os will be in a HIGH-Z state. Under purely capacitive load conditions the output will swing between GND and V_{DDP}.

The LVCMOS I/O buffers incorporate bushold functionality to allow for terminals to maintain state when they are not driven. The bushold circuitry only consumes power during signal transitions.

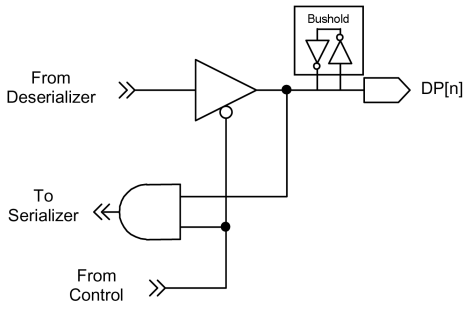


FIGURE 6. LVCMOS I/O

Differential I/O Circuitry (Figure 7)

The differential I/O circuitry is a low power variant of LVDS. The differential outputs operate in the same fashion as LVDS by sourcing and sinking a balanced current through the output pair. Like LVDS an input source termination resistor is required to develop a voltage at the differential input pair. The FIN24 device incorporates an internal termination resistor on the CKSI receiver and a gated internal termination resistor on the DS input receiver. The gated termination resistor insures proper termination regardless of direction of data flow.

During power-down mode the differential inputs will be disabled and powered down and the differential outputs will be placed in a HIGH-Z state.

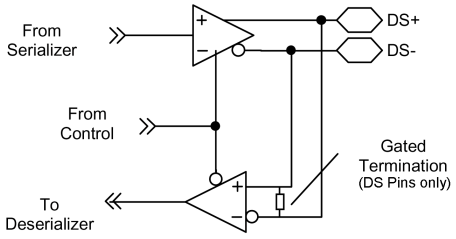


FIGURE 7. Bidirectional Differential I/O Circuitry

PLL Circuitry

The CKREF input signal is used to provide a reference to the PLL. The PLL will generate internal timing signals capable of transferring data at 26 times the incoming CKREF signal. The output of the PLL is a Bit Clock that is sent with the serial data stream.

There are two ways to disable the PLL. The PLL can be disabled by entering the Mode 0 state (S1 = S2 = 0). The PLL will disable immediately upon detecting a LOW on both the S1 and S2 signals. Any of the other modes are entered by asserting either S1 or S2 HIGH and by providing a CKREF signal the PLL will power-up and go through a lock sequence. One must wait the specified number of clock cycles prior to capturing valid data into the parallel port.

An alternate way of powering down the PLL is by stopping the CKREF signal either HIGH or LOW. Internal circuitry detects the lack of transitions and shuts the PLL and serial I/O down. Internal references will not however be disabled allowing for the PLL to power-up and re-lock in a lesser number of clock cycles than when exiting Mode 0. When a transition is seen on the CKREF signal the PLL will once again be reactivated.

Application Mode Diagrams

MODE equals 3: Unidirectional Data Transfer

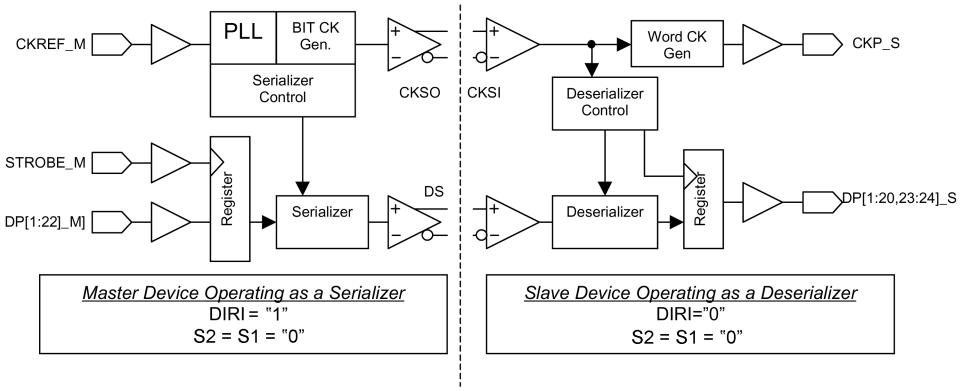


FIGURE 8. Simplified Block Diagram for Unidirectional Serializer and Deserializer

Figure 8 shows the basic operation diagram when a pair of SerDes is configured in an unidirectional operation mode.

Master Operation: The device will...
(Please refer to Figure 8)

1. During power-up the device will be configured as a serializer based on the value of the DIRI signal.
2. Accept CKREF_M word clock and generate a bit clock with embedded word boundary. This bit clock will be sent to the slave device through the CKSO port.
3. Receive parallel data on the rising edge of STROBE_M.
4. Generate and transmit serialized data on the DS signals which is source synchronous with CKSO.
5. Generate an embedded word clock for each strobe signal.

Slave Operation: The device will...

1. Be configured as a deserializer at power-up based on the value of the DIRI signal.
2. Accept an embedded word boundary bit clock on CKSI.
3. Deserialize the DS Data stream using the CKSI input clock.
4. Write parallel data onto the DP_S port and generate the CKP_S. CKP_S will only be generated when a valid data word occurs.

Application Mode Diagrams (Continued)

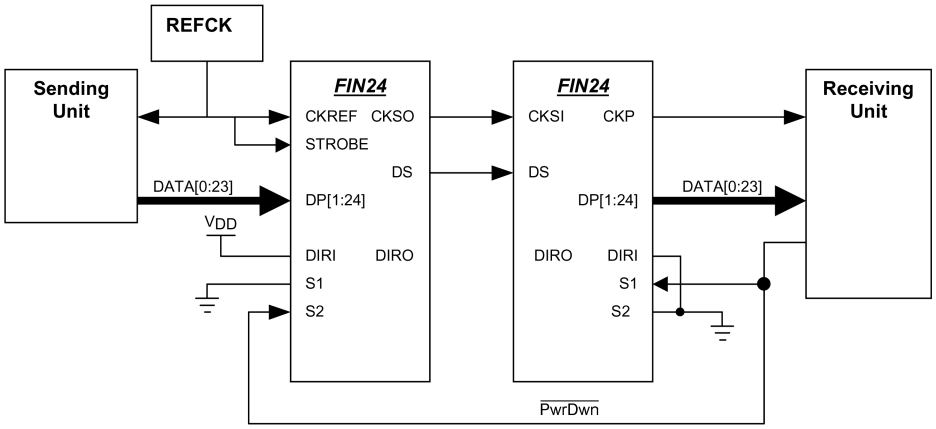


FIGURE 9. 24-Bit Unidirectional Serializer and Deserializer

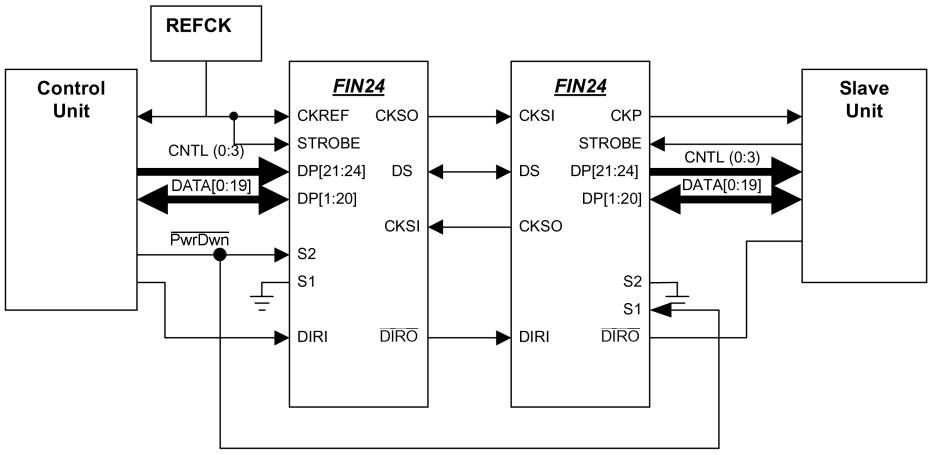


FIGURE 10. Unidirectional Control, Bidirectional Data Interface

Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{DDP})	−0.5V to +4.6V
ALL Input/Output Voltage	−0.5V to +4.6V
LVDS Output Short Circuit Duration	Continuous
Storage Temperature Range (T_{STG})	−65°C to +150°C
Maximum Junction Temperature (T_J)	+150°C
Lead Temperature (T_L)	
(Soldering, 4 seconds)	+260°C
ESD Rating	
Human Body Model, 1.5KΩ, 100pF	>2kV
Machine Model, 0Ω, 200pF	>200V

Recommended Operating Conditions

Supply Voltage (V_{DDA}, V_{DDS})	2.775V ± 5.0%V
Supply Voltage (V_{DDP})	1.65V to 3.6V
Operating Temperature (T_A) (Note 2)	−10°C to + 70°C
Supply Noise Voltage (V_{DDA-PP})	100 mV_{P-P}

Note 2: Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

DC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ (Note 3)	Max	Unit
LVCMOS I/O							
V_{IH}	Input High Voltage			0.65 x V_{DDP}		V_{DDP}	
V_{IL}	Input Low Voltage			GND		0.35 x V_{DDP}	V
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	V_{DDP} = 3.3 ± 0.3	0.75 x V_{DDP}			V
			V_{DDP} = 2.5 ± 0.2				
			V_{DDP} = 1.8 ± 0.15				
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA	V_{DDP} = 3.3 ± 0.3			0.25 x V_{DDP}	V
			V_{DDP} = 2.5 ± 0.2				
			V_{DDP} = 1.8 ± 0.15				
I_{IN}	Input Current	V_{IN} = 0V to 3.6V		−5.0		5.0	µA
$I_{I(Hold)}$	Minimum Bushold Currents	V_{DDP} = 3.0, V_{IN} = 1.95 or 1.05		±35.0			uA
		V_{DDP} = 2.3, V_{IN} = 1.495 or 0.805		±25.0			
		V_{DDP} = 1.65, V_{IN} = 1.07 or 0.58		±10.0			
$I_{I(OD)}$	Minimum Required Bushold Overdrive Current	V_{DDP} = 3.6, V_{IN} = 2.34 or 1.26		±200			uA
		V_{DDP} = 2.7, V_{IN} = 1.76 or 0.945		±150			
		V_{DDP} = 1.95, V_{IN} = 1.268 or 0.682		±75.0			
I_{OFF}	Input/Output Power-Off Leakage Current	V_{DDP} = 0V, V_{DDS} = 0V; V_{DDA} = 0V ALL LVCMOS Inputs/ Outputs 0V to 3.6V				±5.0	µA
DIFFERENTIAL I/O							
V_{OD}	Output Differential Voltage	R_L = 100 Ω, See Figure 11		150	225	350	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW-to-HIGH	R_L = 100 Ω, See Figure 11				15.0	mV
V_{OS}	Offset Voltage	R_L = 100 Ω, See Figure 11	V_{DDS} = 2.775 ± 5%		925		mV
ΔV_{OS}	Offset Magnitude Change from Differential LOW-to-HIGH					15.0	mV
I_{OS}	Short Circuit Output Current (Note 4)	V_{OUT} = 0V	Driver Enabled		−2.5	−5.0	mA
			Driver Disabled			±5.0	µA
I_{OZ}	Disabled Output Leakage Current	DP = 0V to V_{DDP}, DIRI = V_{DDP}			±1.0	±10.0	µA
V_{TH}	Differential Input Threshold HIGH	See Figure 12 and Table 2		100			mV
V_{TL}	Differential Input Threshold LOW	See Figure 12 and Table 2				−100	mV
V_{ICM}	Input Common Mode Range	V_{DDS} = 2.775 ± 5%		300	925	1550	mV
R_{TRM0}	CKSI Internal Receiver Termination Resistor	V_{ID} = 225 mV, V_{IC} = 925 mV, DIRI = 0 $\lvert CKSI^+ - CKSI^-\rvert = V_{ID}$		80.0	100	120	Ω
R_{TRM1}	DS Internal I/O Termination Resistor	V_{ID} = 225 mV, V_{IC} = 925 mV, DIRI = 0 $\lvert DS^+ - DSI^-\rvert = V_{ID}$		80.0	100	120	Ω

DC Electrical Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min	Typ (Note 3)	Max	Unit
I_{IN}	Input Current	$V_{IN} = V_{DDP} + 0.3V$ or 0V $V_{DDP} = 0V$ or 3.6V			±20.0	μA

Note 3: Typical Values are given for $V_{DDP} = 2.5V$ and $T_A = 25°C$. Positive current values refer to the current flowing into device and negative values means current flowing out of pins. Voltage are referenced to Ground unless otherwise specified (except ΔV_{OD} and V_{OD}).

Note 4: The definition of short-circuit includes all the possible situations. For example, the short of differential pairs to ground, the short of differential pairs (No Grounding) and either line of differential pairs tied to Ground.

Power Supply Currents

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
I_{DDA1}	V_{DDA} Serializer Static Supply Current	All DPI and Control Inputs at 0V or V_{DDP}, NO CKREF, S2 = 0, S1 =, DIRI = 1			TBD	TBD	mA
I_{DDA2}	V_{DDA} Deserializer Static Supply Current	All DPI and Control Inputs at 0 or V_{DDP}, NO CKREF, S2 = 0, S1 =, DIRI = 1			TBD	TBD	mA
I_{DDS1}	V_{DDS} Serializer Static Supply Current	All DPI and Control Inputs at 0V or V_{DDP}, NO CKREF, S2 = 0, S1 = 1, DIRI = 1			TBD	TBD	mA
	V_{DDS} Deserializer Static Supply Current	All DPI and Control Inputs at 0V or V_{DDP}, NO CKREF, S2 = 0, S1 = 1, DIRI = 0			TBD	TBD	
I_{DD_PD}	V_{DD} Power-Down Supply Current $I_{DD\_PD} = I_{DDA} + I_{DDS} + I_{DDP}$	S1 = S2 = 0, All Inputs at GND or V_{DDP}				5.0	uA
I_{DD_SER1}	26:1 Dynamic Serializer Power Supply Current $I_{DD\_SER1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = H See Figure 13	10MHz		TBD	TBD	mA
			30MHz		TBD	TBD	
I_{DD_DES1}	1:26 Dynamic Deserializer Power Supply Current $I_{DD\_SER1} = I_{DDA} + I_{DDS} + I_{DDP}$	CKREF = STROBE DIRI = L See Figure 13	10MHz		TBD	TBD	mA
			30MHz		TBD	TBD	
I_{DD_SER2}	26:1 Dynamic Serializer Power Supply Current $I_{DD\_SER2} = I_{DDA} + I_{DDS} + I_{DDP}$	NO CKREF, STROBE Active CKSI = 15x Strobe Rate DIRI = H (see Figure 13)	10 MHz		TBD	TBD	mA
			30 MHz		TBD	TBD	

AC Electrical Characteristics

Over supply voltage and operating temperature ranges, unless otherwise specified.

Symbol	Parameter	Test Conditions		Min	Typ	Max	Units
Serializer Electrical Characteristics							
t_{TCP}	CKREF Clock Period (10MHz - 30MHz)	See Figure 17		33.33	T	100	ns
t_{CPWH}	CKREF Clock HIGH Time			TBD	0.5	TBD	T
t_{CPWL}	CKREF Clock LOW Time			TBD	0.5	TBD	T
t_{CLKT}	LVCMOS Input Transition Time	See Figure 17				1.0	ns
t_{SPWH}	STROBE Pulse Width HIGH	See Figure 17				5.0	ns
t_{SPWL}	STROBE Pulse Width LOW	See Figure 17				5.0	ns
f_{MAX}	Maximum Serial Data Rate	REFCK x 26		260		780	Mb/s
f_{REF}	CKREF Frequency Relative	CKREF	S2 = 0 S1 = 1			5.0	
	to Strobe Frequency	does not equal	S2 = 1 S1 = 0	1.1 * f_{ST}		15.0	MHz
		STROBE	S2 = 1 S1 = 1			30.0	
Serializer AC Electrical Characteristics							
t_{TLH}	Differential Output Rise Time (20% to 80%)	See Figure 14			0.6	0.9	ns
t_{THL}	Differential Output Fall Time (80% to 20%)				0.6	0.9	ns
t_{STC}	DP[n] Setup to STROBE	DIRI = 1		2.5			ns
t_{HTC}	DP[n] Hold to STROBE	See Figure 16 (f = 10MHz)		0			ns
t_{TCCD}	Transmitter Clock Input to Clock Output Delay	See Figure 20, DIRI = 1, CKREF = STROBE		TBD	TBD	TBD	
t_{SPOS}	CKSO Position Relative to DS	See Figure 23, (Note 5) CKREF Serialization Mode		TBD	TBD	TBD	
	CKSO Position Relative to DS	See Figure 23, (Note 5) No CKREF Serialization Mode		TBD	TBD	TBD	
PLL AC Electrical Characteristics Specifications							
t_{JCC}	CKSO Clock Out Jitter (Cycle-to-Cycle)	(Note 6)			TBD		ns
t_{TPLLS0}	Serializer Phase Lock Loop Stabilization Time	See Figure 19				1000	Cycles
t_{TPLLD0}	PLL Disable Time. Loss of Clock	See Figure 24, (Note 7)		3.0		10.0	us
t_{TPLLD1}	PLL Power-Down Time	See Figure 25				20.0	ns
Deserializer AC Electrical Characteristics							
t_{S_DS}	Serial Port Setup Time, DS to CKSI	See Figure 22 (Note 8)		500			ps
t_{H_DS}	Serial Port Hold Time, DS to CKSI	See Figure 22 (Note 8)		500			ps
t_{RCOP}	Deserializer Clock Output (CKP OUT) Period	See Figure 18		50.0	T	200	ns
t_{RCOL}	CKP OUT Low Time	See Figure 18 (Rising Edge Strobe) Serializer Source STROBE = CKREF Where a = 1/f/26 (Note 9)		13a-3		13a+3	ns
t_{RCOH}	CKP OUT High Time			13a-3		13a+3	ns
t_{PDV}	Data Valid to CKP LOW	See Figure 18 (Rising Edge Strobe) Where a = 1/f/26 (Note 9)		6a-3	6a	6a+3	ns
t_{ROLH}	Output Rise Time (20% to 80%)	C_L = 8 pF			2.5	5.0	ns
t_{ROHL}	Output Fall Time (80% to 20%)	See Figure 15			2.5	5.0	ns

Note 5: Skew is measured from either the rising or falling edge of the clock (CKSO) relative to the center of the data bit (DS). Both outputs should have identical load conditions for this to be valid.

Note 6: This jitter specification is based on the assumption that PLL has a REF Clock with cycle-to-cycle input jitter less than 2% of the data period. PLL should be able to track a CKREF that varies up to 2% of the nominal clock period.

Note 7: The power-down time is a function of the CKREF frequency prior to CKREF being stopped HIGH or LOW. The device will power-down approximately n-clock periods after the CKREF signal is stopped either HIGH or LOW.

Note 8: Signals are transmitted from the serializer source synchronously. Note that in some cases data is transmitted when the clock remains at a high state. Setup and hold time measurements can only be measured during the valid data phase and not during the embedded word clock phase.

Note 9: Rising edge of CKP will appear approximately 13 bit times after the falling edge of the CKP output. Falling edge of CKP will occur approximately 6 bit times after a data transition. Variation with respect to the CKP signal is due to internal propagation delays of the device. Note that if CKREF is not equal to STROBE for the serializer the CKP signal will not maintain a 50% Duty Cycle. The low time of CKP will remain 13 bit times.

Control Logic Timing Controls

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
t_{PHL_DIR}, t_{PLH_DIR}	Propagation Delay DIRI-to-$\overline{DIRO}$	DIRI LOW-to-HIGH or HIGH-to-LOW			10.0	ns
t_{PLZ}, t_{PHZ}	Propagation Delay DIRI-to-DP	DIRI LOW-to-HIGH			7.0	ns
t_{PZL}, t_{PZH}	Propagation Delay DIRI-to-DP	DIRI HIGH-to-LOW			10.0	ns
t_{PLZ}, t_{PHZ}	Deserializer Disable Time: S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 27			7.0	ns
t_{PZL}, t_{PZH}	Deserializer Enable Time: S0 or S1 to DP	DIRI = 0, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 27			10.0	ns
t_{PLZ}, t_{PHZ}	Serializer Disable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = HIGH-to-LOW Figure 25			7.0	ns
t_{PZL}, t_{PZH}	Serializer Enable Time: S0 or S1 to CKSO, DS	DIRI = 1, S1(2) = 0 and S2(1) = LOW-to-HIGH Figure 25			10.0	ns

Capacitance

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
C_{IN}	Capacitance of Input Only Signals, CKREF, STROBE, S1, S2, DIRI	DIRI = 1, S1 = 0, V_{DDP} = 2.5V		TBD		pF
C_{IO}	Capacitance of Parallel Port Pins DP[1:12]	DIRI = 1, S1 = 0, V_{DDP} = 2.5V		TBD		pF
$C_{IO-DIFF}$	Capacitance of Differential I/O Signals	DIRI = 0, $\overline{PwnDwn}$ = 0; S1 = 0, V_{DDP} = 2.5V		TBD		pF

AC Loading and Waveforms

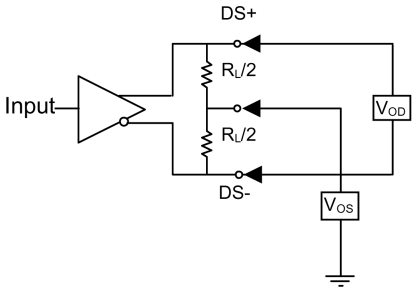
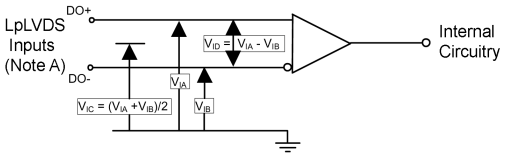
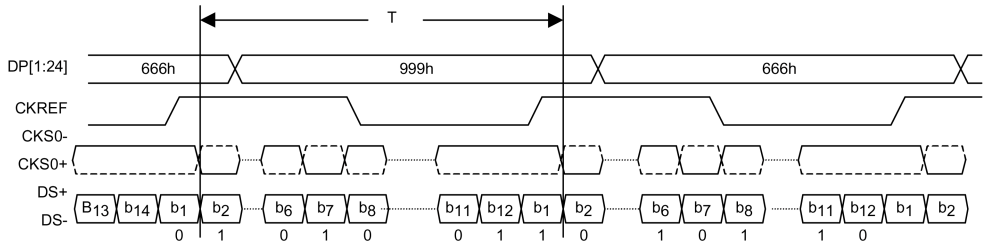


FIGURE 11. Differential LpLVDS Output DC Test Circuit



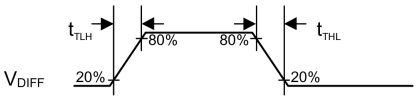
Note A: For All input pulses, t_R or t_F <= 1 ns

FIGURE 12. Differential Receiver Voltage Definitions



Note: The Worst Case test pattern produces a maximum toggling of internal digital circuits, LpLVDS I/O and LVCMOS I/O with the PLL operating at the reference frequency unless otherwise specified. Maximum power is measured at the maximum V_{DD} values. Minimum values are measured at the minimum V_{DD} values. Typical values are measured at V_{DD} = 2.5V.

FIGURE 13. "Worst Case" Serializer Test Pattern



V_{DIFF} = (DS+) – (DS-)

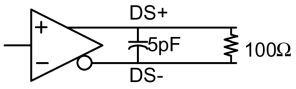
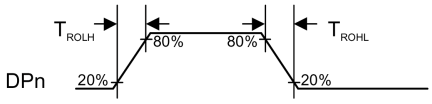


FIGURE 14. LpLVDS Output Load and Transition Times



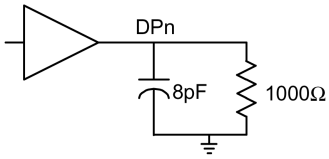
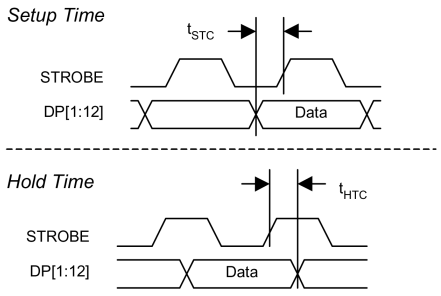


FIGURE 15. LVCMOS Output Load and Transition Times

AC Loading and Waveforms (Continued)



Setup: MODE0 = "0" or "1", MODE1 = "1", SER/$\overline{DES}$ = "1"

FIGURE 16. Serial Setup and Hold Time

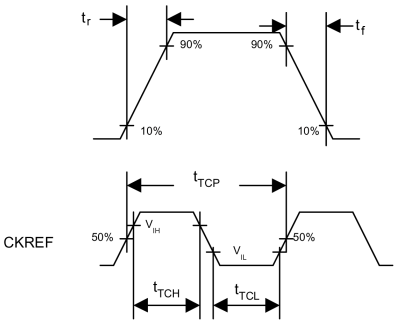
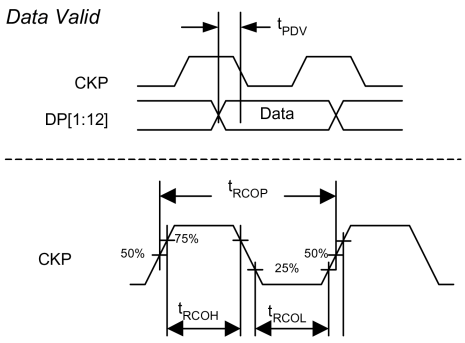
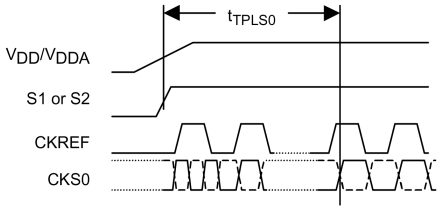


FIGURE 17. LVCMOS Clock Parameters



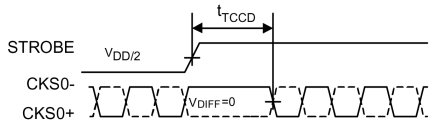
Setup: EN_DES = "1", CKSI and DSI are valid signals

FIGURE 18. Deserializer Data Valid Window Time and Clock Output Parameters



Note: CKREF Signal is free running.

FIGURE 19. Serializer PLL Lock Time



Note: STROBE = CKREF

FIGURE 20. Serializer Clock Propagation Delay

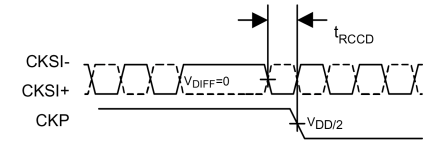


FIGURE 21. Deserializer Clock Propagation Delay

AC Loading and Waveforms (Continued)

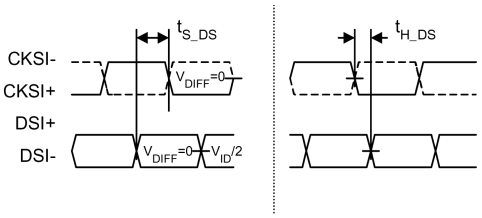


FIGURE 22. Differential Input Setup and Hold Times

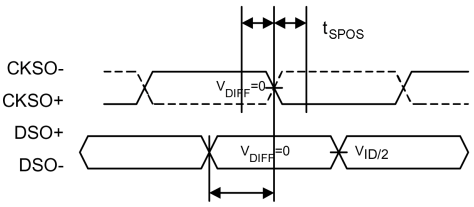
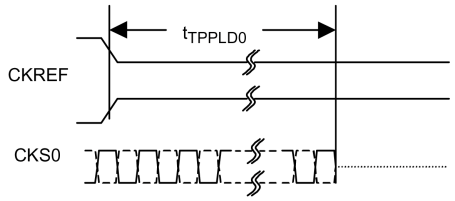


FIGURE 23. Differential Output Signal Skew



Note: CKREF Signal can be stopped either HIGH or LOW

FIGURE 24. PLL Loss of Clock Disable Time

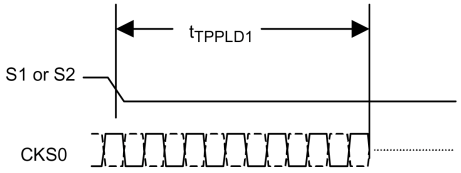
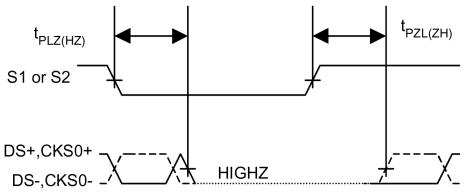
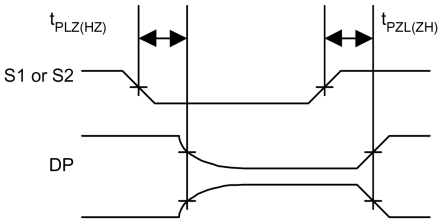


FIGURE 25. PLL PwrDwn Time



Note: CKREF must be active and PLL must be stable

FIGURE 26. Serializer Enable and Disable Time



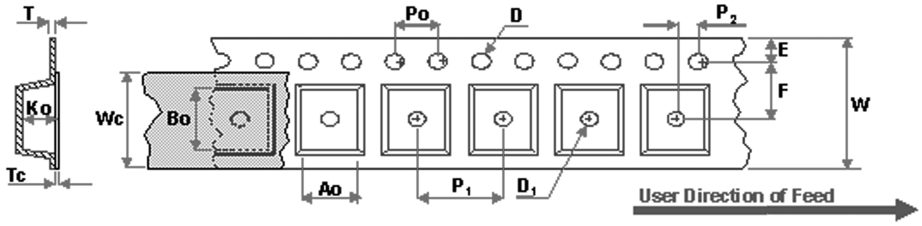
Note: If S1(2) transitioning then S2(1) must = 0 for test to be valid

FIGURE 27. Deserializer Enable and Disable Times

Tape and Reel Specification

TAPE FORMAT for USS-BGA

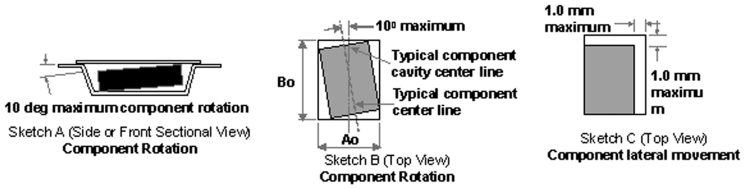
BGA Embossed Tape Dimension



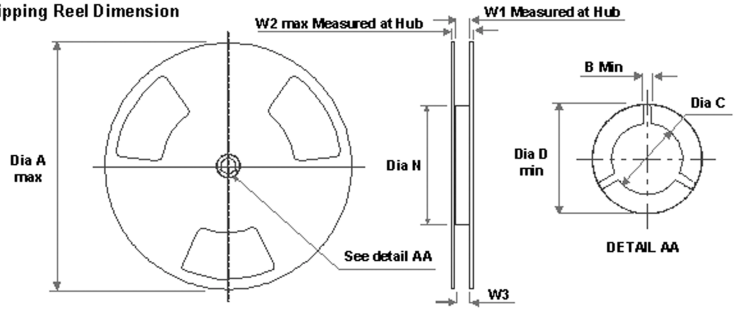
Dimensions are in millimeters

Package	A_0 ±0.10	B_0 ±0.10	D ±0.05	D_1 min	E ±0.1	F ±0.1	K_0 ±0.1	P_1 TYP	P_0 TYP	P_2 ±0/05	T TYP	T_C ±0.005	W ±0.3	W_C TYP
3.5 x 4.5	TBD	TBD	1.55	1.5	1.75	5.5	1.1	8.0	4.0	2.0	0.3	0.07	12.0	9.3

Note: A0, B0, and K0 dimensions are determined with respect to the EIA/JEDEC RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Shipping Reel Dimension



Dimensions are in millimeters

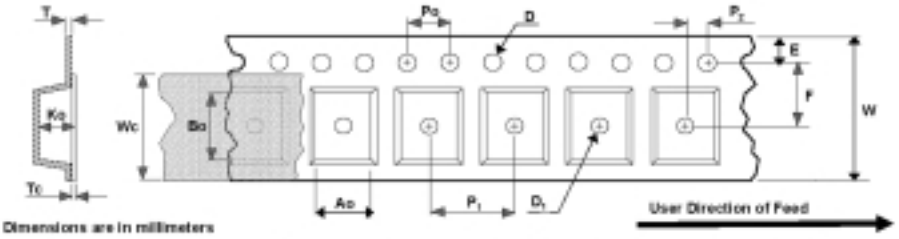
Tape Width	Dia A max	Dim B min	Dia C +0.5/–0.2	Dia D min	Dim N min	Dim W1 +2.0/–0	Dim W2 max	Dim W3 (LSL - USL)
8	330	1.5	13.0	20.2	178	8.4	14.4	7.9 ~ 10.4
12	330	1.5	13.0	20.2	178	12.4	18.4	11.9 ~ 15.4
16	330	1.5	13.0	20.2	178	16.4	22.4	15.9 ~ 19.4

Tape and Reel Specification (Continued)

TAPE FORMAT for MLP

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
MLX	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

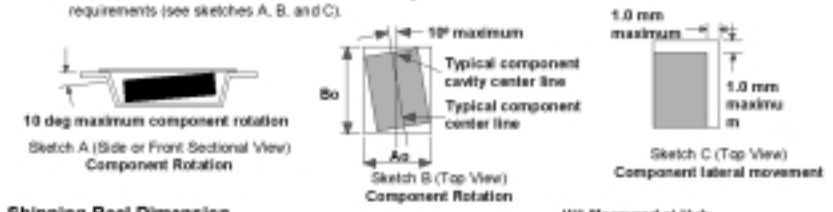
MLP Embossed Tape Dimension



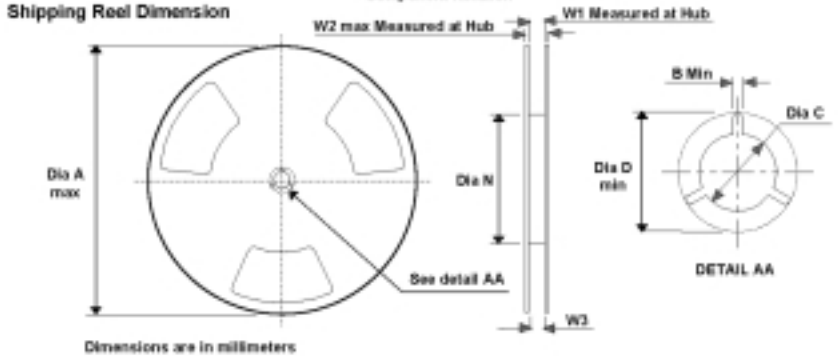
Dimensions are in millimeters

Package	Ao +/-0.10	Bo +/-0.10	D +/-0.05	D1 min	E +/-0.1	F +/-0.1	Ko +/-0.1	P1 TYP	Po TYP	Pr +/-0.05	T TYP	Tc +/-0.005	W +/-0.3	Wc TYP
2 x 2	2.30	2.30	1.55	1.0	1.75	3.5	1.0	8	4	2.0	0.3	0.07	8	5.3
2.5x2.5	2.80	2.80	1.55	1.5	1.75	5.5	0.9	8	4	2.0	0.3	0.07	12	9.3
2.5x3.0	2.80	3.30	1.55	1.5	1.75	5.5	0.9	8	4	2.0	0.3	0.07	12	9.3
2.5x3.5	2.80	3.80	1.55	1.5	1.75	5.5	0.9	8	4	2.0	0.3	0.07	12	9.3
2.5x4.5	2.80	4.80	1.55	1.5	1.75	5.5	0.9	8	4	2.0	0.3	0.07	12	9.3
3.5x4.5	3.80	4.80	1.55	1.5	1.75	5.5	0.9	8	4	2.0	0.3	0.07	12	9.3
2.5x3.0	2.80	3.30	1.55	1.5	1.75	5.5	0.9	8	4	2.0	0.3	0.07	12	9.3
4 x 4	4.35	4.35	1.55	1.5	1.75	5.5	1.1	8	4	2.0	0.3	0.07	12	9.3
5 x 5	5.35	5.35	1.55	1.5	1.75	5.5	1.1	8	4	2.0	0.3	0.07	12	9.3
6 x 6	6.30	6.30	1.55	1.5	1.75	7.5	1.1	12	4	2.0	0.3	0.07	16	13.3

Notes: Ao, Bo, and Ko dimensions are determined with respect to the EIA /Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



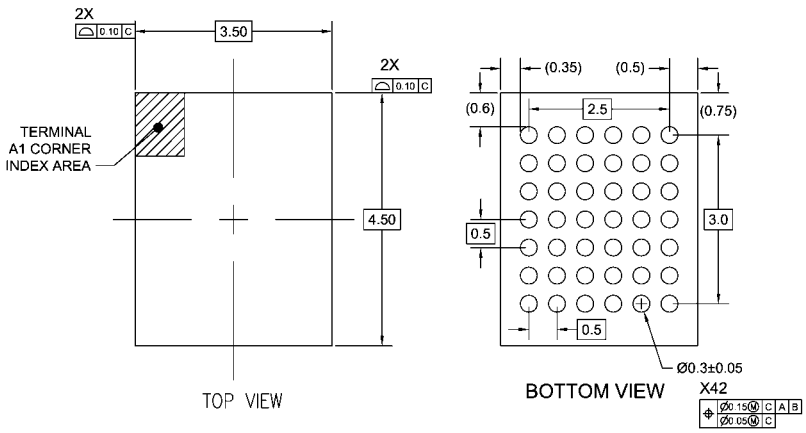
Shipping Reel Dimension

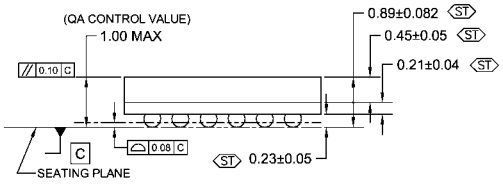


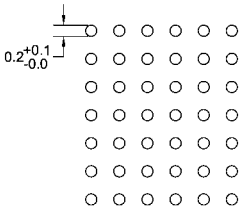
Dimensions are in millimeters

Tape Width	Dia A max	Dim B min	Dia C +.5/-.2	Dia D min	Dia N min	Dim W1 +2/-0	Dim W2 max	Dim W3 (LSL - USL)
8	330	1.5	13	20.2	178	8.4	14.4	7.9~10.4
12	330	1.5	13	20.2	178	12.4	18.4	11.9~15.4
16	330	1.5	13	20.2	178	16.4	22.4	15.9~19.4

Physical Dimensions inches (millimeters) unless otherwise noted







LAND PATTERN
RECOMMENDATION

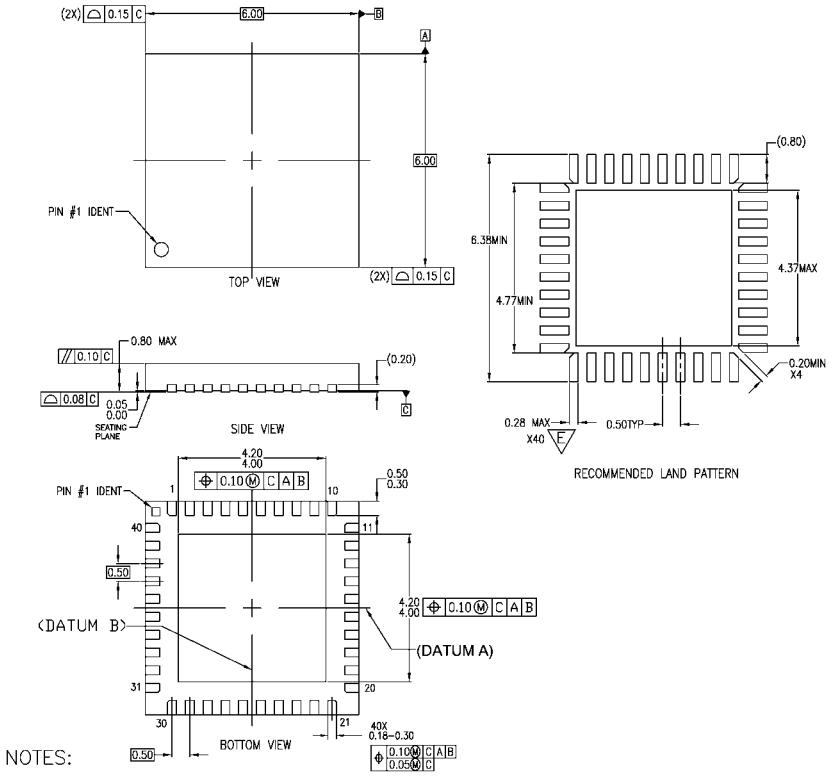
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−195,
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. STATISTICAL TOLERANCING FOR REFERENCE REFER TO MAX DIMENSION FOR QA INSPECTION
E. LAND PATTERN RECOMENDATION PER IPC−7351 TABLE14−15 LAND PATTERN NAME PER TABLE 3−15: BGA50P+6X7−42

BGA42ArevA

Pb-Free 42-Ball Ultra Small Scale Ball Grid Array (USS-BGA), JEDEC MO-195, 3.5mm Wide
Package Number BGA42A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO−220, VARIATION WJJD−2 WITH EXCEPTION THIS IS A SAWN VERSION

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

D. LAND PATTERN PER IPC SM−782 FABRICATION AND ASSEMBLY TOLERANCES OF 0.1 MM APPLIED

E. WIDTH REDUCED TO AVOID SOLDER BRIDGING.

MLP040ArevA

Pb-Free 40-Terminal Molded Leadless Package (MLP), Quad, JEDEC MO-220, 6mm Square
Package Number MLP040A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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