

# FAN8038B(KA3038)

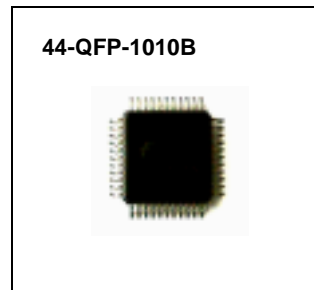
## 4-Channel Motor Drive IC

### Features

- 4-CH H-Bridge Driver
- Built-in DC/DC Converter Controller Circuit
- Built-in Reset Circuit
- Built-in Battery Charging Circuit
- Built-in Voltage Drop Detector
- Built-in Thermal Shutdown Circuit
- Built-in General OP-AMP
- Low Power Consumption
- Built-in Power Controller Circuit

### Description

FAN8038B is monolithic IC for portable CD player.



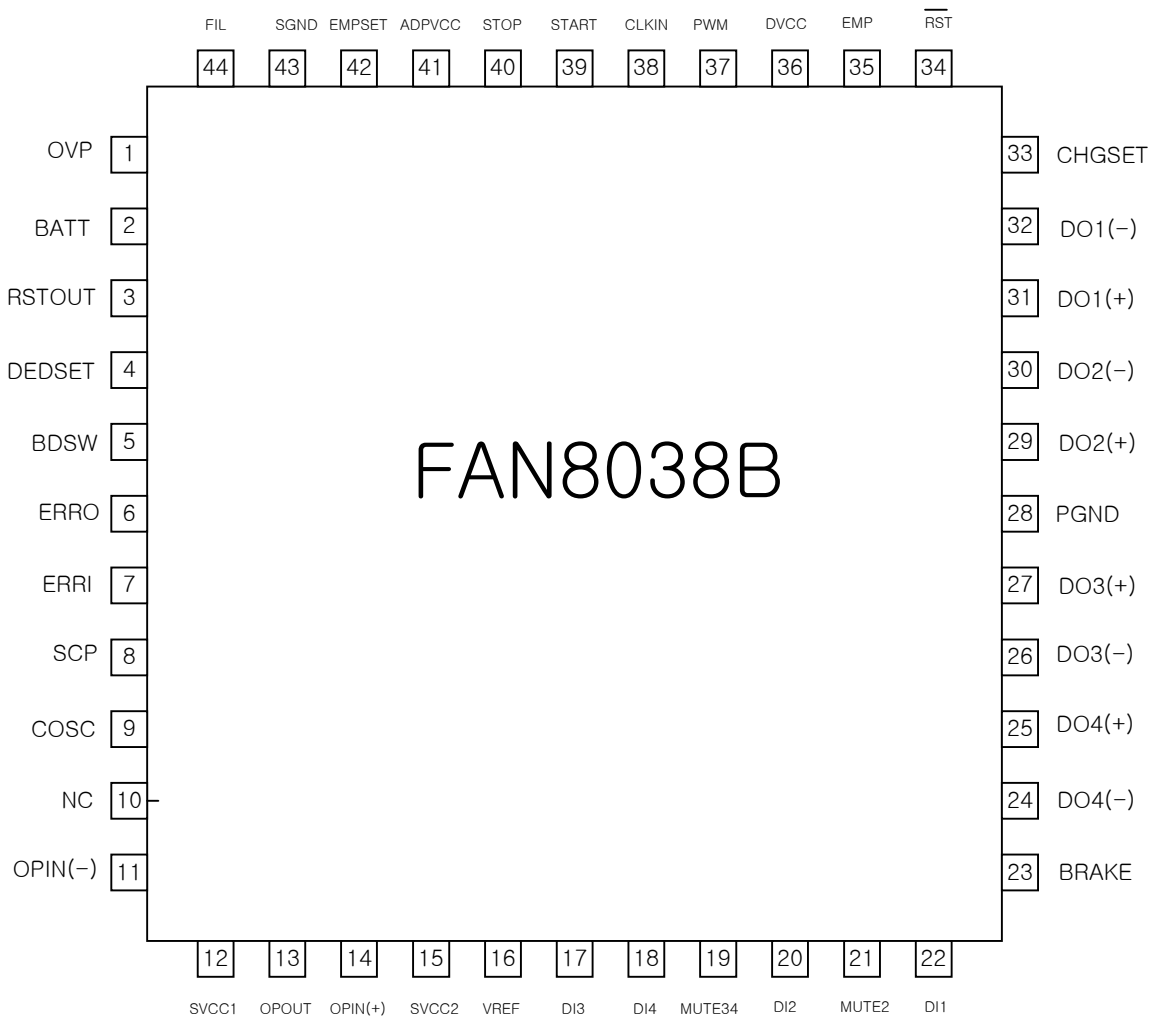
### Typical application

- Portable Compact Disk Player (CDP)
- Portable Mini Disk Player (MD)
- Disc-Man
- Other Potable Compact Disk Media

### Ordering Information

Device	Package	Operating Temp.
FAN8038B	44-QFP-1010B	-35°C ~ +85°C

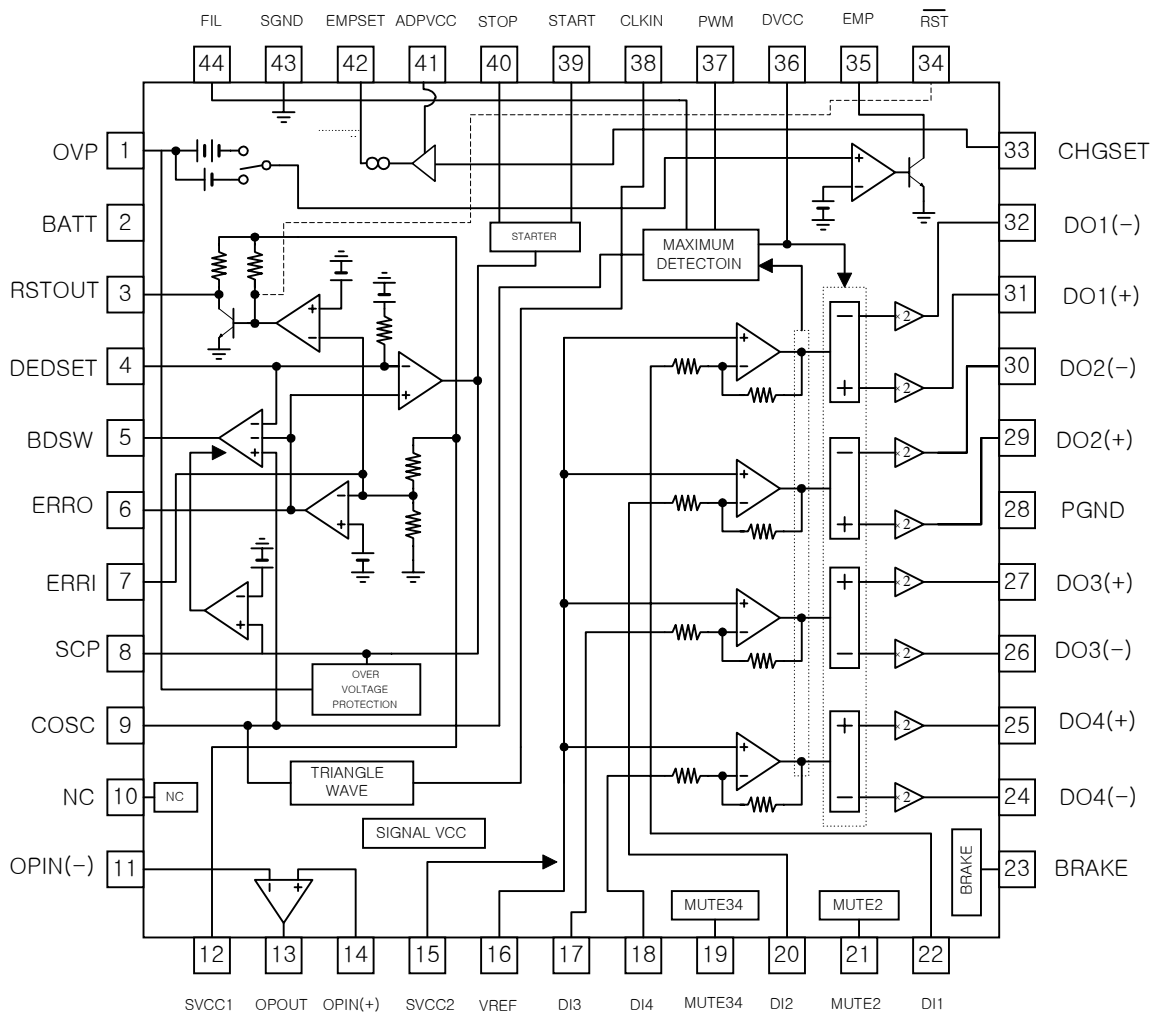
## Pin Assignments



## Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	OVP	Battery Power Supply Mode
2	BATT	Battery Power Supply
3	RSTOUT	RSTOUT Detection Output
4	DEDSET	DEDSET Time Setting
5	BDSW	Booster Transistor Drive
6	ERRO	Error Amp Output
7	ERRI	Error Amp Input
8	SCP	Short Circuit Protection Setting
9	COSC	Triangular Wave Output
10	N.C	No Connection
11	OPIN(-)	OP-AMP Negative Input
12	SVCC1	Control Circuit Power Supply
13	OPOUT	OP-AMP Output
14	OPIN(+)	OP-AMP Positive Input
15	SVCC2	Pre-Drive Power Supply
16	VREF	Reference Voltage
17	DI3	CH3 Control Signal Input
18	DI4	CH4 Control Signal Input
19	MUTE34	CH3, 4 Mute
20	DI2	CH2 Control Signal Input
21	MUTE2	CH2 Mute
22	DI1	CH1 Control Signal Input
23	BRAKE	CH1 Brake
24	DO4(-)	CH4 Negative Output
25	DO4(+)	CH4 Positive Output
26	DO3(-)	CH3 Negative Output
27	DO3(+)	CH3 Positive Output
28	PGND	Power Unit Power Ground
29	DO2(+)	CH2 Positive Output
30	DO2(-)	CH2 Negative Output
31	DO1(+)	CH1 Positive Output
32	DO1(-)	CH1 Negative Output
33	CHGSET	Charge Current Setting
34	RST	RSTOUT Inverting Output
35	EMP	Empty Detection Output
36	DVCC	H-Bridge Power Supply
37	PWM	PWM Transistor Drive
38	CLKIN	External Clock Input
39	START	Boost DC/DC Converter Starting
40	STOP	Boost DC/DC Converter Off
41	ADPVCC	Charging Circuit Power Supply
42	EMPSET	Empty Dection Level Converting
43	SGND	Signal Ground
44	FIL	PWM Phase Compensation

# Internal Block Diagram



## Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Value	Unit
Maximum Supply Voltage	VCC	13.2	V
Maximum Output Current	IO	500	mA
Power Dissipation	PD	1.0	W
Operating Temperature	TOPR	-35 ~ +85	°C
Storage Temperature	TSTG	-55 ~ +150	°C

## Recommended Operating Conditions (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Charging Circuit Power Supply Voltage	ADPVCC	3.0	4.5	8.0	V
Power Supply Voltage	BATT	1.5	2.4	8.0	V
Control Circuit Power Supply Voltage	SVCC	2.7	3.2	5.5	V
PRE-Driver VCC	SVCC2	2.7	3.2	5.5	V
Output Voltage	VM	-	PWM	BATT	V
Operating Temperature	Ta	-10	25	70	°C

## Electrical characteristics

(Ta=25°C, BATT=2.4V, SVCC1=SVCC2=3.2V, VREF=1.6V, ADPVCC=0V, fCLKIN=88.2kHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>COMMON SECTION</b>						
BATT Stand-by Current	IST	BATT=10.5V,SVCC1, 2=VREF=0V	-	-	5	μA
BATT Supply Current (No Load)	IBATT	DVCC=0.45V, MUTE34=3.2V	-	2.5	3.5	mA
SVCC Supply Current (No Load)	ISVCC1	DVCC=0.45V, MUTE34=3.2V, ERRI=0V	-	3.0	3.5	mA
SVCC2 Supply Current (No Load)	ISVCC2	DVCC=0.45V, MUTE34=3.2V	-	3.5	5.0	mA
ADPVCC Supply Current (No Load)	IADPVCC	ADPVCC=4.5V, ROUT=OPEN	-	0.2	1.0	mA
<b>H-DRIVE PART</b>						
Voltage Gain CH1, 3, 4 CH2	GVC134 GVC2	-	12 21.5	14 23.5	16 24.5	dB
Gain Error By Polarity	ΔGVC	-	-2	0	2	dB
Input pin Resistance CH1, 3, 4 CH2	RD1134 RDI2	IN=1.7 & 1.8V	9 6	11 7.5	13 9	KΩ
Maximum Output Voltage	VOUT	RL=8Ω, DVCC=BATT=4V, IN=0 ~ 3.2V	1.9	2.1	-	V
Saturation Voltage (Lower)	VSAT1	IO= -300mA, IN=0 & 3.2V	-	240	400	mV
Saturation Voltage (Upper)	VSAT2	IO=300mA, IN=0 & 3.2V	-	240	400	mV
Input offset Voltage	VIO	-	-8	0	8	mV
Output Offset Voltage CH1, 3, 4 CH2	VOO134 VOO2	VREF=IN=1.6V	-70 -130	0 0	70 130	mV
DEAD Zone	VDB	-	-20	0	20	mV
Brake1 On Voltage	VM1ON	DI1=1.8V	2.0	-	-	V
Brake1 Off Voltage	VM1OFF	DI1=1.8V	-	-	0.8	V
MUTE2 On Voltage	VM2ON	DI2=1.8V	2.0	-	-	V
MUTE2 Off Voltage	VM2OFF	DI2=1.8V	-	-	0.8	V
MUTE34 On Voltage	VM34ON	DI3=DI4=1.8V	-	-	0.8	V
MUTE34 Off Voltage	VM34OFF	DI3=DI4=1.8V	2.0	-	-	V
VREF On Voltage	VREFON	INn=1.8V(N=1, 2, 3, 4)	1.2	-	-	V
VREF Off Voltage	VREFOFF	INn=1.8V(N=1, 2, 3, 4)	-	-	0.8	V
BRAKE1 Brake Current	IBRAKE	Brake Current	4	7	10	mA

\*Granted Design Value

**Electrical Characteristics** (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>PWM POWER SUPPLY DRIVING</b>						
PWM Sink Current	IPWM	DI1=2.1V	10	13	17	mA
*DVCC Level Shift Voltage	VSHIF	DI1=1.8V, DVCC-OUT1F	0.35	0.45	0.55	V
DVCC Leak Current	IDLK	DVCC=9V, SVCC1,2=BATT=0V	-	0	5	μA
*PWM Amp Transfer Gain	GPWM	DI1=1.8V, DVCC=1.2V ~ 1.4V	1/60	1/50	1/40	1/kΩ
<b>DC/DC CONVERTER</b>						
<b>ERROR AMP</b>						
SVCC1 Pin Threshold Voltage	VS1TH	-	3.05	3.20	3.35	V
ERRO Pin Output Voltage H	VEOH	ERRI=0.7V, IO = -100μA	1.4	1.6	-	V
ERRO Pin Output Voltage L	VEOL	ERRI=1.3V, IO = 100μA	-	-	0.3	V
<b>SHORT CIRCUIT PROTECTION</b>						
SCP Pin Voltage	VSCP	ERRI=1.3V	-	0	0.1	V
SCP Pin Current 1	ISCP1	ERRI=0.7V	6	10	16	μA
SCP Pin Current 2	ISCP2	ERRI=1.3V, OFF=0V	12	20	32	μA
SCP Pin Current 3	ISCP3	ERRI=1.3V, BATT=9.5V	12	20	32	μA
*SCP Pin Impedance	RSCP	-	175	220	265	kΩ
SCP Pin Threshold Voltage	VSCPTH	ERRI=0.7V, COSC=470PF	1.10	1.20	1.30	V
Over Voltage Protection Detect	VOVP	OVP Voltage	9.5	10	10.5	V
<b>TRANSISTOR DRIVING</b>						
BDSW Pin Output Voltage 1H	VSW1H	BATT=COSC=1.5V =SVCC2=0V, 10mA	0.78	0.98	1.13	V
BDSW Pin Output Voltage 2H	VSW2H	COSC=0V, IO = -10mA, ERRI=0.7V SCP=0V	1.0	1.5	-	V
BDSW Pin Output Voltage 2L	VSW2L	CT=2V, IO=1-mA	-	0.3	0.45	V
BDSW Pin Oscillating Reequency1	fSW1	COSC=470pF, =SVCC2=0V	65	80	95	kHz
SW Pin Oscillating Reequency 2	fSW2	COSC=470pF, CLKIN=0V	60	70	82	kHz
BDSW Pin Oscillating Reequency 3	fSW3	COSC=470pF	-	88.2	-	kHz
*BDSW Pin Minimum Pulse Width	TSWMIN	COSC=470pF, ERRO=0.5 → 0.7V	0.01	-	0.6	μs
Pulse Duty Start	DSW1	COSC=470PF, SVSS1,SVCC2=0V	40	50	60	%
MAX. Pulse Duty at Self-Running	DSW2	COSC=470pF, ERRO=0.8V, CLKIN=0V	50	60	70	%
MAX. Pulse Duty at CLKIN Synchronization	DSW3	ERRO=0.8V, COSC=470pF	45	55	65	%

\*Granteed Design Value

**Electrical Characteristics** (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>DEAD TIME</b>						
*DESET Pin Impedance	RDESET	-	52	65	78	k $\Omega$
DESET Pin Output Voltage	VDESET	-	0.78	0.88	0.98	V
<b>INTERFACE</b>						
STOP Pin Threshold Voltage	VSTOPH	ERRI=1.3V	2.0	-	-	V
STOP Pin Bias Current	ISTOP	OFF=0V	75	95	115	$\mu$ A
START Pin On Threshold Voltage	VSTATH1	SVCC1,SVCC2=0V, COSC=2V	1.3	-	-	V
START Pin Off Threshold Voltage	VSTATH2	SVCC1,SVCC2=0V, COSC=2V	-	-	2.1	V
START Pin Bias Current	ISTART	START=0V	13	16	19	$\mu$ A
CLKIN Pin Threshold Voltage H	VCLKINTH H	-	2.0	-	-	V
CLKIN Pin Threshold Voltage L	VCLKINTH L	-	-	-	0.8	V
CLKIN Pin Bias Current	ICLKIN	CLKIN=3.2V	-	-	10	$\mu$ A
<b>START CURCUIT</b>						
Starter Switching Voltage	VSSV	SVCC1,SVCC2=0V $\rightarrow$ 3.2V START=0V	2.3	2.5	2.7	V
Starter Switching Hysteresis Width	VSSHS	START=0V	130	200	300	mV
Discharge Release Voltage	VDIS	-	1.63	1.83	2.03	V
<b>RESET CIRCUIT</b>						
*SVCC1 RESET Threshold Voltage Ratio	RRSTOTH	-	85	90	95	%
RESET Detection Hysteresis Width	VRSTHS	-	25	50	100	mV
RSTOUT Pin Output Voltage	VRSTO	IO=1mA, SVCC1,SVCC2=2.8V	-	-	0.5	V
RSTOUT Pin Pull Up Resistance	RRSTO	-	72	90	108	k $\Omega$
RST Pin Output Voltage 1	VRST1	IO= -1mA, SVCC1,SVCC2=2.8V	2.0	-	2.4	V
RST Pin Output Voltage 2	VRST2	IO= -1mA, SVCC1,SVCC2=0V	2.0	-	2.4	V
*RST Pin Pull Up Resistance	RRST	-	77	95	113	k $\Omega$

\*Granteed Design Value



**Electrical Characteristics** (Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>OP-AMP</b>						
Input Bias Current	IBIAS	IN(+)=1.6V	-	-	300	nA
Input Offset Voltage	VOFOP	IN(+)=1.6V	-5.5	0	5.5	mV
High Level Output Voltage	VOHOP	RL=OPEN	2.8	-	-	V
Low Level Output Voltage	VOLOP	RL=OPEN	-	-	0.2	V
Output Drive Current (Source)	VSOURCE	50Ω GND	-	-6.5	-3.0	mA
Output Drive Current (Sink)	VSINK	50Ω SVCC	0.4	0.7	-	mA
*Open Loop Voltage Gain	GVO	VIN= -75dB, F=1kHz	-	70	-	dB
*Slew Rate	SR	-	-	0.5	-	V/μs
<b>BATTERY CHARGING CURCUIT</b>						
CHGSET Pin Bias Voltage	VCHGSET	ADPVCC=4.5V, CHGSET=1.8kΩ	0.71	0.81	0.91	V
*CHGSET Pin Output Resistance	RCHGSET	ADPVCC=4.5V	0.75	0.95	1.20	kΩ
EMPSET Pin Leak Current 1	IEMPSET	ADPVCC=4.5V, CHGSET=OPEN	-	-	1.0	μA
EMPSET Pin Leak Current 2	IEMPSET	ADPVCC = 0.6V, CHGSET = 1.8kΩ	-	-	1.0	μA
EMPSET Pin Saturation Voltage	VEMPSET	ADPVCC = 4.5V, IO = 300mA, CHGSET = 0Ω	-	0.45	1.0	V
<b>EMPTY DETECTION</b>						
EMP Detection Voltge 1	VEMPT1	VEMPSET = 0V	2.1	2.2	2.3	V
EMP Detection Voltge 2	VEMPT2	IEMPSET = -2μA	1.7	1.8	1.9	V
EMP Detection Hysteresis Voltage 1	VEMHS1	VEMPSET = 0V	25	50	100	mV
EMP Detection Hysteresis Voltage 2	VEMHS2	IEMPSET = -2μA	25	50	100	mV
EMP Pin Output Voltage	VEMP	IO = 1mA, OVP = 1V	-	-	0.5	V
EMP Pin Output Leak Current	IEMPLK	OVP = 2.4V	-	-	1.0	μA
*OVP Pin Input Resistance	ROVP	VEMPSET = 0V	17	23	27	kΩ
OVP Pin Leak Current	IOVPLK	SVCC1 = SVCC2 = 0V, OVP = 4.5V	-	-	1.0	V
EMP_SET Pin Detection Voltage	VEMPSET	VEMPSET = BATT-EMPSET, OVP = 2V	1.5	-	-	V
EMP_SET Pin Detection Current	IEMPSET	EMPSET	-2	-	-	μA

\*Granteed Design Value

## Application Information

### 1. Mute Function

- When The BRAKE Pin is low is normal operation (high is CH1 mute on).
- When The Mute2 Pin is low is normal operation (high is CH2 mute on).
- When The Mute34 Pin is high is normal operation (low is CH3,4 mute on).

### 2. Vref Drop Mute (Figure 1)

- When the Voltage of the mute pin is above 1V, the mute circuit is stopped and the output circuit is.

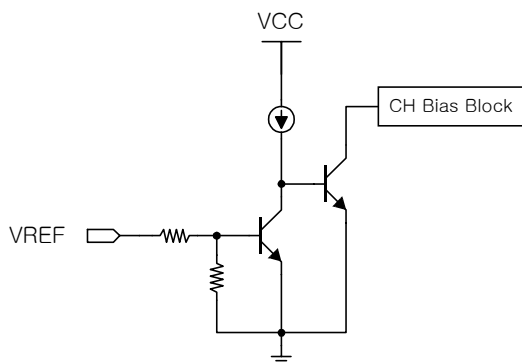


Figure 1. VREF Drop MUTE Circuit

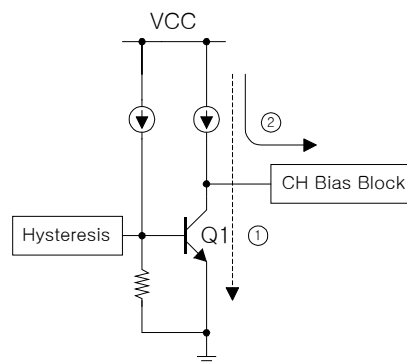


Figure 2. TSD Circuit

### 3. Thermal Shutdown(Figure 2)

- If the chip temperature rises above 150°C, then the thermal shutdown (TSD) circuit is activated and the output circuit will be mute.

### 4. H-bridge Driver (4-Channels)

Driver input resistance is 10kΩ of CH1, CH3, CH4 and input resistance of CH2 is 7.5kΩ.

Driver gain can obtain under -mentioned

$$\text{CH1, 3, 4: } \text{GV} = 20\log\left|\frac{55\text{K}}{11\text{K} + \text{R}}\right|$$

$$\text{CH2: } \text{GV} = 20\log\left|\frac{110\text{K}}{7.5\text{K} + \text{R}}\right|$$

R is External resistance.

### 5. Switching Regulated Power Supply Drive

- This circuit detects a maximum output value of 4CH drivers and then generates PWM Signal.
- External Component is PNP-Tr, Coil, Schottky Diodeand Capacitor .

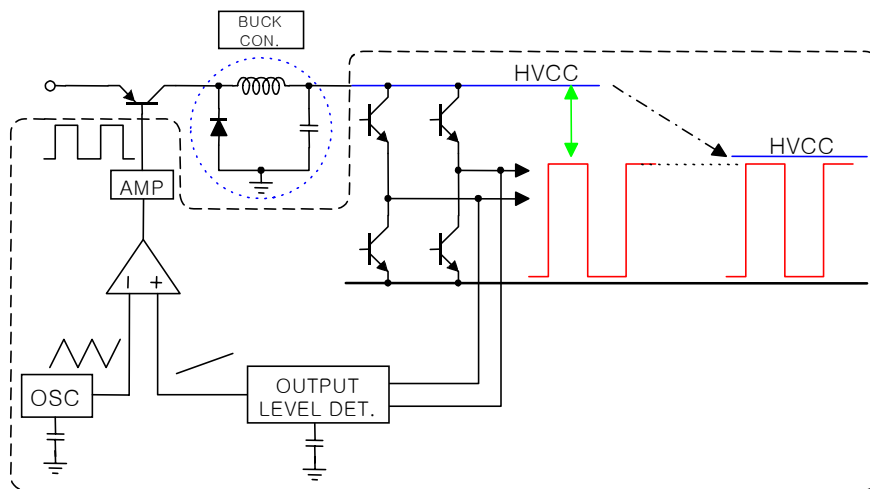


Figure 1. Switching Regulated Power Supply

### 6. DC/DC Converter Control Circuit

- Booster circuit needs External component. and the voltage() is defined as follows.

$$SVCC1 = 1.267 \times \frac{\frac{R1 \cdot R3}{R1 + R3} + \frac{R2 \cdot R4}{R2 + R4}}{\frac{R2 \cdot R4}{R2 + R4}}$$

R1 = Resistor1
R2 = Resistor2
R3 = 30KΩ
R4 = 30.5KΩ

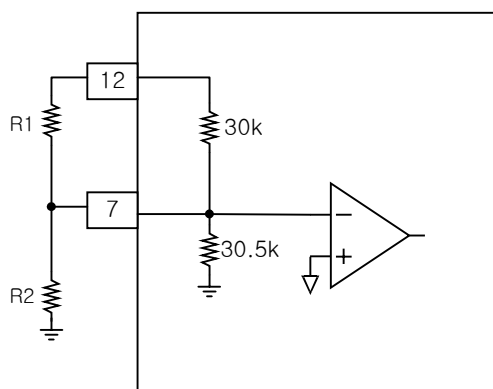


Figure 2. Output Voltage

- Short Circuit Protection function when GND and is short, ERRI become LOW and ERRO HIGH and it makes capacitor charging. fanally AMP3 is OFF.(figure 5)

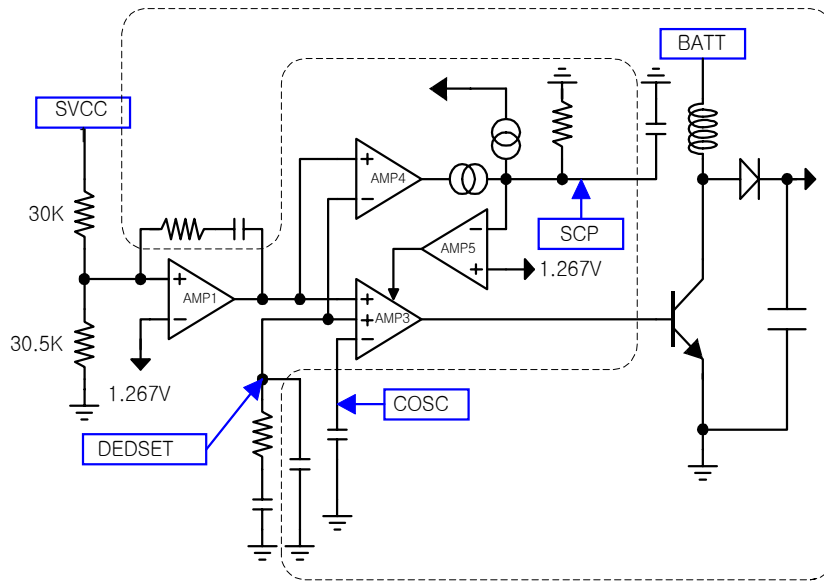


Figure 3. DC/DC Converter Control Circuit

Switching off time depen on a capacitor of the SCP . and the equation is as follow.

$$t = C_{SCP} \times \frac{V_{TH}}{I_{SCP}} \quad (V_{TH} = 1.25V, I_{SPRT} = 10\mu A)$$

- Max Duty can be controlled resistor. the equation is as follow.

$$t = C_{DEDSET} \times R \quad (R = 65K\Omega)$$

- Capacitor of the SCP terminal can control disable switching time and it can be calculated by as follow equation.

$$t = C_{SCP} \times \frac{V_{TH}}{I_{STOP}} \quad (V_{TH} = 1.25V, I_{OFF} = 20\mu A)$$

- Over Voltage Protection BATT Voltage is over 9.7V charging SCP terminal Capacitor, it reach to  $V_{TH}$  SW terminal signal is OFF the equation is as follow

$$t = C_{SCP} \times \frac{V_{TH}}{I_{HV}} \quad (V_{TH} = 1.25V, I_{HV} = 20\mu A)$$

- If Output Voltage of RSTOUT Circuit DC/DC Conver is over than 90%, RSTOUT terminal turn to HIGH and Hysteresis is 50mV. and RSTOUT stste is ON.

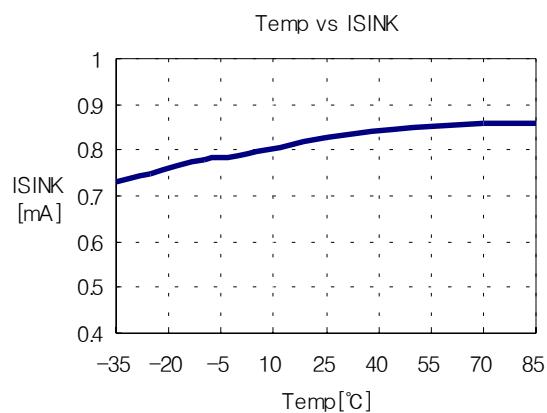
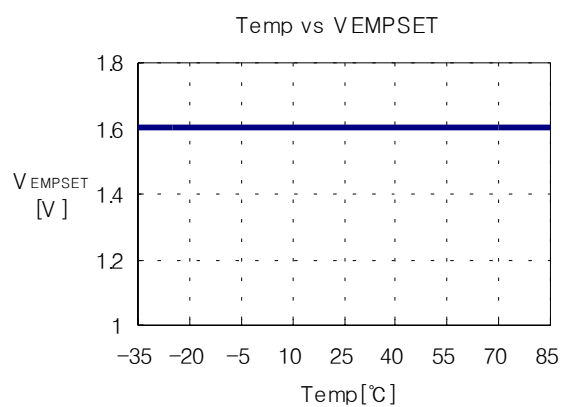
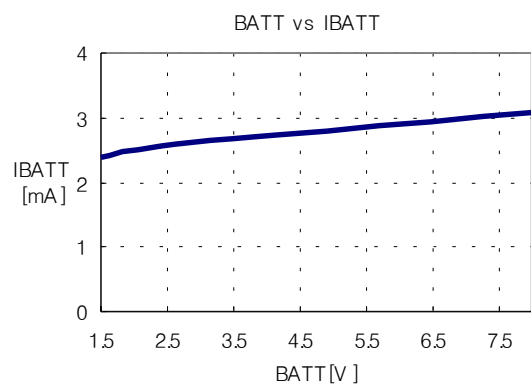
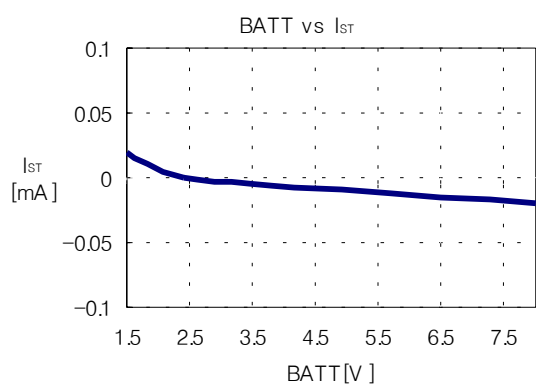
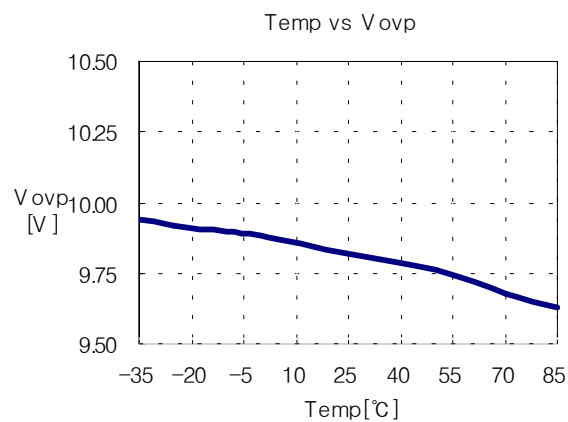
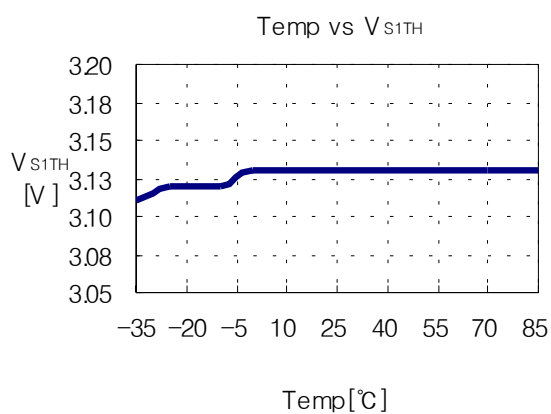
### 7. Empty Detecting Circuit.

EMPSET	Detect Voltage	Hysteresis	Mode
LOW	2.2V	50mV	Battery Mode
HIGH-Z	1.8V	50mV	Adapter Mode

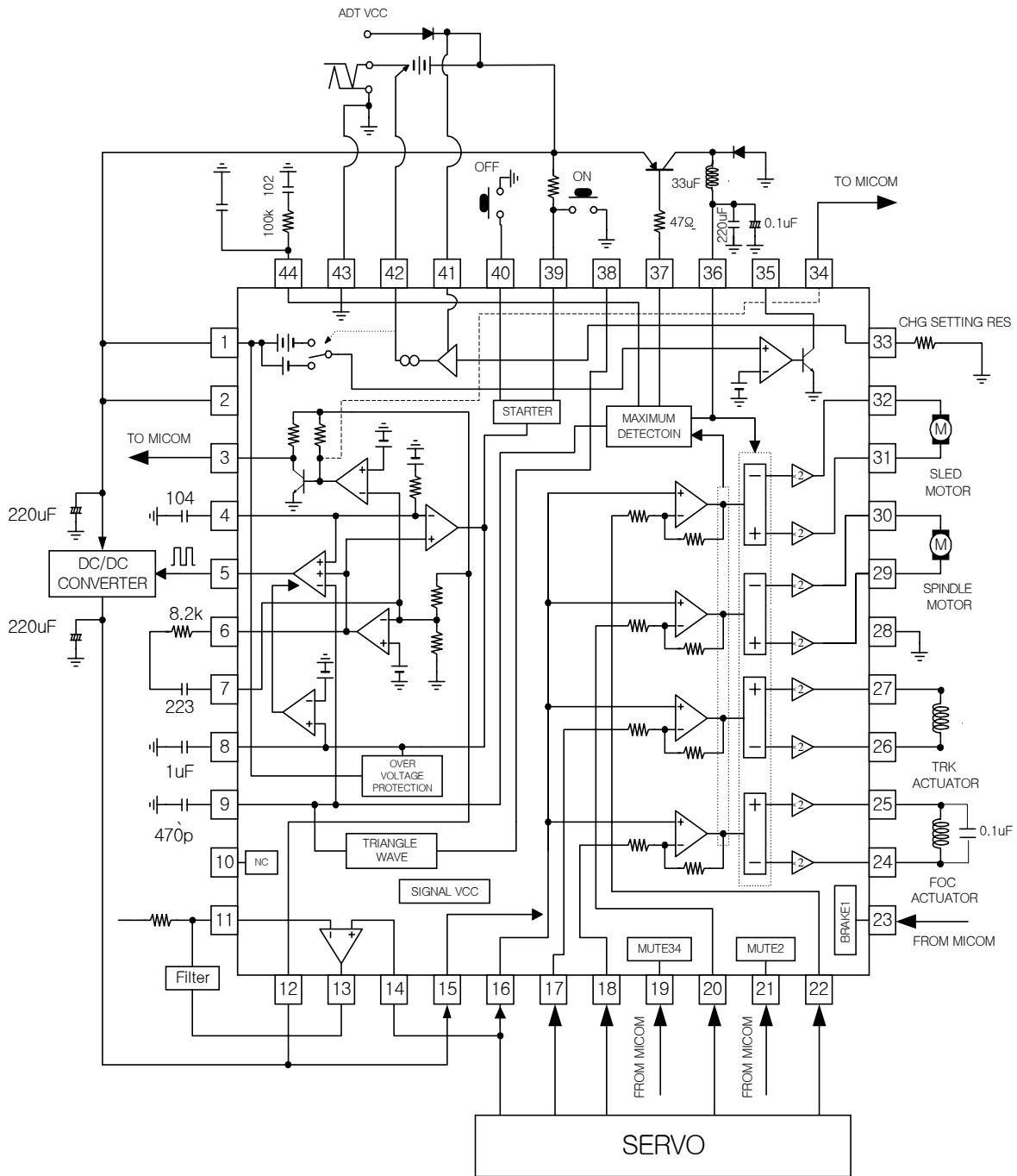
### 8. Battery Charging Circuit

- the battery charger circuit is separated from any other block .
- TSD operate at 150°C. Hysteresis is 30°C

## Typical Performance Characteristics



# Application Circuits





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