FAN4272

Dual, Low Cost, +2.7V & +5V, Rail-to-Rail I/O Amplifier

Features at 2.7V

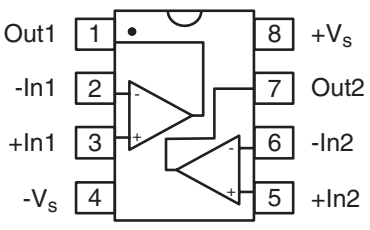
- 130µA supply current per amplifier
- 4MHz bandwidth
- Output swings to within 25mV of either rail
- Input voltage range exceeds the rail by >250mV
- 4V/µs slew rate
- 16mA output current
- 22nV/√Hz input voltage noise
- Operating temperature range: -40°C to +125°C
- Directly replaces TLC2272 in single supply applications
- Available in SOIC-8 and MSOP-8 package options
- Available evaluation boards:
  KEB006 (SOIC) and KEB010 (MSOP)

Applications

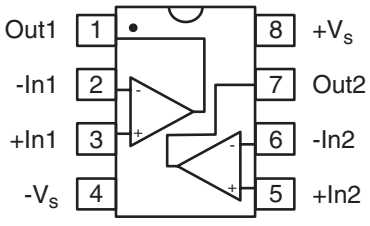
- Automotive applications
- Portable/battery-powered applications
- PCMCIA, USB
- Mobile communications, cellular phones, pagers
- Notebooks and PDA's
- Sensor Interface
- A/D buffer
- Active filters
- Signal conditioning
- Portable test instruments

FAN4272 Packages

SOIC



MSOP

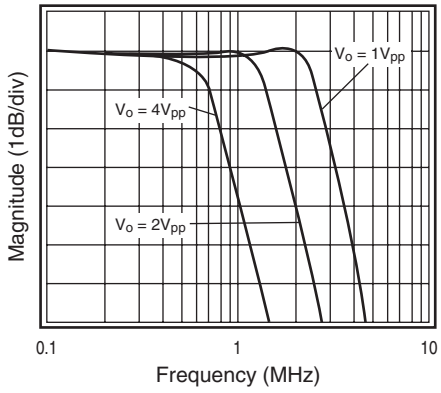


Description

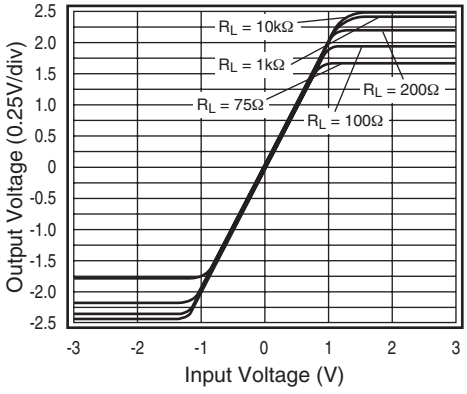
The FAN4272 is an ultra-low cost, low power, voltage feedback amplifier. At 5V, the FAN4272 uses only 160µA of supply current per amplifier and is designed to operate from a supply range of 2.5V to 5.5V (±1.25V to 2.75V). The input voltage range exceeds the negative and positive rails.

The FAN4272 offers high bipolar performance at a low CMOS price. The FAN4272 offers superior dynamic performance with a 4MHz small signal bandwidth and 4V/µs slew rate. The combination of low power, high bandwidth, and rail-to-rail performance make the FAN4272 well suited for battery-powered communication/computing systems.

Large Signal Freq. Response V_s = +5V



Output Swing vs. Load V_s = +5V



Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
Supply Voltages	0	+6	V
Maximum Junction Temperature	–	+175	°C
Storage Temperature Range	-65	+150	°C
Lead Temperature, 10 seconds	–	+260	°C
Operating Temperature Range, recommended	-40	+125	°C
Input Voltage Range	$-V_S$ -0.5	$+V_S$ +0.5	V

Electrical Specifications

(V_S = +2.7V, G = 2, R_L = 10kΩ to V_S/2, R_f = 5kΩ, T_a = 25°C; unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
AC Performance					
-3dB Bandwidth[1]	G = +1, V_O = 0.02V_{pp}		4		MHz
	G = +2, V_O = 0.2V_{pp}		3.7		MHz
Large Signal Bandwidth	G = +2, V_O = 2V_{pp}		1.1		MHz
Gain Bandwidth Product			1.7		MHz
Rise and Fall Time	1V step		215		ns
Overshoot	1V step		<1		%
Slew Rate	1V step		4		V/µs
2nd Harmonic Distortion	1V_{pp}, 10kHz		-74		dBc
3rd Harmonic Distortion	1V_{pp}, 10kHz		-62		dBc
THD	1V_{pp}, 10kHz		0.08		%
Input Voltage Noise	>10kHz		22		nV/√Hz
Crosstalk	>100kHz		95		dB
DC Performance					
Input Offset Voltage			<0.5		mV
Average Drift			4		µV/°C
Input Bias Current			90		nA
Average Drift			100		pA/°C
Power Supply Rejection Ratio[2]	DC	70	85		dB
Open Loop Gain	R_L = 10kΩ		75		dB
Quiescent Current Per Channel			130		µA
Input Characteristics					
Input Resistance			12		MΩ
Input Capacitance			1.8		pF
Input Common Mode Voltage Range			-0.25 to 2.95		V
Common Mode Rejection Ratio	DC, V_{cm} = 0V to V_S		78		dB
Output Characteristics					
Output Voltage Swing	R_L = 10kΩ to V_S/2[2]	0.06 to 2.64	0.025 to 2.68		V
	R_L = 1kΩ to V_S/2		0.07 to 2.645		V
	R_L = 200Ω to V_S/2		0.198 to 2.59		V
Output Current			±16		mA
Power Supply Operating Range		2.5	2.7	5.5	V

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes:

1. For G = +1, R_f = 0.
2. Guaranteed by testing or statistical analysis at 25°C.

Electrical Specifications

(V_S = +5V, G = 2, R_L = 10kΩ to V_S/2, R_f = 5kΩ, T_a = 25°C; unless otherwise noted)

Parameter	Conditions	Min.	Typ.	Max.	Unit
AC Performance					
-3dB Bandwidth[1]	G = +1, V_o = 0.02V_{pp}		4		MHz
	G = +2, V_o = 0.2V_{pp}		4.7		MHz
Large Signal Bandwidth	G = +2, V_o = 2V_{pp}		1.7		MHz
Gain Bandwidth Product			1.8		MHz
Rise and Fall Time	1V step		150		ns
Overshoot	1V step		<1		%
Slew Rate	1V step		6		V/µs
2nd Harmonic Distortion	2V_{pp}, 10kHz		-73		dBc
3rd Harmonic Distortion	2V_{pp}, 10kHz		-75		dBc
THD	2V_{pp}, 10kHz		0.03		%
Input Voltage Noise	>10kHz		23		nV/√Hz
Crosstalk	>100kHz		95		dB
DC Performance					
Input Offset Voltage[2]		-2	<0.5	+2	mV
Average Drift			8		µV/°C
Input Bias Current[2]		-420	90	420	nA
Average Drift			100		pA/°
Input Offset Current[2]		-50		+50	nA
Power Supply Rejection Ratio[2]	DC	70	85		dB
Open Loop Gain	R_L = 10kΩ		72		dB
Quiescent Current Per Channel[2]			160	235	µA
Input Characteristics					
Input Resistance			12		MΩ
Input Capacitance			1.7		pF
Input Common Mode Voltage Range			-0.25 to 5.25		V
Common Mode Rejection Ratio[2]	DC, V_{cm} = 0V to V_S	58	85		dB
Output Characteristics					
Output Voltage Swing	R_L = 10kΩ to V_S/2[2]	0.09 to 4.91	0.031 to 4.976		V
	R_L = 1kΩ to V_S/2		0.094 to 4.94		V
	R_L = 200Ω to V_S/2		0.315 to 4.865		V
Output Current			±30		mA
Power Supply Operating Range		2.5	2.7	5.5	V

Min/max ratings are based on product characterization and simulation. Individual parameters are tested as noted. Outgoing quality levels are determined from tested parameters.

Notes:

1. For G = +1, R_f = 0.
2. Guaranteed by testing or statistical analysis at 25°C.
3. R_L = 10kΩ to V_S/2.

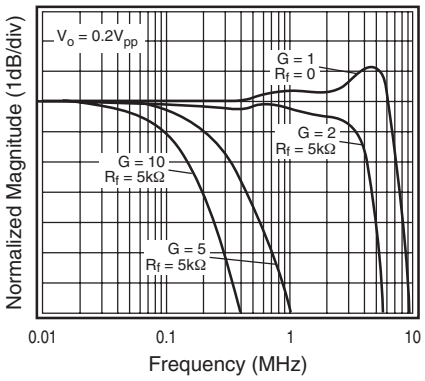
Package Thermal Resistance

Package	θ_{JA}
8 lead SOIC	152°C/W
8 lead MSOP	206°C/W

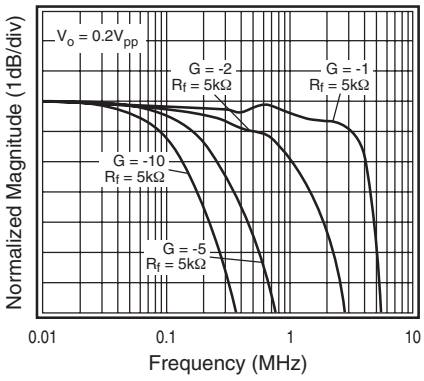
Typical Operating Characteristics

(V_S = +5V, G = 2, R_L = 10kΩ to V_S/2, R_f = 5kΩ, T_a = 25°C; unless otherwise noted)

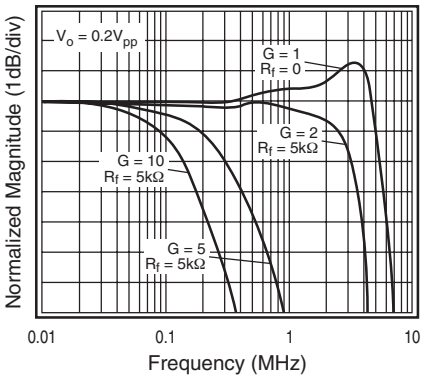
Non-Inverting Freq. Response V_s = +5V



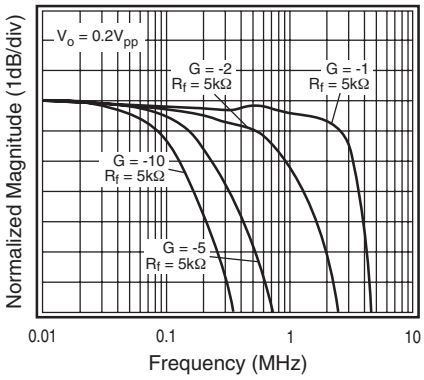
Inverting Freq. Response V_s = +5V



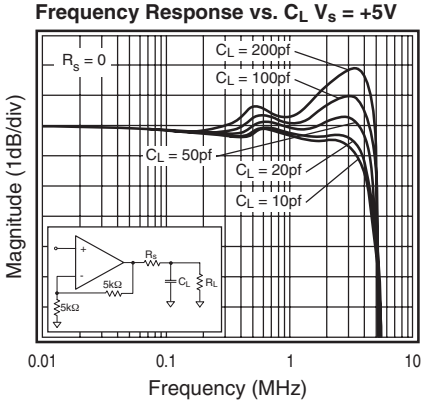
Non-Inverting Freq. Response V_s = +2.7V



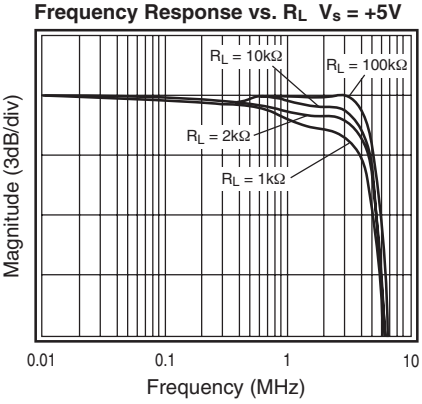
Inverting Freq. Response V_s = +2.7V



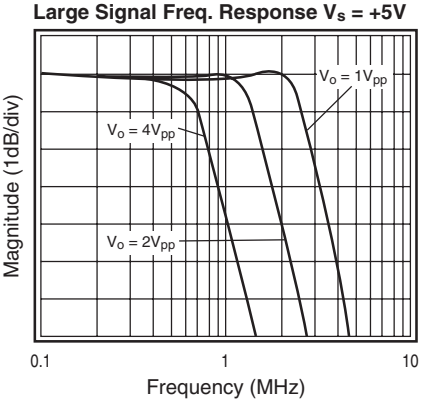
Frequency Response vs. C_L V_s = +5V



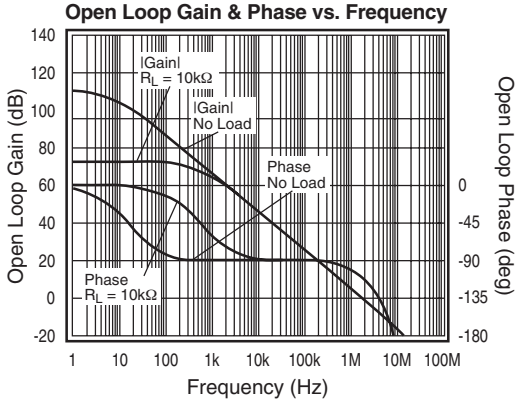
Frequency Response vs. R_L V_s = +5V



Large Signal Freq. Response V_s = +5V



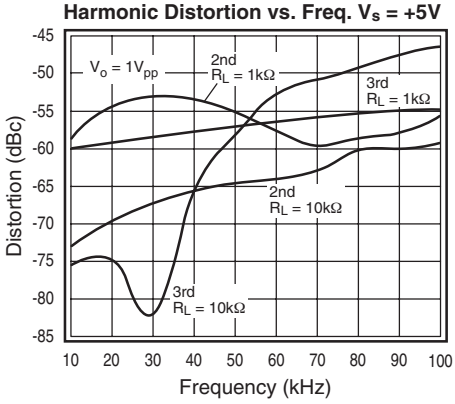
Open Loop Gain & Phase vs. Frequency



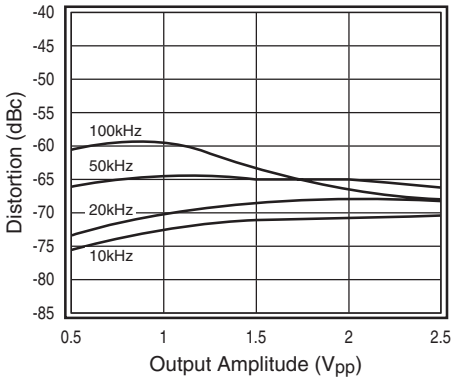
Typical Operating Characteristics

(V_S = +5V, G = 2, R_L = 10kΩ to V_S/2, R_f = 5kΩ, T_a = 25°C; unless otherwise noted)

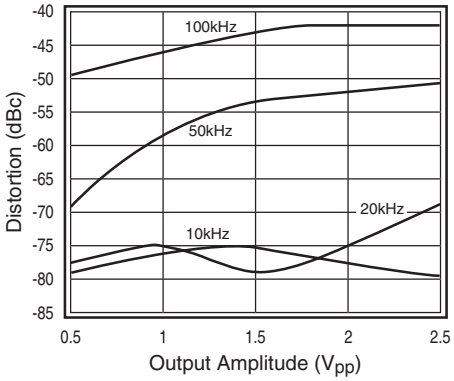
Harmonic Distortion vs. Freq. V_s = +5V



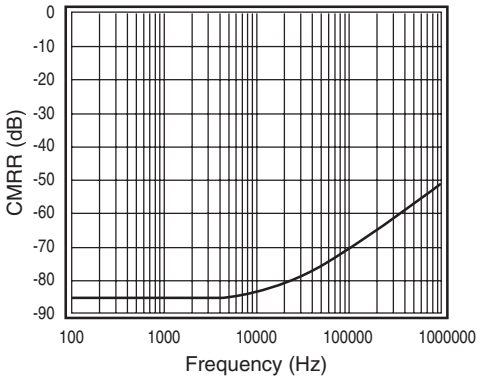
2nd Harmonic Distortion vs. V_o for V_s = +5V



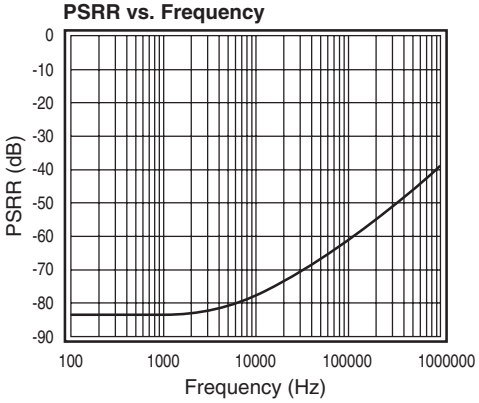
3rd Harmonic Distortion vs. V_o for V_s = +5V



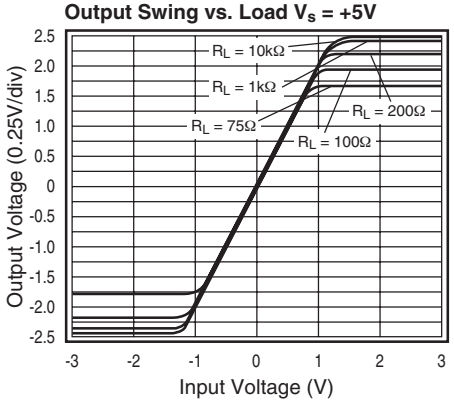
CMRR vs. Frequency



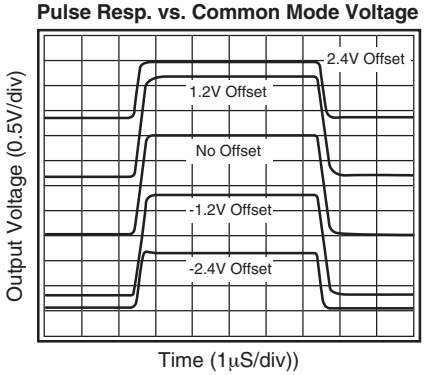
PSRR vs. Frequency



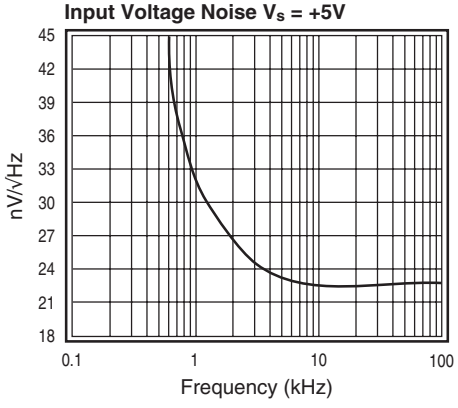
Output Swing vs. Load V_s = +5V



Pulse Resp. vs. Common Mode Voltage

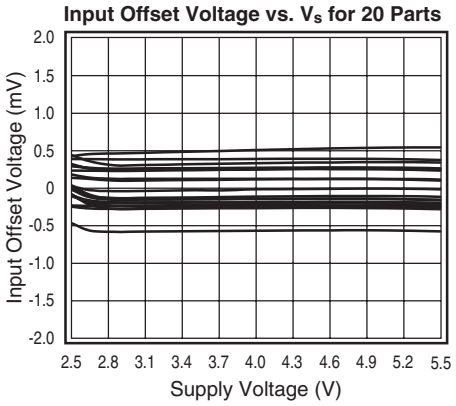


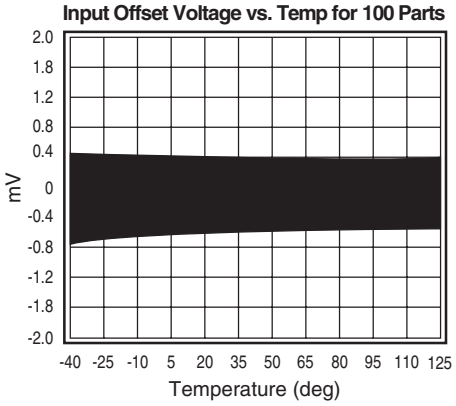
Input Voltage Noise V_s = +5V



Typical Operating Characteristics

(V_S = +5V, G = 2, R_L = 10kΩ to V_S/2, R_f = 5kΩ, T_a = 25°C; unless otherwise noted)





Application Information

General Description

The FAN4272 is single supply, general purpose, voltage-feedback amplifier. The FAN4272 is fabricated on a complementary bipolar process, features a rail-to-rail input and output, and is unity gain stable.

The typical non-inverting circuit schematic is shown in Figure 1.

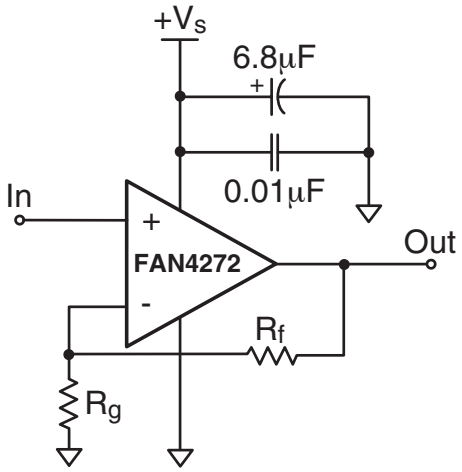


Figure 1: Typical Non-inverting Configuration

Input Common Mode Voltage

The common mode input range extends to 250mV below ground and to 250mV above V_S, in single supply operation. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition. If the absolute maximum input voltage (700mV beyond either rail) is exceeded, externally limit the input current to ±5mA as shown in Figure 2.

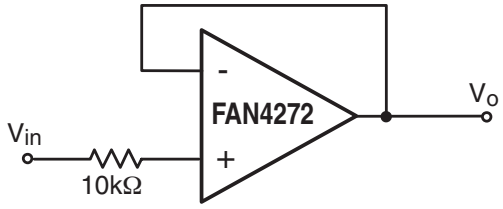


Figure 2: Circuit for Input Current Protection

Power Dissipation

The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C, some performance degradation will occur. It the maximum junction temperature exceeds 175°C for an extended time, device failure may occur.

Overdrive Recovery

Overdrive of an amplifier occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FAN4272 will typically recover in less than 50ns from an overdrive condition. Figure 3 shows the FAN4272 in an overdriven condition.

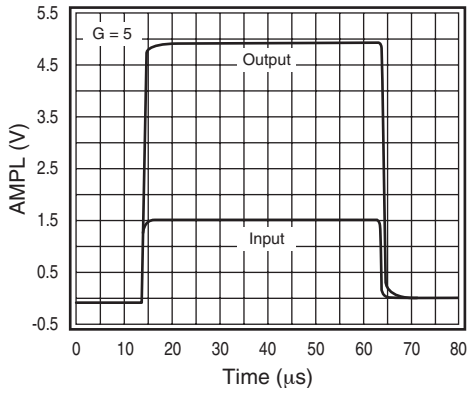


Figure 3: Overdrive Recovery

Driving Capacitive Loads

The ***Frequency Response vs. C_L*** plot, illustrates the response of the FAN4272. A small series resistance (R_S) at the output of the amplifier, illustrated in Figure 4, will improve stability and settling performance. R_S values in the ***Frequency Response vs. C_L*** plot were chosen to achieve maximum bandwidth with less than 2dB of peaking. For maximum flatness, use a larger R_S. Capacitive loads larger than 200pF require the use of R_S.

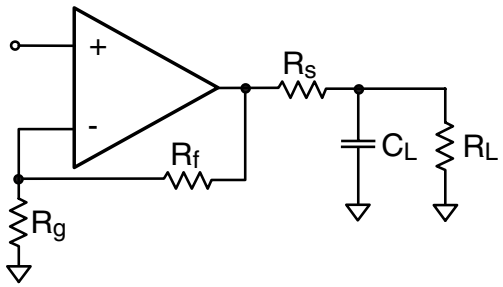


Figure 4: Typical Topology for driving a capacitive load

Driving a capacitive load introduces phase-lag into the output signal, which reduces phase margin in the amplifier. The unity gain follower is the most sensitive configuration. In a unity gain follower configuration, the FAN4272 requires a 75Ω series resistor to drive a 100pF load.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. Fairchild has evaluation boards to use as a guide for high frequency layout and as aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.01µF ceramic capacitors
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.01µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts shown in Figure 6 for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of this device:

Eval Bd	Description	Products
KEB006	Dual Channel, Dual Supply, 8 lead SOIC	FAN4272AM8
KEB010	Dual Channel, Dual Supply, 8 lead MSOP	FAN4272AMU8

Evaluation board schematics and layouts are shown in Figure 5 and Figure 6.

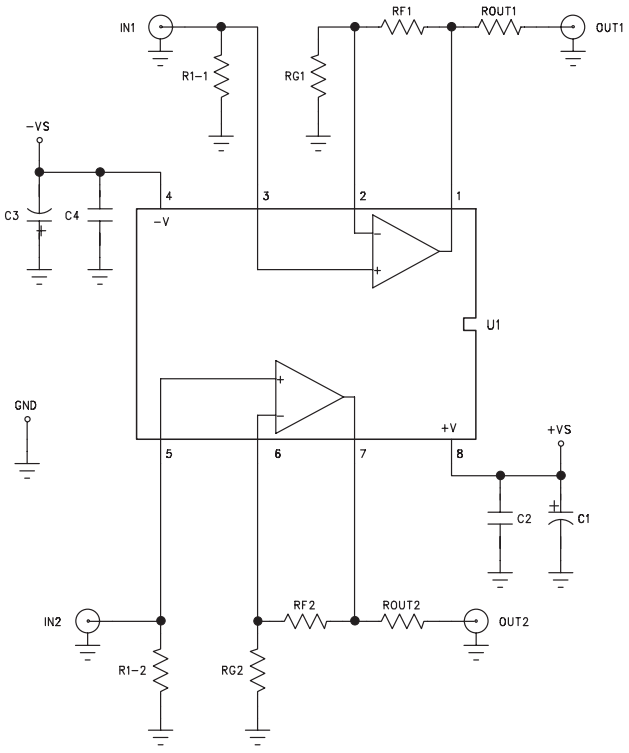


Figure 5: Evaluation Board Schematic

FAN4272 Evaluation Board Layout

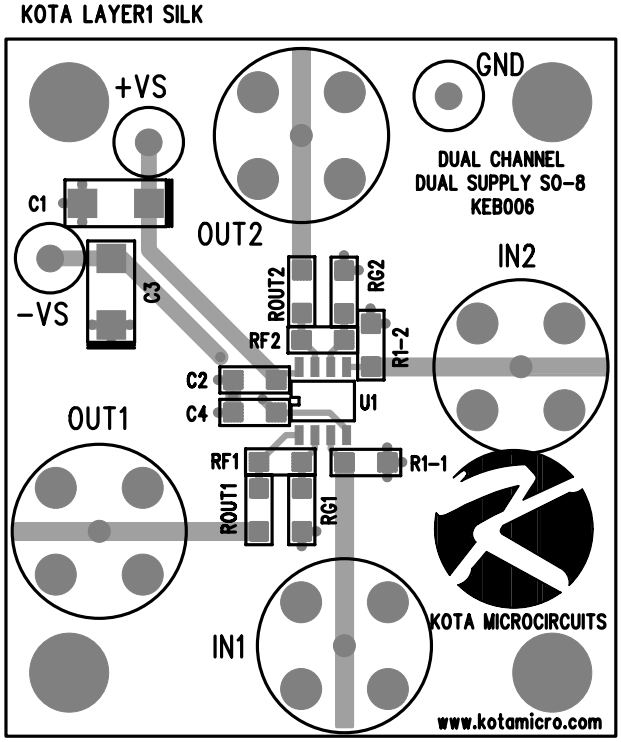


Figure 6a: KEB006 (top side)

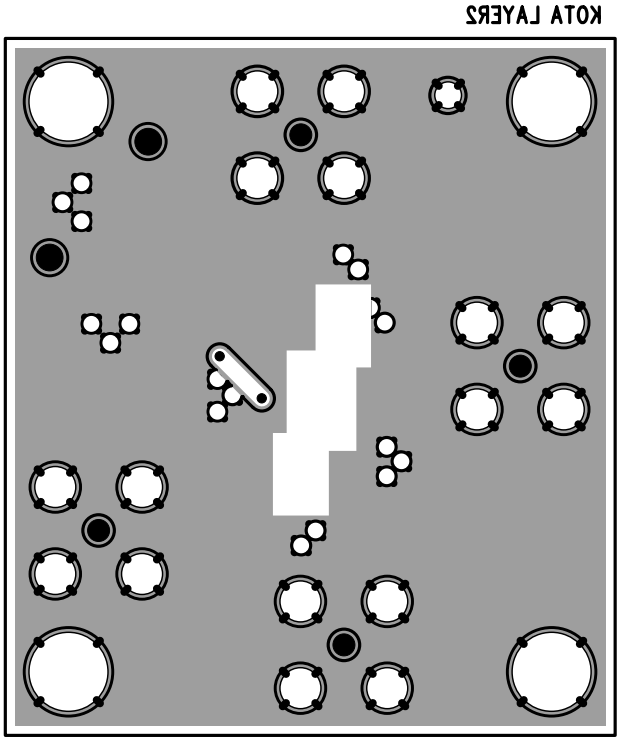


Figure 6b: KEB006 (bottom side)

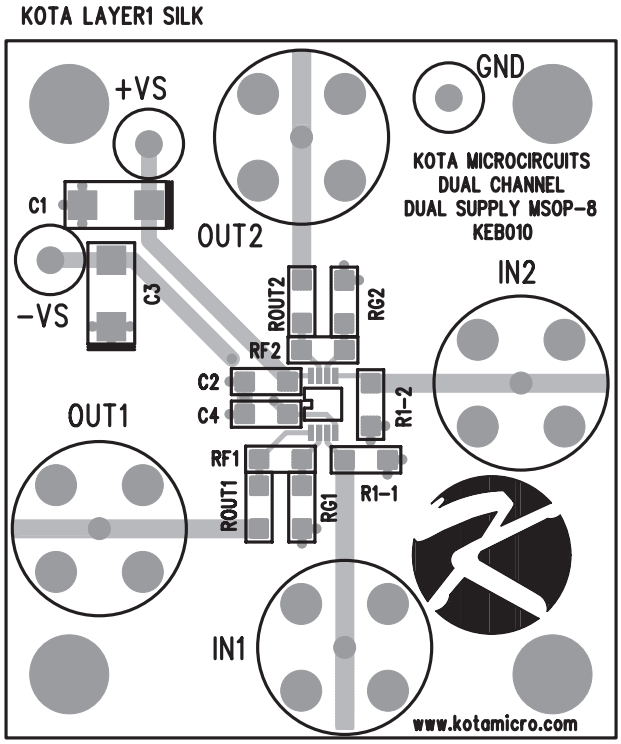


Figure 6c: KEB010 (top side)

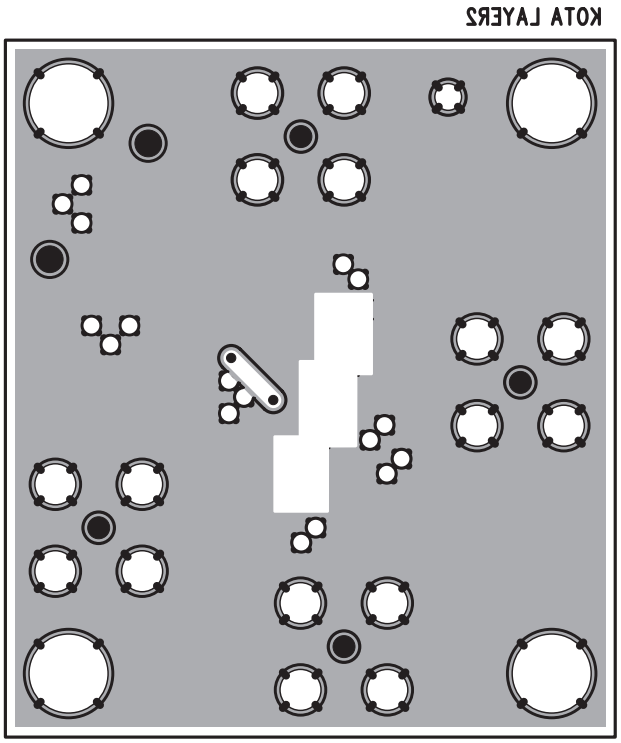
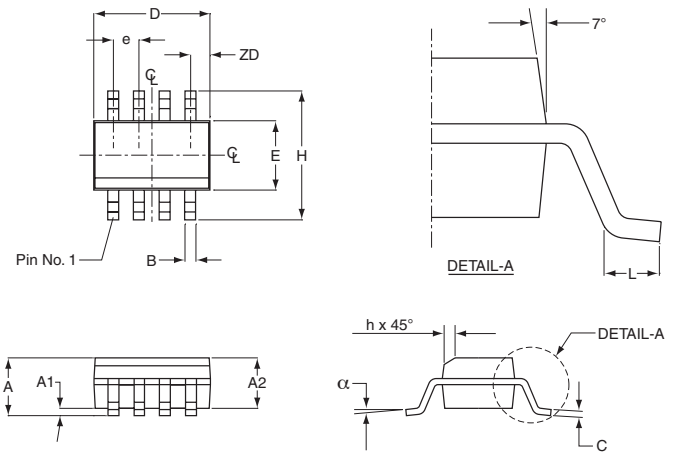


Figure 6d: KEB010 (bottom side)

FAN4272 Package Dimensions

SOIC

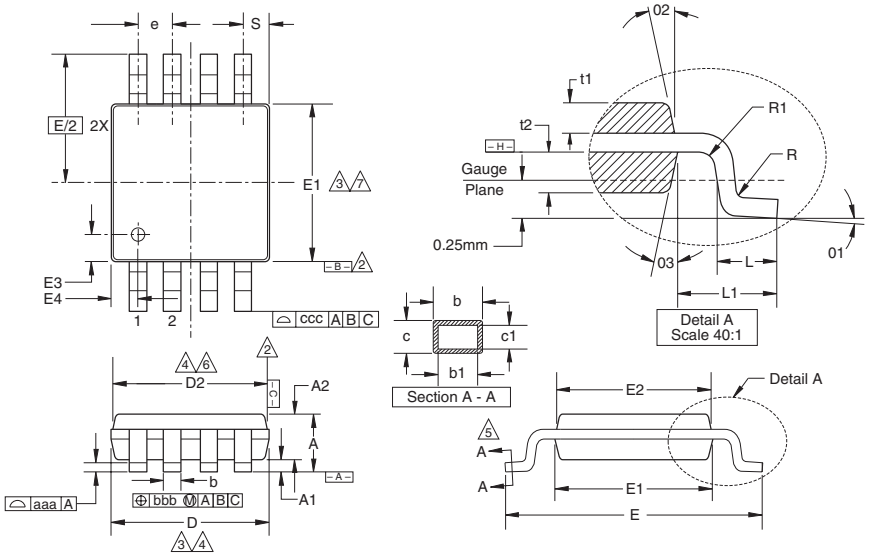


SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.41	1.27
A	1.52	1.72
	0°	8°
ZD	0.53 ref	
A2	1.37	1.57

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.10mm (.004") max.
3. Package surface finishing:
   (2.1) Top: matte (charmilles #18~30).
   (2.2) All sides: matte (charmilles #18~30).
   (2.3) Bottom: smooth or matte (charmilles #18~30).
4. All dimensions excluding mold flashes and end flash from the package body shall not exceed o.152mm (.006) per side(d).

MSOP



MSOP-8		
SYMBOL	MIN	MAX
A	1.10	–
A1	0.10	±0.05
A2	0.86	±0.08
D	3.00	±0.10
D2	2.95	±0.10
E	4.90	±0.15
E1	3.00	±0.10
E2	2.95	±0.10
E3	0.51	±0.13
E4	0.51	±0.13
R	0.15	+0.15/-0.06
R1	0.15	+0.15/-0.06
t1	0.31	±0.08
t2	0.41	±0.08
b	0.33	+0.07/-0.08
b1	0.30	±0.05
c	0.18	±0.05
c1	0.15	+0.03/-0.02
01	3.0°	±3.0°
02	12.0°	±3.0°
03	12.0°	±3.0°
L	0.55	±0.15
L1	0.95 BSC	–
aaa	0.10	–
bbb	0.08	–
ccc	0.25	–
e	0.65 BSC	–
S	0.525 BSC	–

NOTE:

1 All dimensions are in millimeters (angle in degrees), unless otherwise specified.

2 Datums –B– and –C– to be determined at datum plane –H–.

3 Dimensions "D" and "E1" are to be determined at datum –H–.

4 Dimensions "D2" and "E2" are for top package and dimensions "D" and "E1" are for bottom package.

5 Cross sections A – A to be determined at 0.13 to 0.25mm from the leadtip.

6 Dimension "D" and "D2" does not include mold flash, protrusion or gate burrs.

7 Dimension "E1" and "E2" does not include interlead flash or protrusion.

Ordering Information

Model	Part Number	Package	Container	Pack Qty
FAN4272	FAN4272AM8X	SOIC-8	Reel	2500
FAN4272	FAN4272AMU8X	MSOP-8	Reel	3000

Temperature range for all parts: -40°C to +125°C.