FAN3506

PC SMPS Secondary Side Control IC

Features

- Few External Components
- Low Voltage Operation (Vcc_min=4.5V)
- Over Voltage Protection for 3.3V/5V/12V Output
- Two Protection Inputs (PT1, PT2)
- Fault Protection Output with Open Collector
- Power Supply on/off Delay Time Control (PSON)
- Latch Function Controlled by PSON and Protection
- Power Good Signal Generator with Hysteresis
- 300ms(Typ) Power Good Delay
- Programmable Shunt Regulator Trimmed to ±2%
- 16-Pin Dual In-line Package (16-DIP-300)

Description

The FAN3506 is complete housekeeping circuitry for use in the secondary side of PC SMPS (Switched Mode Power Supply). It contains various functions, which are over voltage protection including two extra protection inputs, power supply on/off delay control and power good signal generator. Especially, it contains a programmable shunt regulator for output feedback and the reference voltage is trimmed to ±2%. The FAN3506 is available in 16-DIP.

16-DIP

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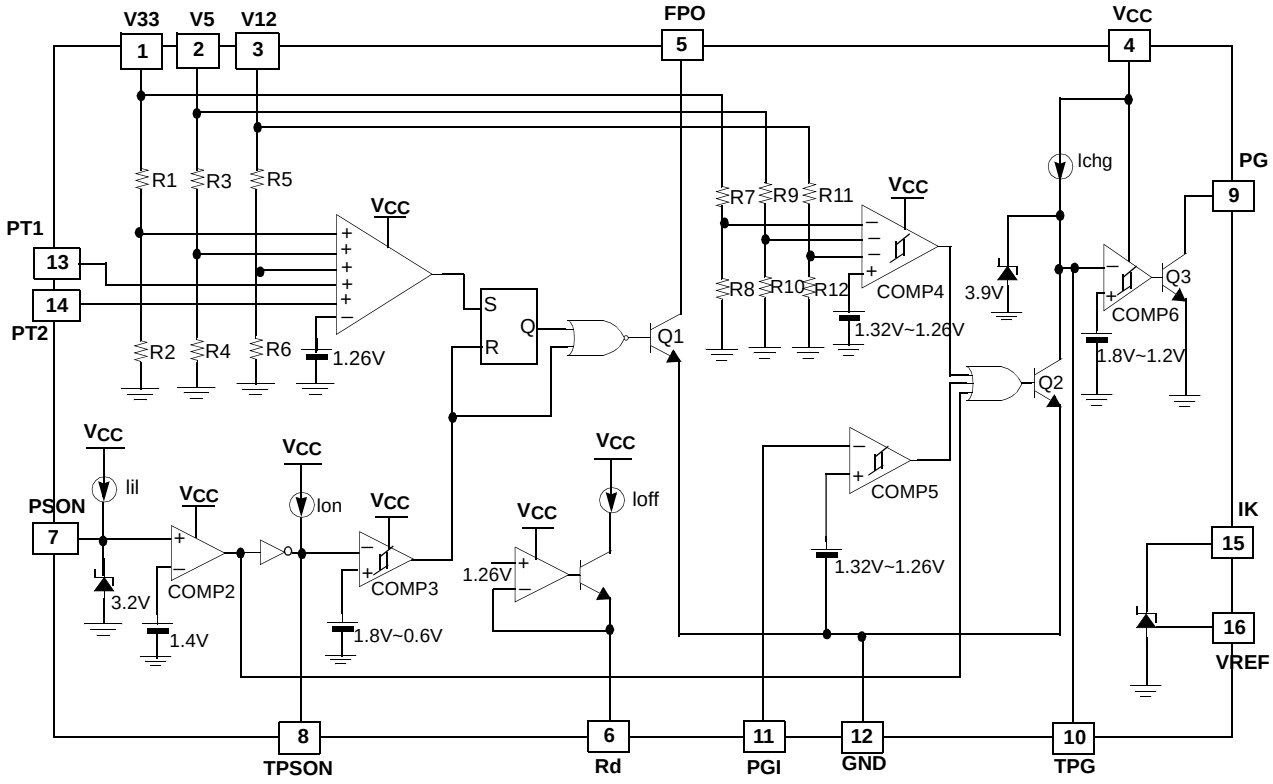
Block Diagram



Rev. 1.0.2

Pin Description

No	Name	I/O	Function
1	V33	I	+3.3V Output Voltage of SMPS Secondary Side
2	V5	I	+5V Output Voltage of SMPS Secondary Side
3	V12	I	+12V Output Voltage of SMPS Secondary Side
4	V_{CC}	I	Supply Voltage. +5Vsb(+5V Standby Supply) is Recommended for Vcc. The Operating Range is 4.5V~15V. Vcc=5V, Ta=25°C at test.
5	FPO	O	Fault Protection Output(FPO) With Open Collector Structure. This Signal Controls the Primary Switch(PWM IC) Through an Opto-coupler. Maximum Current Rating is 20mA. When FPO = "Low", the Main SMPS is Operational and if FPO = "High", the Main SMPS is Turned-off.
6	Rd	-	OFF Delay Resistor. This Block is Made up of a Buffer With Vout = 1.258V. A Resistor Should be Connected to the Pin6 for Determination of Off Delay Current. The Recommended Value of Rd Resistor is 28kΩ at Ctpson=0.22uF. The off Delay Time is Gotten by Following Equation. Toff = [Ctpson * (V8max-VthL)] / (1.258V/Rrd)
7	PSON	I	Power Supply On/Off (Remote On/Off) Input. It is TTL Operation and its Threshold Voltage is 1.4V. The Maximum Voltage of Pin7 is About 3.9V(Typ), With ABsolutely Maximum Voltage, 5.25v. If Pson Is Low, Fpo Is Low, Too. That Means The main SMPS is Operation(Active). When PSON is High, then FPO is High and the Main SMPS is off.
8	TPSON	-	Power Supply On/Off Delay. Ton/Toff = 24ms/8ms(Typ) with Ctpson=0.22uF & Rd=28kΩ. Its High/Low Threshold Voltages 1.8V/0.6V and the Maximum Voltage After Full Charging is About 2.2V. So Vcharge = VthH = 1.8V and Vdischg = V8max - VthL = 1.6V. Each Delay Time is Decided by the Following Equations, Ton = (Ctpson*VthH) / Ion, Toff = [Ctpson*(V8max-VthL)] / (Vrd/Rrd) .
9	PG	O	Power Good Signal Output with Open Collector. The Maximum Current Rating is 20mA. PG High Means that the Power is Good for Operation and PG low Means Power Fail.
10	TPG	-	PG Delay. Td = 300ms(Typ) with Ctpg=2.2uF. The Threshold Voltage is 1.8V and the Delay Time is Decided by the Following Equation, Td = (Ctpg * Vth) / Ichg = 1.8Ctpg / Ichg.
11	PGI	I	Power Good Signal Input. Its Threshold Voltage is 1.26V When the PGI Voltage Drops From High to Low.
12	GND	-	Ground
13	PT1	I	Protection Input 1. This can be Used for an Adjustable OVP or Another Protection Input.
14	PT2	I	Protection Input 2. This can be Used for an Adjustable OVP or Another Protection Input.
15	IK	I	Cathode of the Programmable Shunt Regulator. Absolute Min/Max Current Rating is 1mA/30mA.
16	V_{REF}	I	Reference of Programmable Shunt Regulator. This Circuit is Prepared for Feedback of Output Voltage as it Equals to KA431(LM431). It is Trimmed to ±2%.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	4.5 ~ 15	V
FPO (Fault Protection Output) Voltage	VFPO	20	V
FPO Maximum Current	IFPO	20	mA
PGI Maximum Voltage	Vpgi	20	V
PG Output Maximum Current	Io(PG)	20	mA
Cathode Voltage	Vka	20	V
Cathode Current for IK	IK	1 ~ 30	mA
Power Dissipation	P_D	1	W
Operating Temperature Range	T_{OPR}	-25 ~ +80	ºC
Storage Temperature	T_{STG}	-65 ~ +150	ºC

Electrical Characteristics

(V_{CC} = 5V, T_a = 25ºC, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
PROTECTION SECTION						
OVP Detecting Voltage for 3.3V	$V_{OVP}33$	PSON=0V	3.9	4.1	4.3	V
OVP Detecting Voltage for 5V	$V_{OVP}5$	PSON=0V	5.7	6.1	6.5	V
OVP Detecting Voltage for 12V	$V_{OVP}12$	PSON=0V	13.6	14.3	15.0	V
Protection Input Voltage 1	$V_{pt}1$	PSON=0V	1.21	1.26	1.31	V
Protection Input Voltage 2	$V_{pt}2$	PSON=0V	1.21	1.26	1.31	V
POWER SUPPLY ON/OFF SECTION (PSON)						
PSON Input Threshold Voltage	V_{th}	PSON=0V : 0V to 2V	1	1.4	1.8	V
PSON Input Open Voltage	V_{ih}	PSON : Open	2	-	5.25	V
PSON Input Low Current	Iil	PSON=0V	0	-	-1	mA
PSON Delay Charging Current	Ion	PSON=TPSON=0V	-10	-16	-24	uA
Buffer Output Voltage	VRd	Isink=45uA, 200uA	1.21	1.26	1.31	V
Pin8 Clamping Voltage	V_{8max}	PSON=0V	2.0	2.2	2.4	V
High Threshold for On/Off Delay (Note1)	VthH	TPSON : 0V to 2.2V	1.6	1.8	2.0	V
Low Threshold for On/Off Delay (Note2)	VthL	TPSON : 2.2V to 0V	0.4	0.6	0.8	V
Power Supply ON Delay Time (Note3)	Ton	Cpin8=0.22µF, Rd=28kΩ	16	26	36	msec
Power Supply OFF Delay Time (Note4)	Toff	Cpin8=0.22µF, Rd=28kΩ	4	8	14	msec
FPO Saturation Voltage	V_{sat}(FPO)	Io=10mA	-	0.2	0.4	V
FPO Leakage Current	Ileak(FPO)	FPO=20V	0	0.01	1	uA

Electrical Characteristics (Continued)

(V_{CC}= 5V, T_a = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
POWER GOOD SECTION						
PGI Threshold Voltage	V_{pgi}	PGI : 1.5V to 1V	1.21	1.26	1.31	V
V33 Under Voltage Level	$V_{uv}33$	V33 : 3.3V to 2V	2.66	2.8	2.94	V
V5 Under Voltage Level	$V_{uv}5$	V5 : 5V to 3.5V	4.1	4.3	4.5	V
V12 Under Voltage Level	$V_{uv}12$	V12 : 12V to 9V	9.8	10.3	10.8	V
Pin10 Clamping Voltage	$V10_{max}$	TPG : Open	3.4	3.9	4.4	V
PG Delay Comparator Threshold Voltage	Vth(TPG)	TPG : 0V to 2.5V	1.5	1.8	2.1	V
PG Delay Comparator Hysteresis Voltage	HY	TPG : 2.5V to 0V	0.3	0.6	0.9	V
Charging Current for PG Delay	Ichg	TPG = 0V	-9	-15	-23	uA
PG Delay Time	Td(PG)	Cpin10 = 2.2uF	100	300	500	msec
PG Output Rising Time (Note5)	Tr	Cpin9 = 0.1uF	-	1	-	usec
PG Output Falling Time (Note6)	Tf	Cpin9 = 0.1uF	-	1	-	usec
PG Output Saturation Voltage	Vsat(PG)	Isink = 15mA	-	0.2	0.4	V
PG Output Leakage Current	Ileak(PG)	V(PG) = 20V	0	0.01	1	uA
PROGRAMMABLE SHUNT REGULATOR (KA431) SECTION						
Reference Input Voltage	V_{ref}	IK = V_{REF}, IK = 1mA	2.45	2.50	2.55	V
Load Regulation	Vref	IK = 1mA to 10mA	-	5	15	mV
Temperature Stability (Note7)	ΔVref/ΔT	Ta = -25 ~ +85°C	-	4.5	17	mV
Output Sinking Current Capability	Isink	-	10	25	-	mA
Gain Bandwidth (Note8)	GBW	GV = 1	-	1	-	MHz
TOTAL DEVICE						
Supply Current	Icc	PSON = 2V	-	3	8	mA

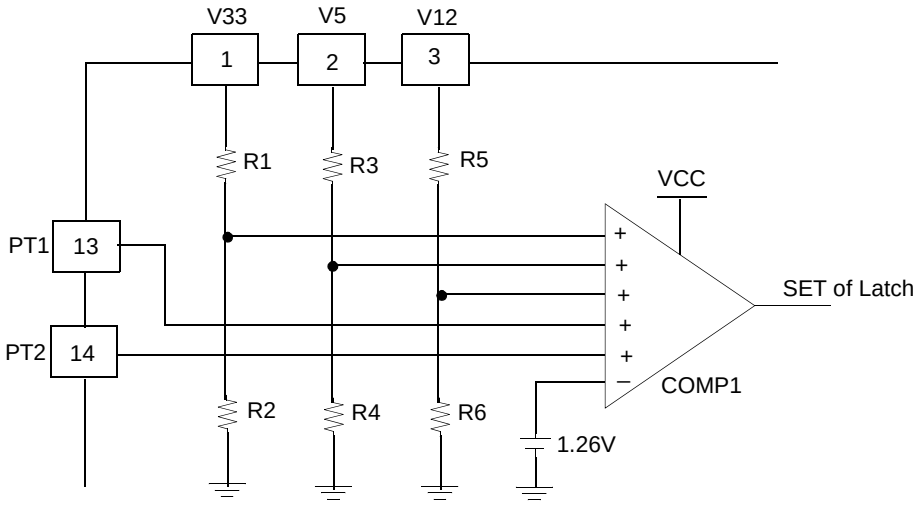
Note :

1. Power Supply ON Delay (PSON :High → Low). Power Supply is Active when PSON is Low.
2. Power Supply OFF Delay (PSON :Low → High). Power Supply is Off when PSON is High.
3. Ton = (Cpin8 * Von) / Ion = (Cpin8 * VthH) / Ion
4. Toff = (Cpin8 * Voff) / Ioff = [Cpin8 * (V8max - VthL)] / (VRd / Rd)

5,6,7,8 : These parameters, although guaranteed, are but not 100% tested in production.

Block Description & Application Hints

1. OVP Block



OVP function is simply realized by connecting Pin1, Pin2, Pin3 to each secondary output. R1,2,3,4,5,6 are internal resistors of the IC. Each OVP level is determined by resistor ratio and the typical values are 4V/6.1V/14.2V.

- OVP Detecting voltage for +3.3V

  . Vovp33 = (R1+R2)/R2 * 1.26V = 4.1V(Typ)

- OVP Detecting voltage for +5V

  . Vovp5 = (R3+R4)/R4 * 1.26V = 6.1V(Typ)

- OVP Detecting voltage for +12V

  . Vovp12 = (R5+R6)/R6 * 1.26V = 14.3V(Typ)

Especially, Pin13 & Pin14 are prepared for extra OVP inputs or another protection signal, respectively. That is, if you want over voltage protection of extra output voltage, then you can make a function with two external resistors.

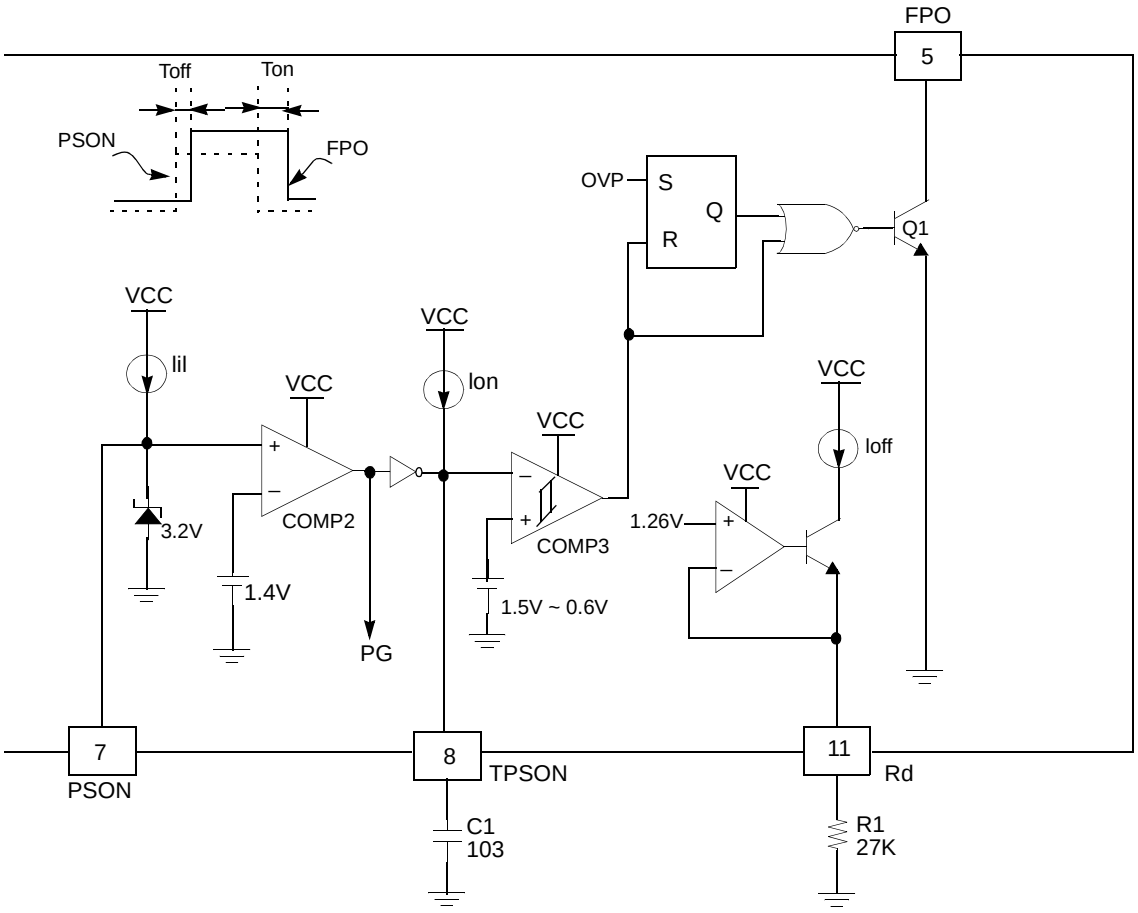
- Threshold Voltage of Protection Input 1 : Vpt1 = 1.26V

- Threshold Voltage of Protection Input 2 : Vpt1 = 1.26V

OVP function operates without delay time. In the case of OVP, system designer should know a fact that the main power can be dropped after a little time because of system delay, even if FPO is triggered by OVP.

So when the OVP level is tested with a set, you should check the secondary outputs(+3.3V/+5V/+12V) and FPO(Pin5) simultaneously. you can know the each OVP level as checking each output voltage in just time that FPO is triggered from low to high.

2. PSON & ON /OFF Delay Block



PSON & On/Off Delay Block is controlled by a Microprocessor.

If a high signal is supplied to the PSON(Pin7), the output of COMP2 becomes high status. The output signal is transferred to On/Off delay block and PG block.

If no signal is supplied to Pin7, Pin7 maintains high status(=3.2V) for the internal pull-up resistor.

When PSON is high, it produces FPO(Pin5) "High" signal after OFF delay time (about 8ms) for stabilizing system.

Then, all outputs (+3.3V, +5V, +12V) are grounded.

When PSON is changed to "Low", it produces FPO "Low" signal after ON delay time (about 26ms) for stabilizing the system.

If PSON is low, then FPO is low. That means the main SMPS is Active(operational). When PSON is high, FPO is high and the main SMPS is turned-off.

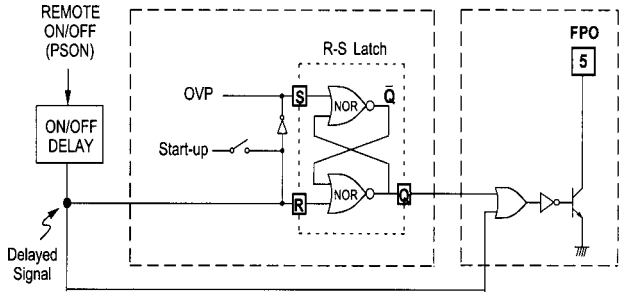
On/Off Delay Time can be calculated by following equation. 0.22uF Capacitor is recommended for following equations.

- Ton = (Ctpson*VthH)/Ion=(0.22uF*1.8V)/16uA = 26ms

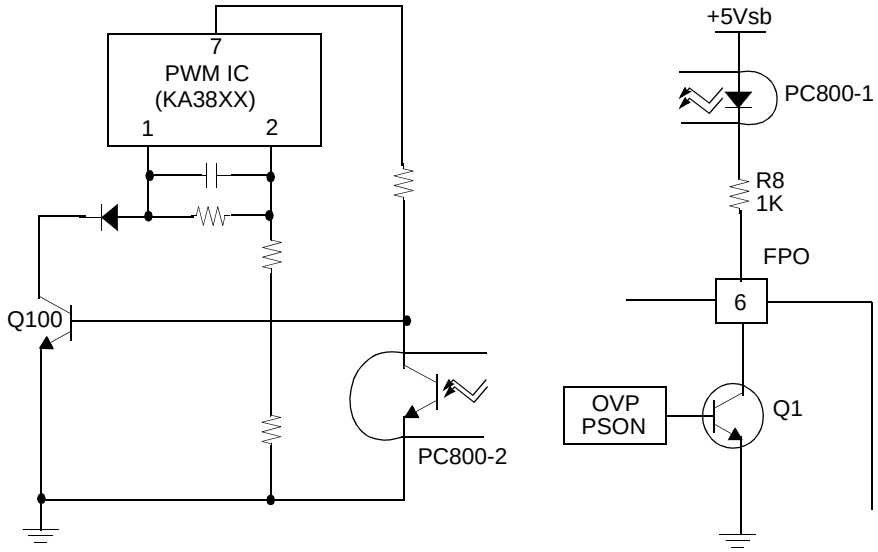
- Toff = [Ctpson*(V8max-VthL)] / Ioff = [Ctpson*(V8max-VthL)] / (VRd/Rd)

Because Ion current for charging is fixed by internal current source, On delay time is varied by the capacitor value. On the contrary, Off Delay time is decided by the Rd value. If the Rd is 27K(Recommended) and the Delay capacitor valuse is 0.22uF, Toff is 8ms(Typ).

3. Latch & FPO Output



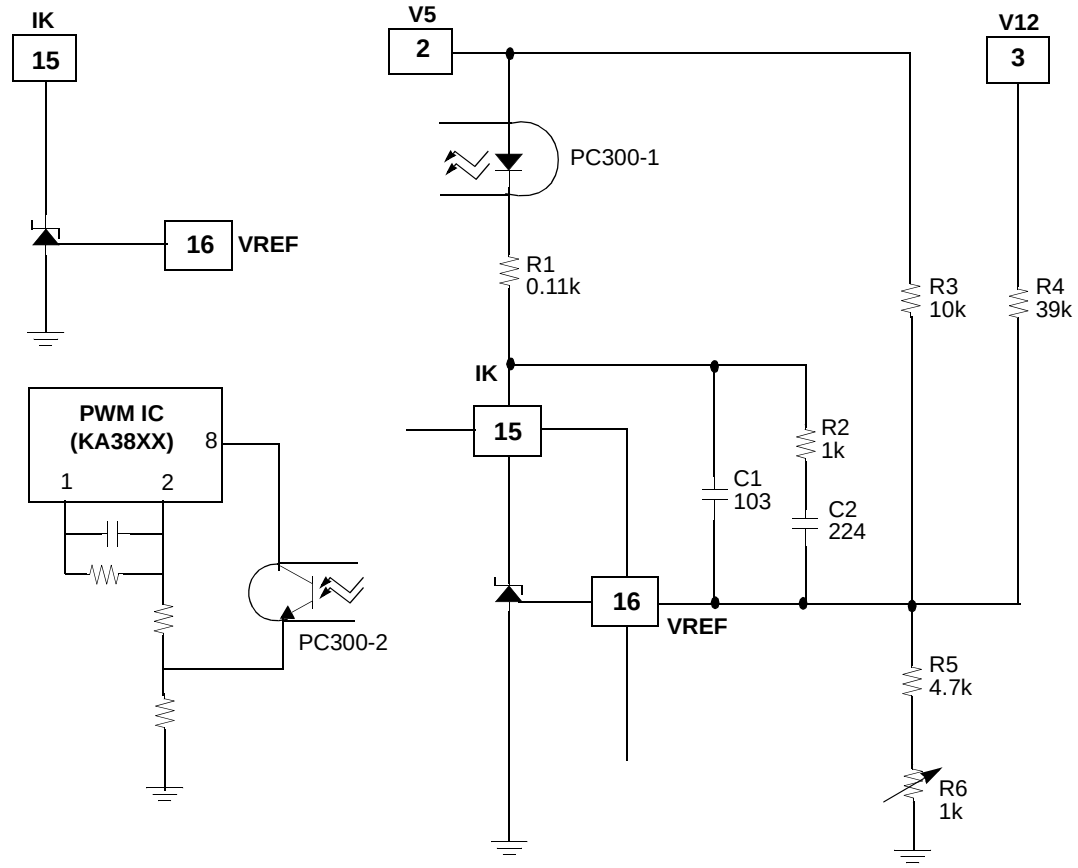
OVP	SET	RESET	Qn+1	$\overline{Qn+1}$
L	L	L	Qn	$\overline{Qn}$
L	L	H	L	H
H	H	L	H	L
H	H	H	L	H



Power Good Signal Generator circuits generate "On & Off" signal depending on the status of output voltage to prevent the malfunctions of following systems like microprocessor and etc. from unstable outputs at power on & off .
At Power On, it produces PG "High" signal after some delay (300ms_Typ) for stabilizing outputs.
At power Off, it produces PG "Low" signal without delay by sensing the status of power source for protecting following systems. COMP6 creates PG "Low" without delay when +5V output falls to less than 4.3V to prevent some malfunction at transient status, thus it improves system stability. FAN3506 detects the Under Voltage level of three outputs(+3.3V/+5V/+12V) and PGI, respectively.
- UV Deducing Level of +3.3V : Vuv33 = 2.8V(Typ)
- UV Deducing Level of +5V : Vuv5 = 4.3V(Typ)
- UV Deducing Level of +12V : Vuv12 = 10.3V(Typ)
- UV Deducing Level of PGI : Vpgi = 1.26V(Typ)

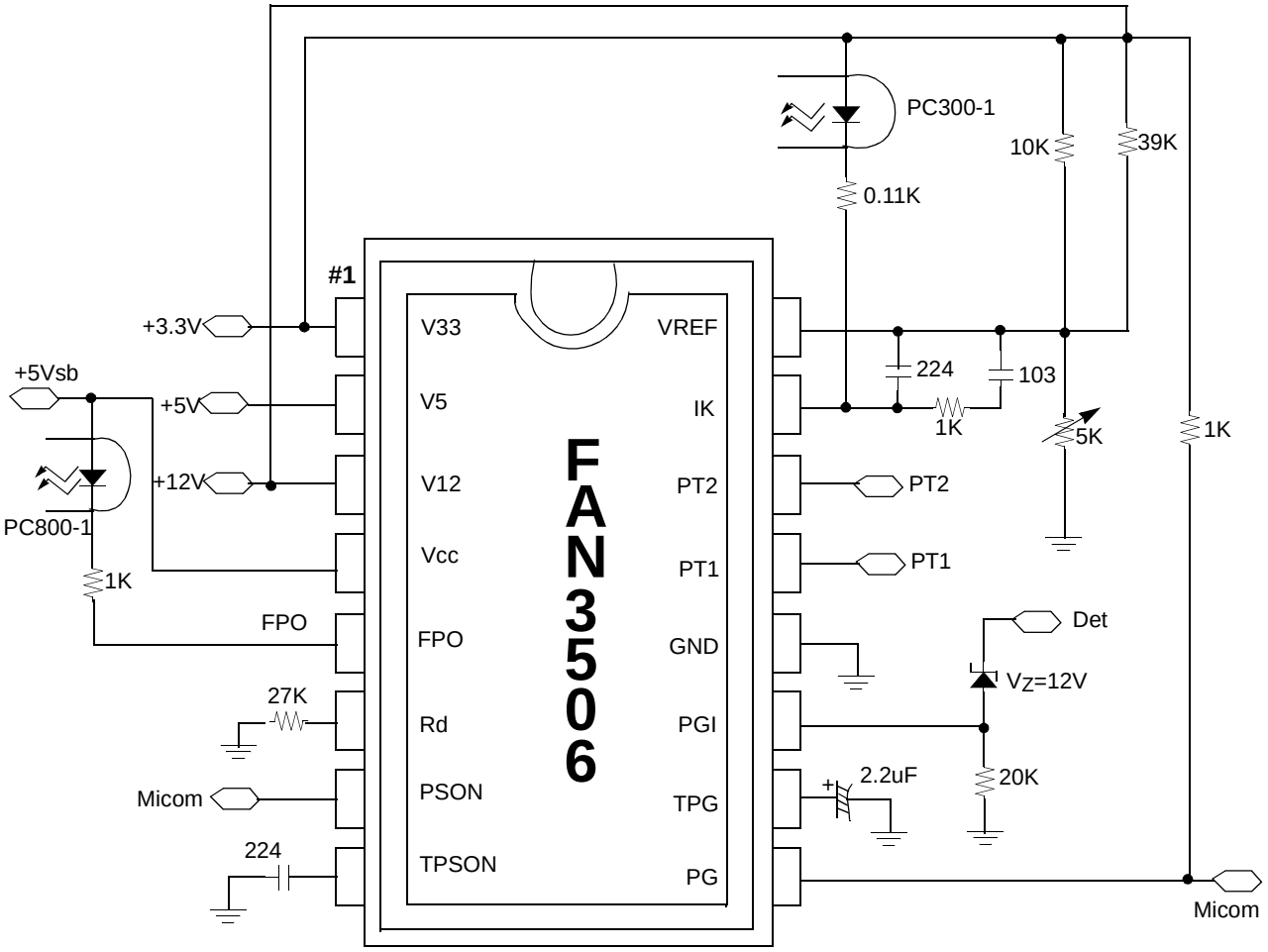
When PSON signal is high, it generates PG "Low" signal without delay. It means that PG becomes "Low" before main power is grounded. PG delay time(Td(PG)) is determined by capacitor value, threshold voltage of COMP6 and the charging current and its equation is as following.
Td(PG) = (Ctpg * VthH) / Ichg = 300ms(Typ)

4. Programmable Shunt Regulator

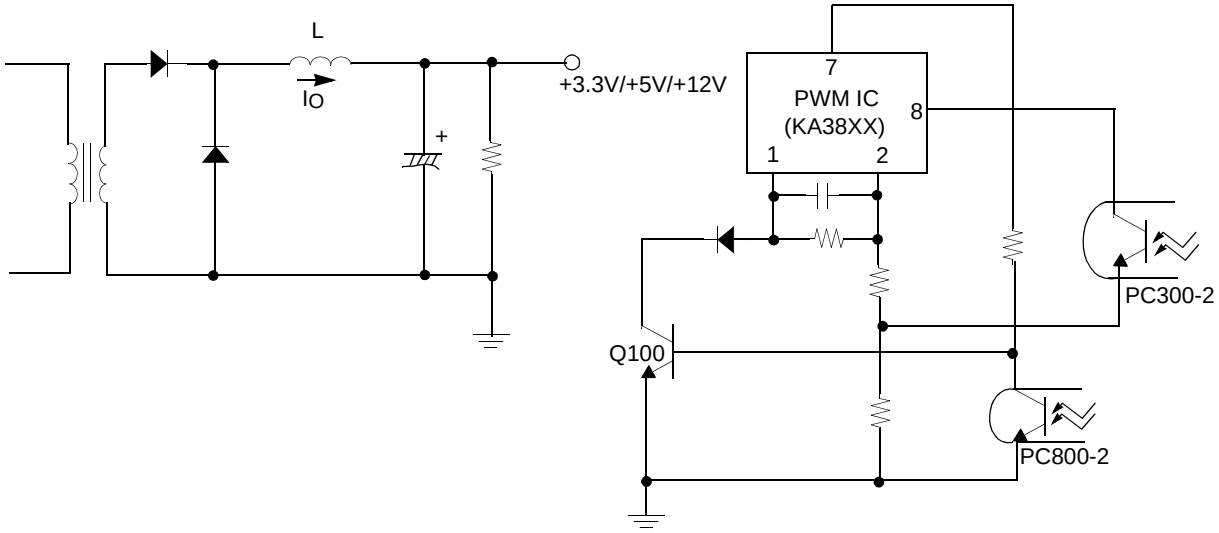


The core of the circuit equals to KA431(LM431) and Vref1 is trimmed to ±2% (2.45V ~ 2.55V) and it is for corrective output voltages (+5V/+12V). + 5V/ + 12V output voltages are determined by the resistor ratio of R3, R4, R5, R6.
A photo coupler is used in order to control PWM IC in the primary side. R1 determines the bias current of the shunt regulator and 110Ω is appropriate value. The resistor value can be changed by set condition and requirements.
C1 and R2 , C2 are the compensation circuit for stability.

Typical Application Circuit



[Complete Housekeeping Circuit using the FAN3506]



Typical Performance Characteristics

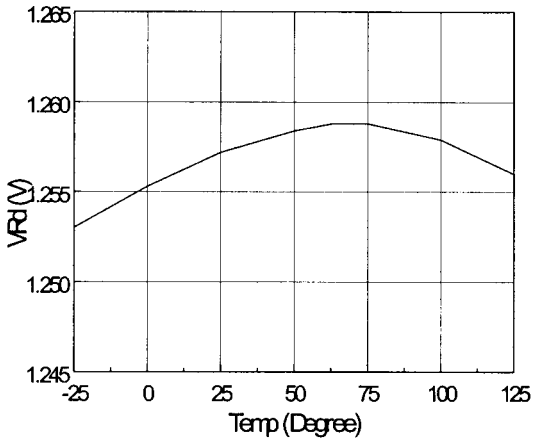


Figure 1. Temperature Stability for VRd

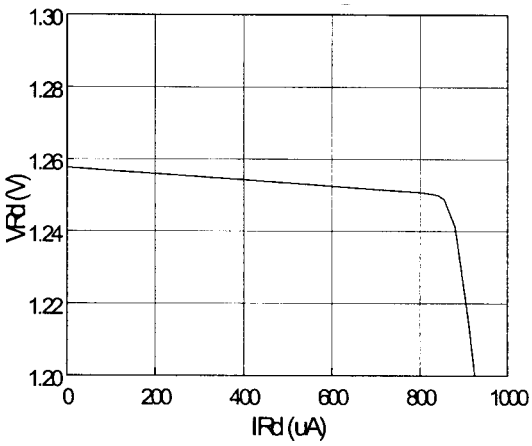


Figure 2. Buffer Output Voltage vs. IRd

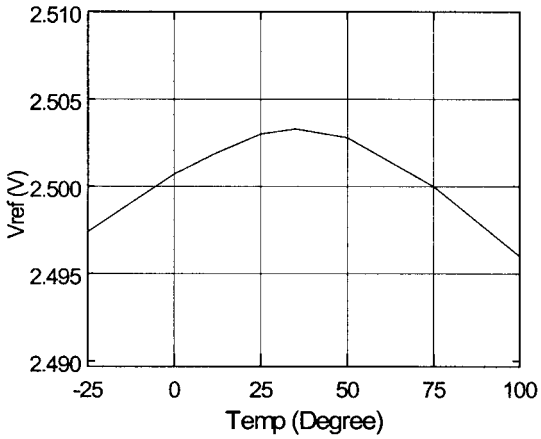


Figure 3. Temperature Stability for Vref

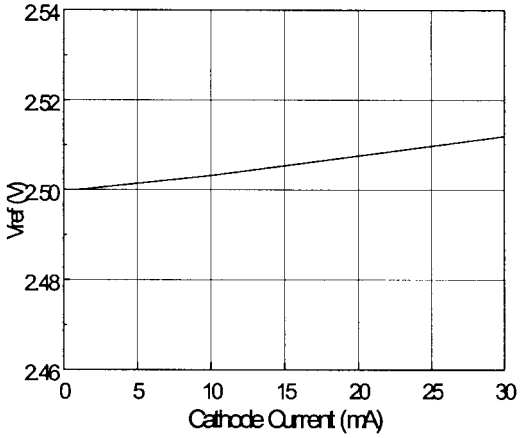


Figure 4. Current Stability of Vref

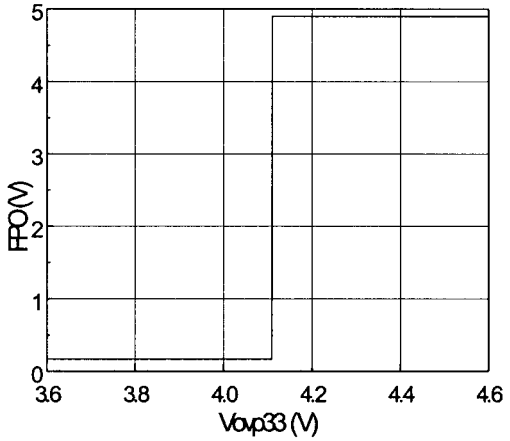


Figure 5. OVP Detecting Voltage for 3.3V

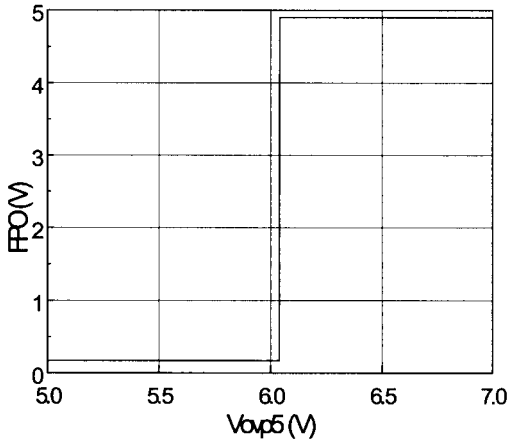


Figure 6. OVP Detecting Voltage for 5V

Typical Performance Characteristics (Continued)

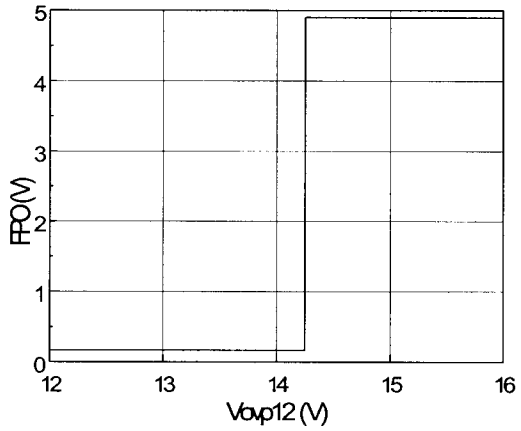


Figure 7. OVP Detecting Voltage for 12V

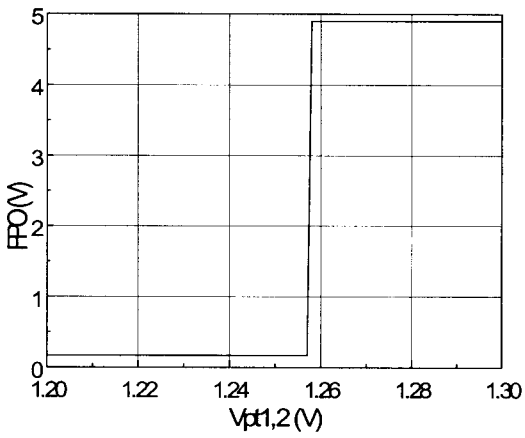


Figure 8. Protection Input Voltage 1,2

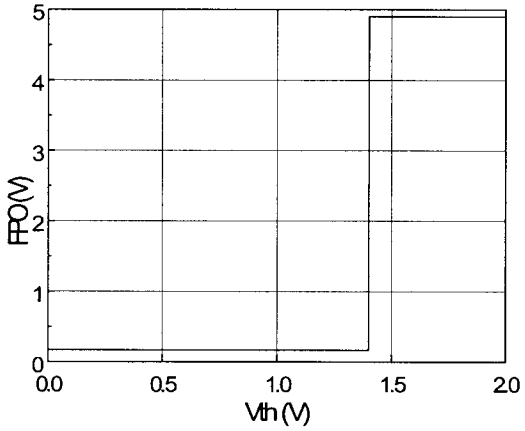


Figure 9. PSON Input Threshold Voltage

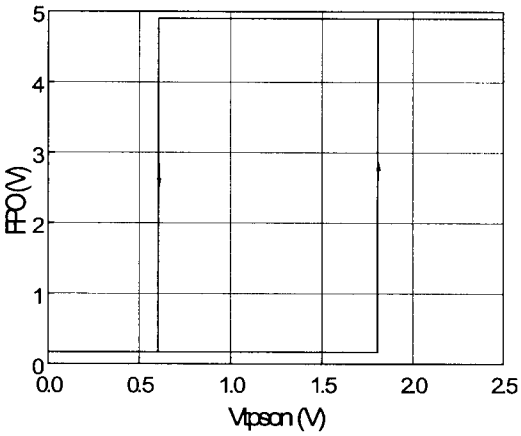


Figure 10. High/Low Threshold of On/Off Delay

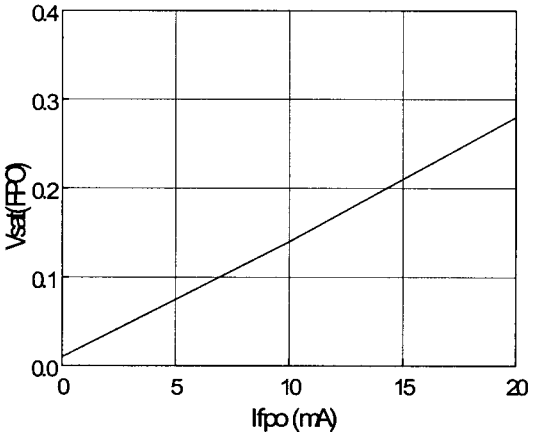


Figure 11. FPO Saturation Voltage

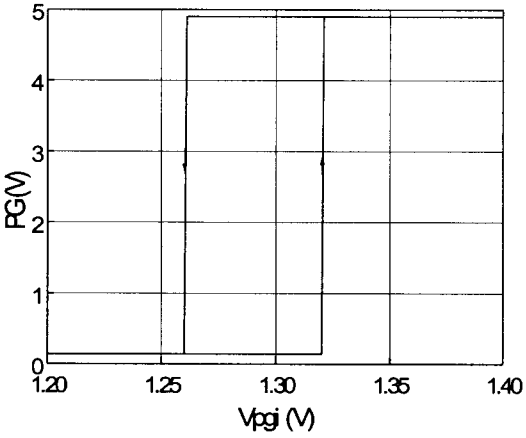


Figure 12. PGI Threshold Voltage

Typical Performance Characteristics (Continued)

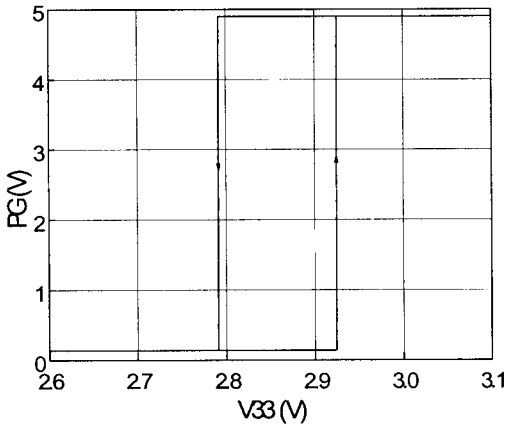


Figure 13. V33 Under Voltage Level

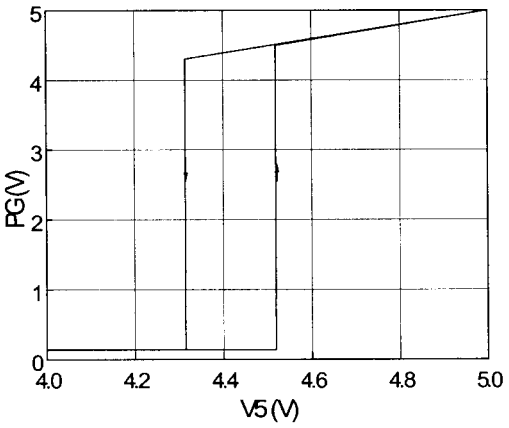


Figure 14. V5 Under Voltage Level

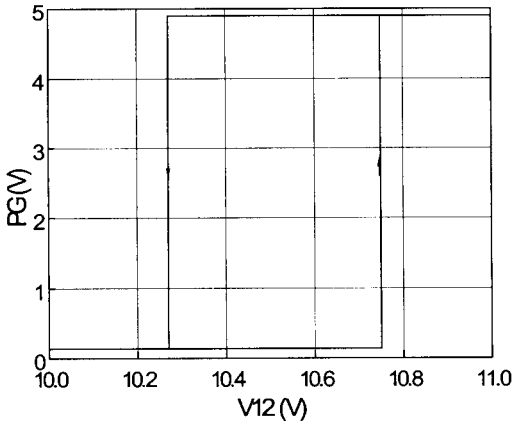


Figure 15. V12 Under Voltage Level

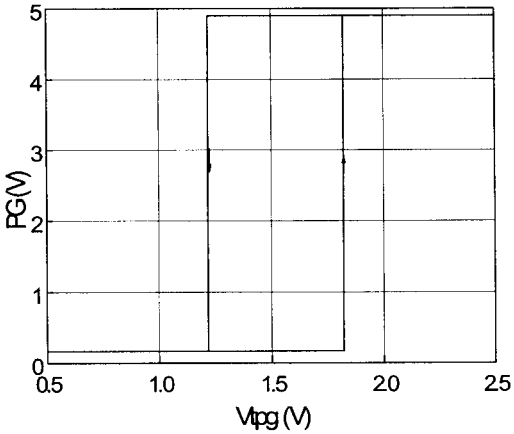


Figure 16. High/Low Threshold of PG Delay COMP

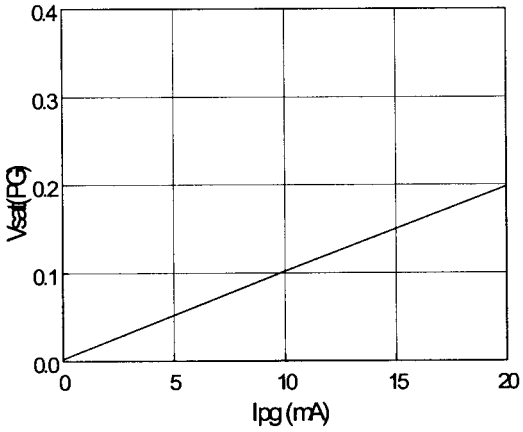


Figure 17. PG Saturation Voltage

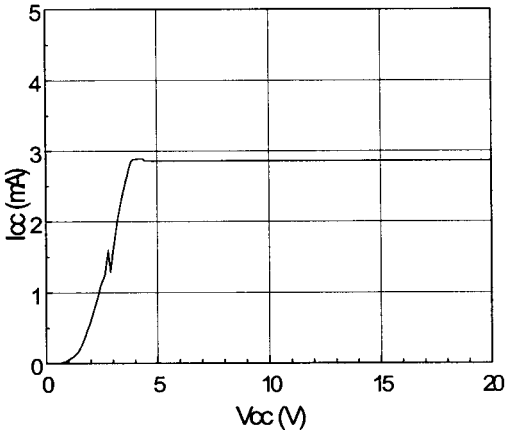


Figure 18. Supply Current of V_{CC}

Typical Performance Characteristics (Continued)

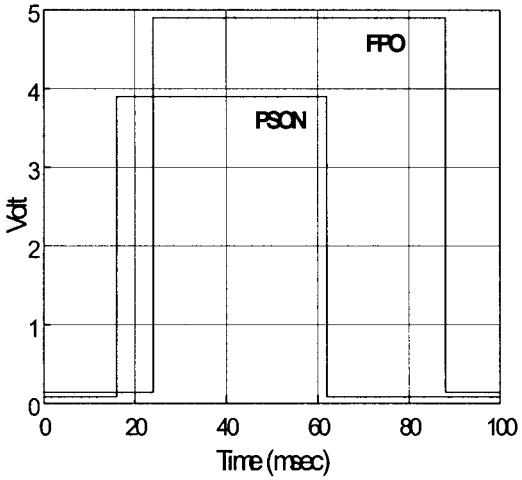


Figure 19. Power Supply On/Off Delay Time

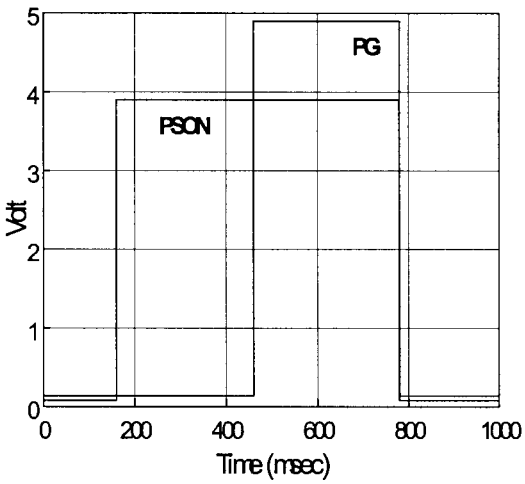


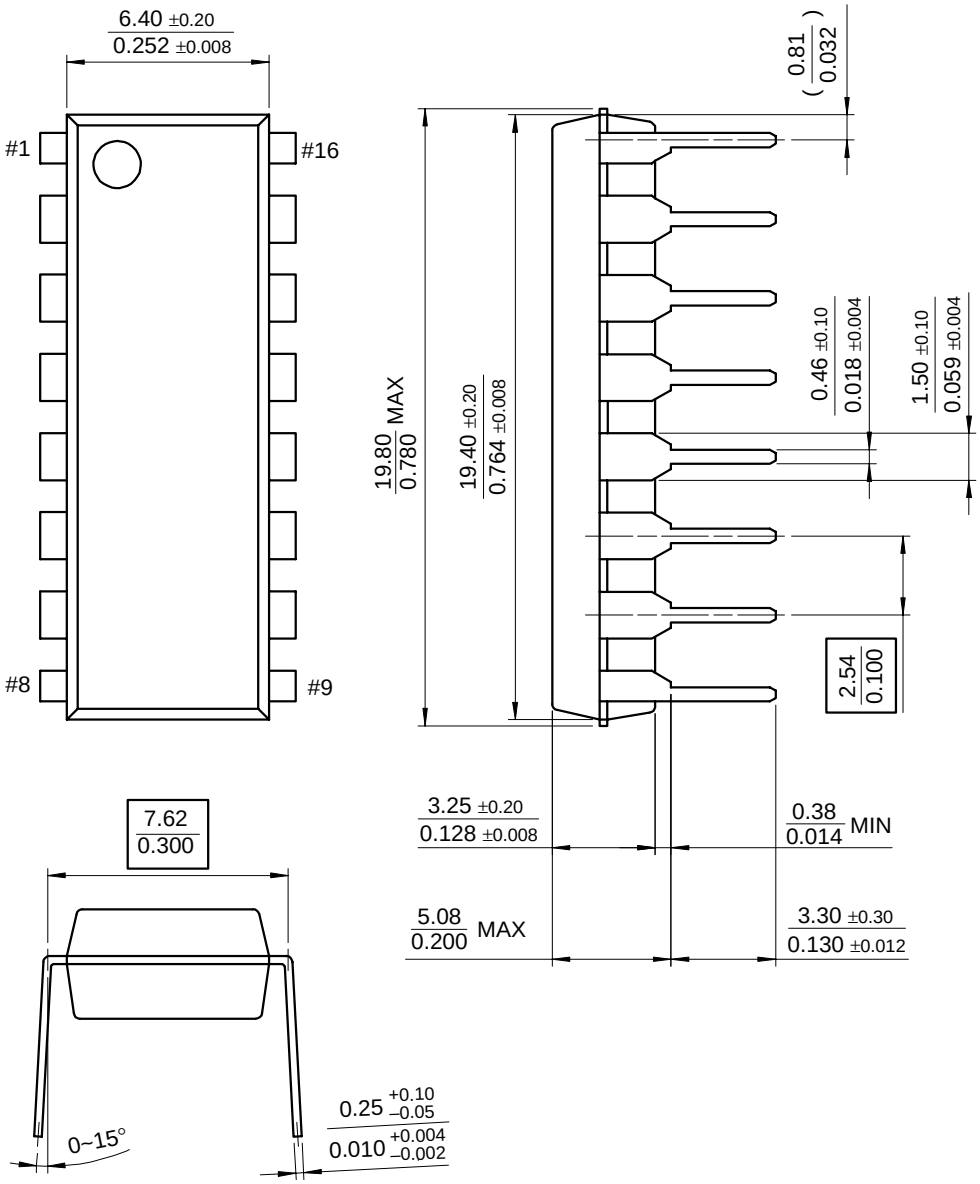
Figure 20. PG Delay Time

Mechanical Dimensions

Package

Dimensions in millimeters

16-DIP



Ordering Information

Product Number	Package	Operating Temperature
FAN3506	16-DIP	-25°C ~ +85°C

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