

## 74LVT16240 • 74LVTH16240

### Low Voltage 16-Bit Inverting Buffer/Line Driver with 3-STATE Outputs

#### General Description

The LVT16240 and LVTH16240 contain sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled.

Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The LVTH16240 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These buffers and line drivers are designed for low-voltage (3.3V)  $V_{CC}$  applications, but with the capability to provide a TTL interface to a 5V environment. The LVT16240 and LVTH16240 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

#### Features

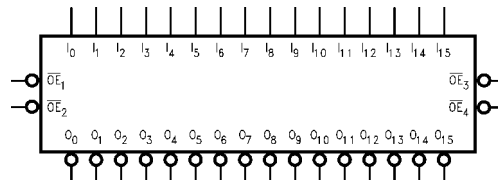
- Input and output interface capability to systems at 5V  $V_{CC}$
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH16240), also available without bushold feature (74LVT16240)
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- Functionally compatible with the 74 series 16240
- Latch-up performance exceeds 500 mA
- ESD performance:
  - Human-body model > 2000V
  - Machine model > 200V
  - Charged-device model > 1000V

#### Ordering Code:

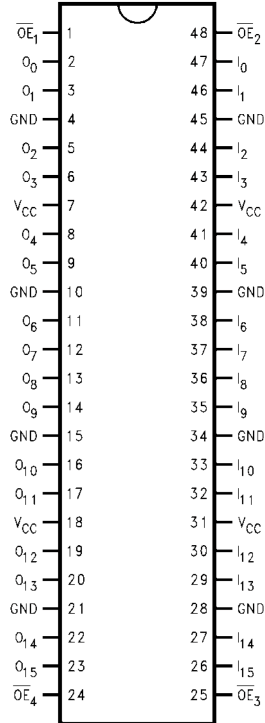
Order Number	Package Number	Package Description
74LVT16240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVT16240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH16240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LVTH16240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_n$	Output Enable Inputs (Active LOW)
$I_0-I_{15}$	Inputs
$\overline{O}_0-\overline{O}_{15}$	3-STATE Outputs

### Truth Table

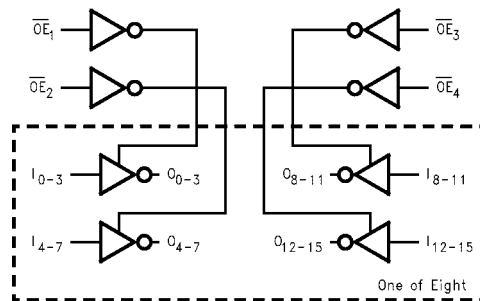
Inputs		Outputs
$\overline{OE}_1$	$I_0-I_3$	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z
Inputs		Outputs
$\overline{OE}_2$	$I_4-I_7$	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z
Inputs		Outputs
$\overline{OE}_3$	$I_8-I_{11}$	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z
Inputs		Outputs
$\overline{OE}_4$	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance

### Functional Description

The LVT16240 and LVTH16240 contain sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4-bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are controlled by an Output Enable ( $\overline{OE}_n$ ) input for each nibble. When  $\overline{OE}_n$  is LOW, the outputs are in 2-state mode. When  $\overline{OE}_n$  is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings <sup>(Note 1)</sup>					
Symbol	Parameter	Value	Conditions	Units	
$V_{CC}$	Supply Voltage	-0.5 to +4.6		V	
$V_I$	DC Input Voltage	-0.5 to +7.0		V	
$V_O$	DC Output Voltage	-0.5 to +7.0	Output in 3-STATE	V	
		-0.5 to $V_{CC} + 0.5$	Output in HIGH or LOW State (Note 2)		
$I_{IK}$	DC Input Diode Current	-50	$V_I < GND$	mA	
$I_{OK}$	DC Output Diode Current	-50	$V_O < GND$	mA	
$I_O$	DC Output Current	64	$V_O > V_{CC}$ Output at HIGH State	mA	
		128	$V_O > V_{CC}$ Output at LOW State		
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 64$		mA	
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 128$		mA	
$T_{STG}$	Storage Temperature	-65 to +150		°C	

Recommended Operating Conditions					
Symbol	Parameter	Min	Max	Units	
$V_{CC}$	Supply Voltage	2.7	3.6	V	
$V_I$	Input Voltage	0	5.5	V	
$I_{OH}$	HIGH Level Output Current		-32	mA	
$I_{OL}$	LOW Level Output Current		64	mA	
$T_A$	Free-Air Operating Temperature	-40	85	°C	
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8V-2.0V$ , $V_{CC} = 3.0V$	0	10	ns/V	

**Note 1:** Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

**Note 2:**  $I_O$  Absolute Maximum Rating must be observed.

### DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$			Units	Conditions	
			Min	Typ (Note 10)	Max			
$V_{IK}$	Input Clamp Diode Voltage	2.7			-1.2	V	$I_I = -18\text{ mA}$	
$V_{IH}$	Input HIGH Voltage	2.7-3.6	2.0			V	$V_O \leq 0.1V$ or $V_O \geq V_{CC} - 0.1V$	
$V_{IL}$	Input LOW Voltage	2.7-3.6			0.8	V		
$V_{OH}$	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$			V	$I_{OH} = -100\ \mu\text{A}$	
		2.7	2.4				$I_{OH} = -8\text{ mA}$	
		3.0	2.0				$I_{OH} = -32\text{ mA}$	
$V_{OL}$	Output LOW Voltage	2.7			0.2	V	$I_{OL} = 100\ \mu\text{A}$	
		2.7			0.5		$I_{OL} = 24\text{ mA}$	
		3.0			0.4		$I_{OL} = 16\text{ mA}$	
		3.0			0.5		$I_{OL} = 32\text{ mA}$	
		3.0			0.55		$I_{OL} = 64\text{ mA}$	
$I_{I(HOLD)}$ (Note 4)	Bushold Input Minimum Drive	3.0	75			$\mu\text{A}$	$V_I = 0.8V$	
			-75				$V_I = 2.0V$	
$I_{I(OD)}$ (Note 4)	Bushold Input Over-Drive Current to Change State	3.0	500			$\mu\text{A}$	(Note 5)	
			-500				(Note 6)	
$I_I$	Input Current	3.6			10	$\mu\text{A}$	$V_I = 5.5V$	
		Control Pins	3.6				$\pm 1$	$V_I = 0V$ or $V_{CC}$
			Data Pins	3.6				-5
					1	$V_I = V_{CC}$		
$I_{OFF}$	Power Off Leakage Current	0			$\pm 100$	$\mu\text{A}$	$0V \leq V_I$ or $V_O \leq 5.5V$	
$I_{PU/PD}$	Power Up/Down 3-STATE	0-1.5V			$\pm 100$	$\mu\text{A}$	$V_O = 0.5V$ to $3.0V$	
	Output Current						$V_I = GND$ or $V_{CC}$	
$I_{OZL}$	3-STATE Output Leakage Current	3.6			-5	$\mu\text{A}$	$V_O = 0.5V$	
$I_{OZH}$	3-STATE Output Leakage Current	3.6			5	$\mu\text{A}$	$V_O = 3.0V$	

## DC Electrical Characteristics (Continued)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 10)	Max		
I <sub>OZH</sub> <sup>+</sup>	3-STATE Output Leakage Current	3.6			10	μA	V <sub>CC</sub> < V <sub>O</sub> ≤ 5.5V
I <sub>CCH</sub>	Power Supply Current	3.6			0.19	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs HIGH
I <sub>CCL</sub>	Power Supply Current	3.6			5	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs LOW
I <sub>CCZ</sub>	Power Supply Current	3.6			0.19	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , Outputs Disabled
I <sub>CCZH</sub> <sup>+</sup>	Power Supply Current	3.6			0.19	mA	V <sub>I</sub> = GND or V <sub>CC</sub> , V <sub>CC</sub> ≤ V <sub>O</sub> ≤ 5.5V, Outputs Disabled
ΔI <sub>CC</sub>	Increase in Power Supply Current (Note 7)	3.6			0.2	mA	One Input at V <sub>CC</sub> - 0.6V Other Inputs at V <sub>CC</sub> or GND

**Note 3:** All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

**Note 4:** Applies to bushold versions only (LVTH16240).

**Note 5:** An external driver must source at least the specified current to switch from LOW-to-HIGH.

**Note 6:** An external driver must sink at least the specified current to switch from HIGH-to-LOW.

**Note 7:** This is the increase in supply current for each input that is at the specified voltage level rather than V<sub>CC</sub> or GND.

## Dynamic Switching Characteristics (Note 8)

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			Units	Conditions C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω
			Min	Typ	Max		
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub>	3.3		0.8		V	(Note 9)
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub>	3.3		-0.8		V	(Note 9)

**Note 8:** Characterized in SSOP package. Guaranteed parameter, but not tested.

**Note 9:** Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output at LOW.

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500Ω					Units
		V <sub>CC</sub> = 3.3V ± 0.3V			V <sub>CC</sub> = 2.7V		
		Min	Typ (Note 10)	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay Data to Output	1.0		3.5	1.0	4.2	ns
t <sub>PHL</sub>		1.0		3.5	1.0	4.0	
t <sub>PZH</sub>	Output Enable Time	1.0		4.0	1.0	4.9	ns
t <sub>PZL</sub>		1.2		4.8	1.2	6.1	
t <sub>PHZ</sub>	Output Disable Time	1.7		4.7	1.7	5.2	ns
t <sub>PLZ</sub>		1.7		4.2	1.7	4.4	
t <sub>OSHL</sub>	Output to Output Skew (Note 11)			1.0		1.0	ns
t <sub>OSLH</sub>							

**Note 10:** All typical values are at V<sub>CC</sub> = 3.3V, T<sub>A</sub> = 25°C.

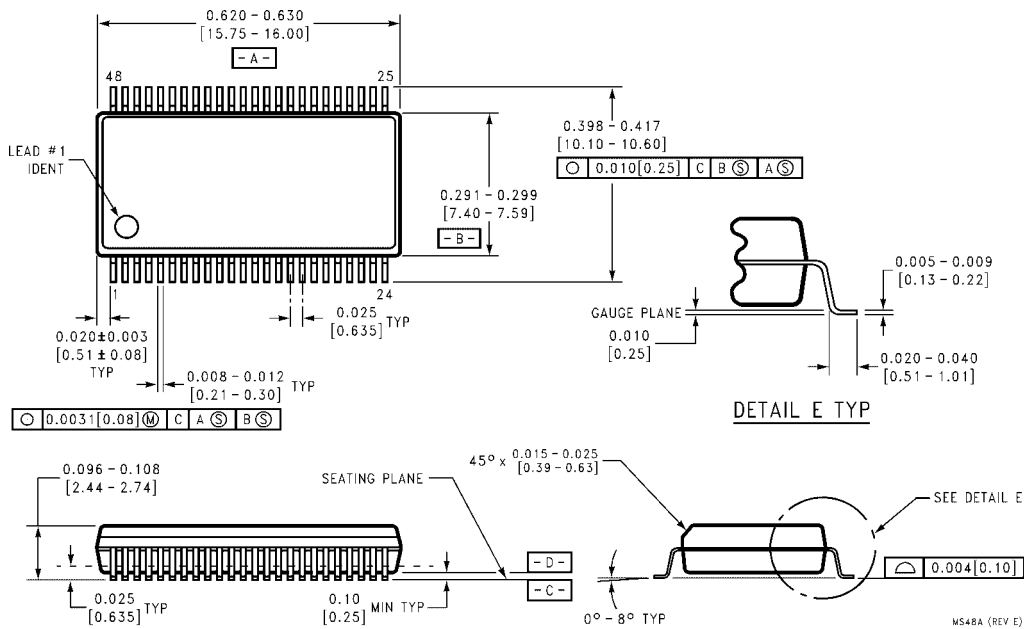
**Note 11:** Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t<sub>OSHL</sub>) or LOW-to-HIGH (t<sub>OSLH</sub>).

## Capacitance (Note 12)

Symbol	Parameter	Conditions	Typical	Units
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = 0V, V <sub>I</sub> = 0V or V <sub>CC</sub>	4	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>CC</sub> = 3.0V, V <sub>O</sub> = 0V or V <sub>CC</sub>	8	pF

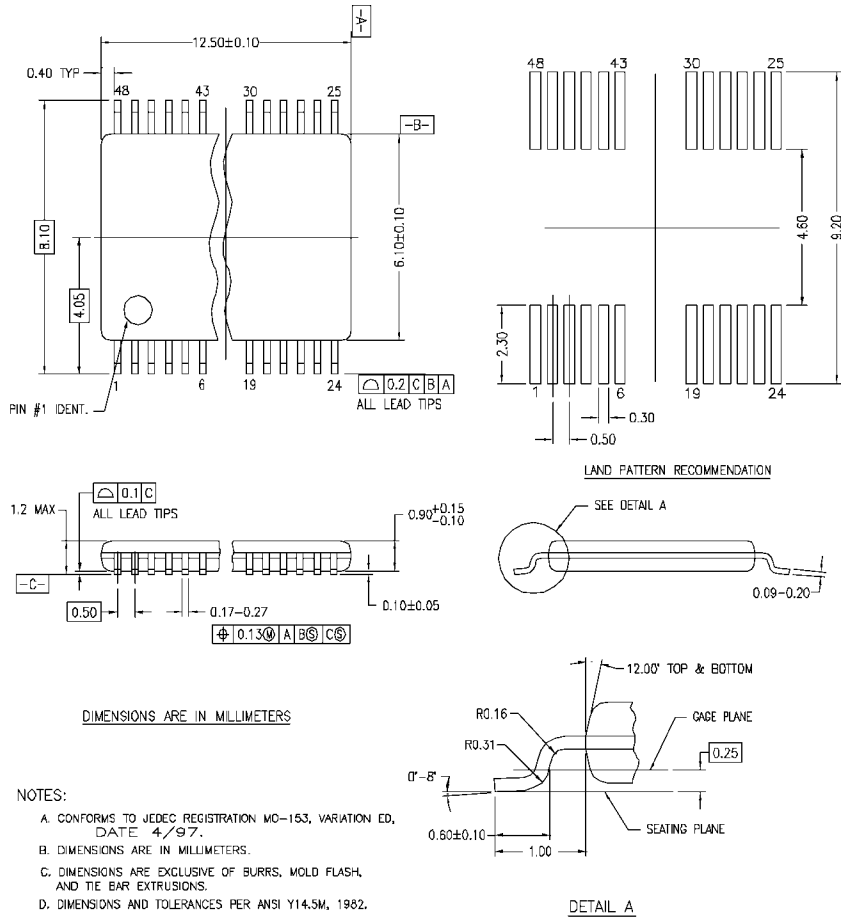
**Note 12:** Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

**Physical Dimensions** inches (millimeters) unless otherwise noted



**48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide  
Package Number MS48A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



MTD48REV C

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)