

74LCX38

Low Voltage Quad 2-Input NAND Gate (Open Drain) with 5V Tolerant Inputs

General Description

The LCX38 contains four 2-input open drain NAND gates. The inputs tolerate voltages up to 7V allowing the interface of 5V systems to 3V systems.

The 74LCX38 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

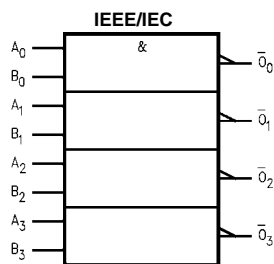
- 5V tolerant inputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.5 ns t_{PD} max ($V_{CC} = 3.3V$), 10 μA I_{CC} max
- Power down high impedance inputs and outputs
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 150V

Ordering Code:

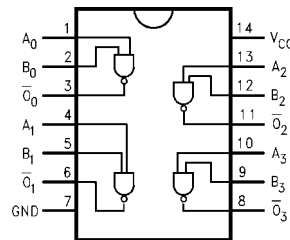
Order Number	Package Number	Package Description
74LCX38M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
74LCX38SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX38MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n, B_n	Inputs
\bar{O}_n	Outputs

74LCX38 Low Voltage Quad 2-Input NAND Gate (Open Drain) with 5V Tolerant Inputs

Absolute Maximum Ratings (Note 1)					
Symbol	Parameter	Value	Conditions	Units	
V _{CC}	Supply Voltage	-0.5 to +7.0		V	
V _I	DC Input Voltage	-0.5 to +7.0		V	
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	Output in HIGH or LOW State (Note 2)	V	
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA	
I _{OK}	DC Output Diode Current	-50 +50	V _O < GND V _O > V _{CC}	mA	
I _O	DC Output Source/Sink Current	±50		mA	
I _{CC}	DC Supply Current per Supply Pin	±100		mA	
I _{GND}	DC Ground Current per Ground Pin	±100		mA	
T _{STG}	Storage Temperature	-65 to +150		°C	

Recommended Operating Conditions (Note 3)					
Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage				
		Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V _I	Input Voltage	0	5.5	V	
V _O	Output Voltage				
		HIGH or LOW State	0	V _{CC}	V
I _{OH} /I _{OL}	Output Current				
		V _{CC} = 3.0V – 3.6V		±24	mA
		V _{CC} = 2.7V – 3.0V		±12	
		V _{CC} = 2.3V – 2.7V		±8	
T _A	Free-Air Operating Temperature	-40	85	°C	
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V	

Note 1: The Absolute Maximum Ratings are those beyond which the safety of the device cannot be guaranteed. The device should not be operating at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 – 2.7 2.7 – 3.6	1.7 2.0		V
V _{IL}	LOW Level Input Voltage		2.3 – 2.7 2.3 – 3.6		0.7 0.8	V
V _{OL}	LOW Level Output Voltage	I _{OL} = 100μA I _{OL} = 8mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA	2.3 – 3.6 2.3 2.7 3.0 3.0		0.2 0.6 0.4 0.4 0.55	V
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND 3.6V ≤ V _I ≤ 5.5V	2.3 – 3.6 2.3 – 3.6		10 ±10	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6V	2.3 – 3.6		500	μA

AC Electrical Characteristics								
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500 Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
t _{PZL}	Propagation Delay Time	1.5	5.0	1.5	5.5	1.5	6.5	ns
t _{PLZ}		1.5	5.0	1.5	5.5	1.5	6.0	
t _{OSSL}	Output to Output Skew (Note 4)		1.0					ns
t _{OSLH}			1.0					
Note 4: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t _{OSSL}) or LOW-to-HIGH (t _{OSLH}).								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C	Units			
				Typical				
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	0.8 0.6	V			
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	3.3 2.5	-0.8 -0.6	V			
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF				
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF				
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	25	pF				

AC Loading and Waveforms Generic for LCX Family

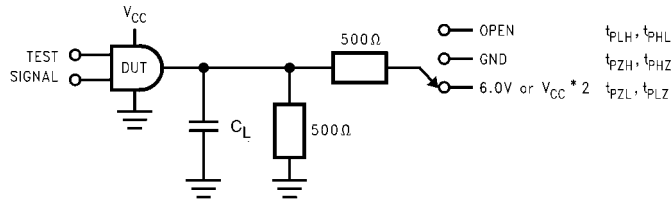
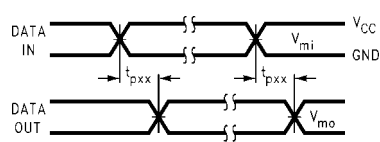
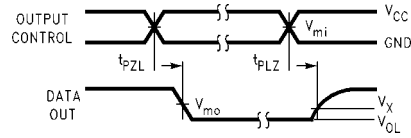


FIGURE 1. AC Test Circuit
(C_L includes probe and jig capacitance)

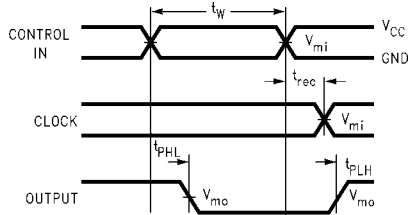
Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$ $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND



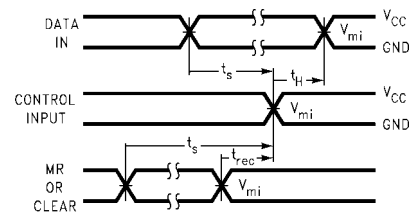
Waveform for Inverting and Non-Inverting Functions



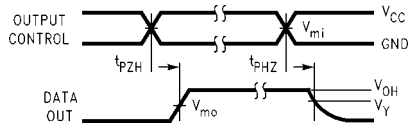
3-STATE Output Low Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output High Enable and Disable Times for Logic

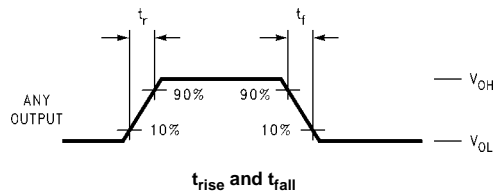
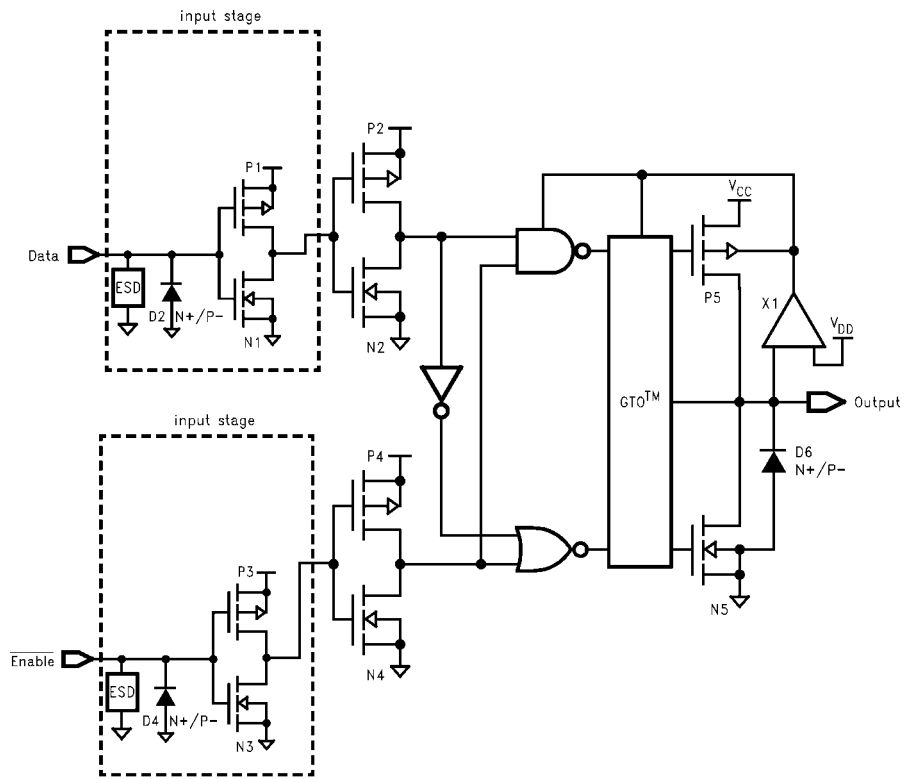


FIGURE 2. Waveforms

(Input Pulse Characteristics; $f=1MHz, t_r=t_f=3ns$)

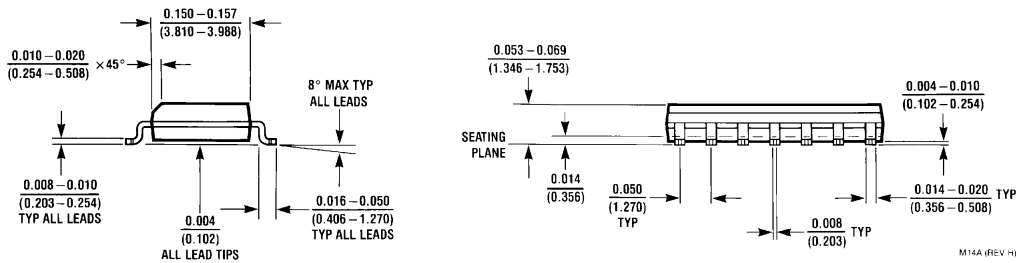
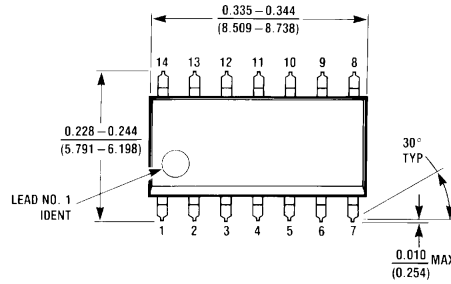
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram

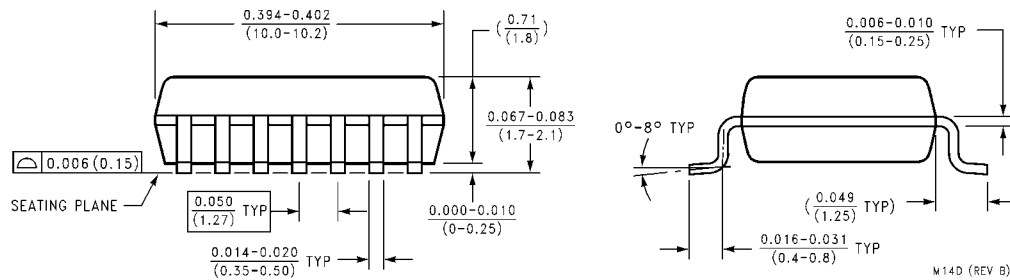
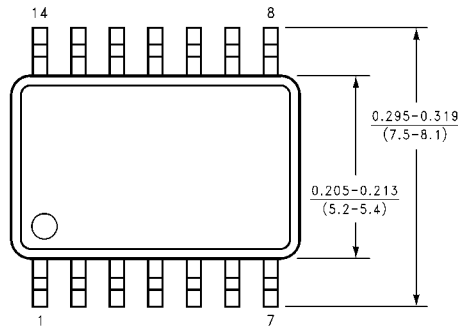


74LCX38

Physical Dimensions inches (millimeters) unless otherwise noted

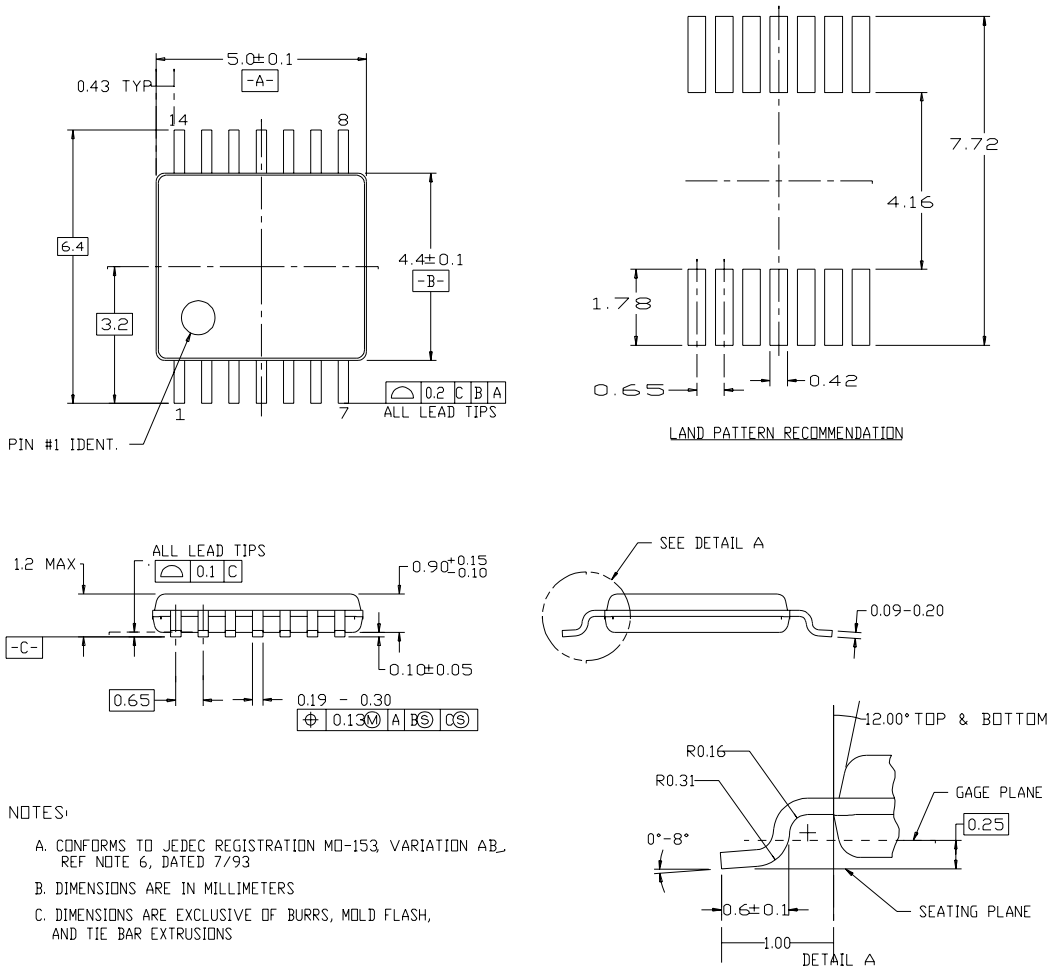


**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
Package Number M14A**



**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

- Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com