

74ACT533

Octal Transparent Latch with 3-STATE Outputs

General Description

The ACT533 consists of eight latches with 3-STATE outputs for bus organized system applications. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. When LE is low, the data satisfying the input timing requirements is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH, the bus output is in the high impedance state.

Features

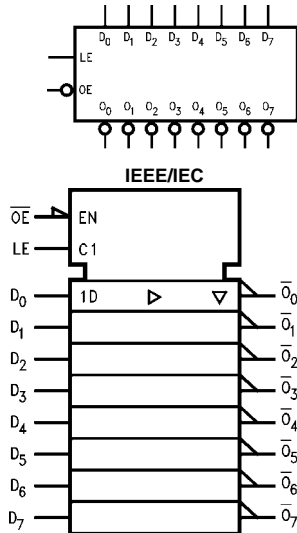
- I_{CC} and I_{OZ} reduced by 50%
- Eight latches in a single package
- 3-STATE outputs drive bus lines or buffer memory address registers
- Outputs source/sink 24 mA
- Inverted version of the ACT373
- TTL-compatible inputs

Ordering Code:

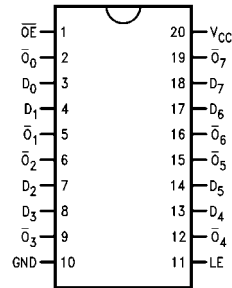
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74ACT533SC | M20B | 20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide |
| 74ACT533MTC | MTC20 | 20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT533PC | N20A | 20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code

Logic Symbols



Connection Diagram



Pin Descriptions

| Pin Names | Description |
|-------------------------------------|-----------------------|
| D_0 - D_7 | Data Inputs |
| LE | Latch Enable Input |
| \overline{OE} | Output Enable Input |
| \overline{O}_0 - \overline{O}_7 | 3-STATE Latch Outputs |

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Functional Description

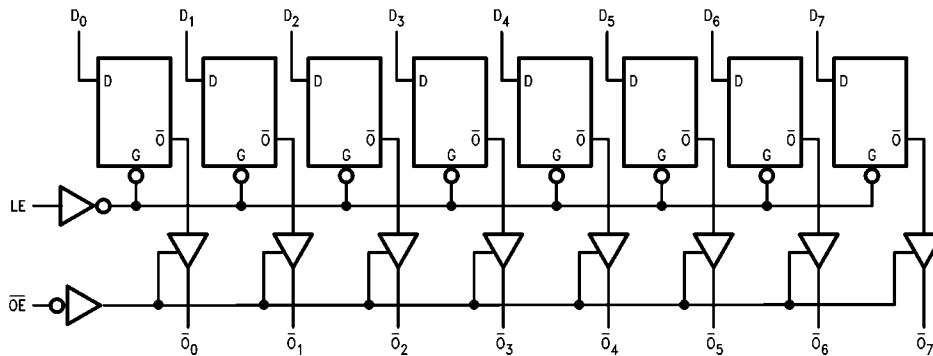
The ACT533 contains eight D-type latches with 3-STATE standard outputs. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW, the latches store the information that was present on the D inputs at setup time preceding the HIGH-to-LOW transition of LE. The 3-STATE standard outputs are controlled by the Output Enable (\overline{OE}) input. When \overline{OE} is LOW, the standard outputs are in the 2-state mode. When \overline{OE} is HIGH, the standard outputs are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

| Inputs | | | Outputs |
|--------|-----------------|-------|------------------|
| LE | \overline{OE} | D_n | \overline{O}_n |
| X | H | X | Z |
| H | L | L | H |
| H | L | H | L |
| L | L | X | \overline{O}_0 |

H = HIGH Voltage Level
 L = LOW Voltage Level
 Z = High Impedance
 X = Immaterial
 \overline{O}_0 = Previous \overline{O}_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

| | |
|--|---------------------------|
| Supply Voltage (V_{CC}) | - 0.5V to + 7.0V |
| DC Input Diode Current (I_{IK}) | |
| $V_I = -0.5V$ | - 20 mA |
| $V_I = V_{CC} + 0.5V$ | + 20 mA |
| DC Input Voltage (V_I) | -0.5V to $V_{CC} + 0.5V$ |
| DC Output Diode Current (I_{OK}) | |
| $V_O = -0.5V$ | - 20 mA |
| $V_O = V_{CC} + 0.5V$ | + 20 mA |
| DC Output Voltage (V_O) | - 0.5V to $V_{CC} + 0.5V$ |
| DC Output Source | |
| or Sink Current (I_O) | ± 50 mA |
| DC V_{CC} or Ground Current | |
| per Output Pin (I_{CC} or I_{GND}) | ± 50 mA |
| Storage Temperature (T_{STG}) | - 65°C to + 150°C |
| DC Latchup Source | |
| or Sink Current | ± 300 mA |
| Junction Temperature (T_J) | |
| PDIP | 140°C |

Recommended Operating Conditions

| | |
|---|----------------|
| Supply Voltage (V_{CC}) | 4.5V to 5.5V |
| Input Voltage (V_I) | 0V to V_{CC} |
| Output Voltage (V_O) | 0V to V_{CC} |
| Operating Temperature (T_A) | -40°C to +85°C |
| Minimum Input Edge Rate $\Delta V/\Delta t$ | |
| V_{IN} from 0.8V to 2.0V | |
| V_{CC} @ 4.5V, 5.5V | 125 mV/ns |

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, with-out exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

| Symbol | Parameter | V_{CC} (V) | $T_A = +25^\circ\text{C}$ | | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ | | Units | Conditions |
|-----------|--------------------------------------|-----------------|---------------------------|-------------------|---|---------|--|------------|
| | | | Typ | Guaranteed Limits | | | | |
| V_{IH} | Minimum HIGH Level Input Voltage | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 2.0 | 2.0 | | | |
| V_{IL} | Maximum LOW Level Input Voltage | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$ | |
| | | 5.5 | 1.5 | 0.8 | 0.8 | | | |
| V_{OH} | Minimum HIGH Level Output Voltage | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50 \mu A$ | |
| | | 5.5 | 5.49 | 5.4 | 5.4 | | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -24$ mA $I_{OH} = -24$ mA (Note 2) | |
| | | 5.5 | | 4.86 | 4.76 | | | |
| V_{OL} | Maximum LOW Level Output Voltage | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50 \mu A$ | |
| | | 5.5 | 0.001 | 0.1 | 0.1 | | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 2) | |
| | | 5.5 | | 0.36 | 0.44 | | | |
| I_{IN} | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CC}, GND$ | |
| I_{OZ} | Maximum 3-STATE Leakage Current | 5.5 | | ± 0.25 | ± 2.5 | μA | $V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$ | |
| I_{CCT} | Maximum $I_{CC}/Input$ | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC} - 2.1V$ | |
| I_{OLD} | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max | |
| I_{OHD} | Output Current (Note 3) | 5.5 | | | -75 | mA | $V_{OHD} = 3.85V$ Min | |
| I_{CC} | Maximum Quiescent Supply Current | 5.5 | | 4.0 | 40.0 | μA | $V_{IN} = V_{CC}$ or GND | |

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

| Symbol | Parameter | V _{CC} (V) (Note 4) | T _A = + 25°C C _L = 50 pF | | | T _A = - 40°C to + 85°C C _L = 50 pF | | Units |
|--------------------------------------|---|------------------------------------|---|-----|------|---|------|-------|
| | | | Min | Typ | Max | Min | Max | |
| t _{PHL} t _{PLH} | Propagation Delay D _n to O _n | 5.0 | 2.0 | 6.0 | 8.0 | 2.0 | 8.5 | ns |
| t _{PHL} t _{PLH} | Propagation Delay LE to O _n | 5.0 | 2.5 | 7.0 | 9.0 | 2.5 | 9.5 | ns |
| t _{PZL} , t _{PZH} | Output Enable Time | 5.0 | 2.0 | 7.0 | 9.0 | 2.0 | 9.5 | ns |
| t _{PHZ} , t _{PLZ} | Output Disable Time | 5.0 | 1.0 | 8.0 | 10.0 | 1.0 | 10.5 | ns |

Note 4: Voltage Range 5.0 is 5.0V ± 0.5V.

AC Operating Requirements

| Symbol | Parameter | V _{CC} (V) (Note 5) | T _A = + 25°C C _L = 50 pF | | T _A = - 40°C to + 85°C C _L = 50 pF | Units |
|----------------|---|------------------------------------|---|--------------------|---|-------|
| | | | Typ | Guaranteed Minimum | | |
| t _S | Setup Time, HIGH or LOW D _n to LE | 5.0 | 0 | 3.0 | 3.0 | ns |
| t _H | Hold Time, HIGH or LOW D _n to LE | 5.0 | 0 | 1.5 | 1.5 | ns |
| t _W | LE Pulse Width, HIGH | 5.0 | 2.0 | 4.0 | 4.0 | ns |

Note 5: Voltage Range 5.0 is 5.0V ± 0.5V.

Capacitance

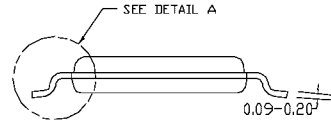
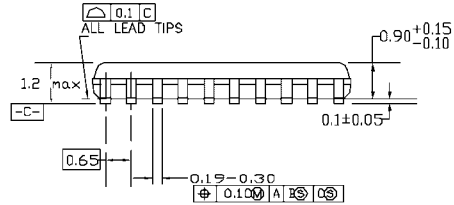
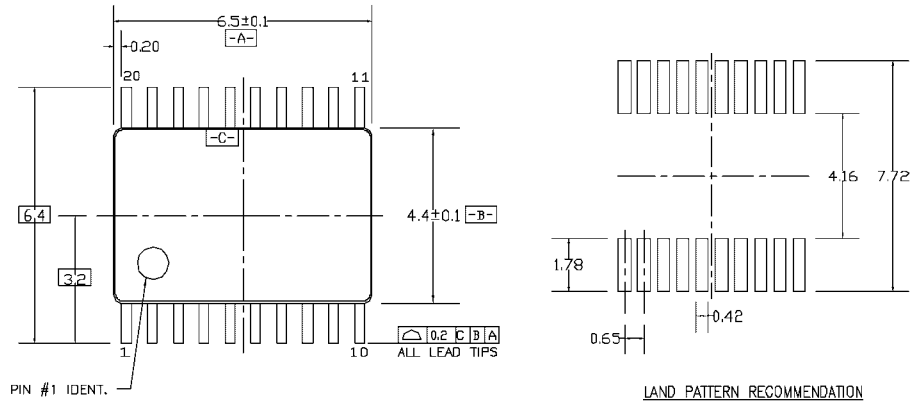
| Symbol | Parameter | Typ | Units | Conditions |
|-----------------|-------------------------------|-----|-------|------------------------|
| C _{IN} | Input Capacitance | 4.5 | pF | V _{CC} = OPEN |
| C _{PD} | Power Dissipation Capacitance | 40 | pF | V _{CC} = 5.0V |

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B**

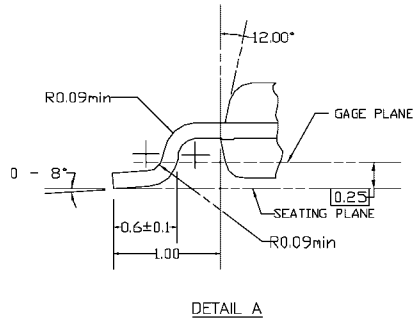
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

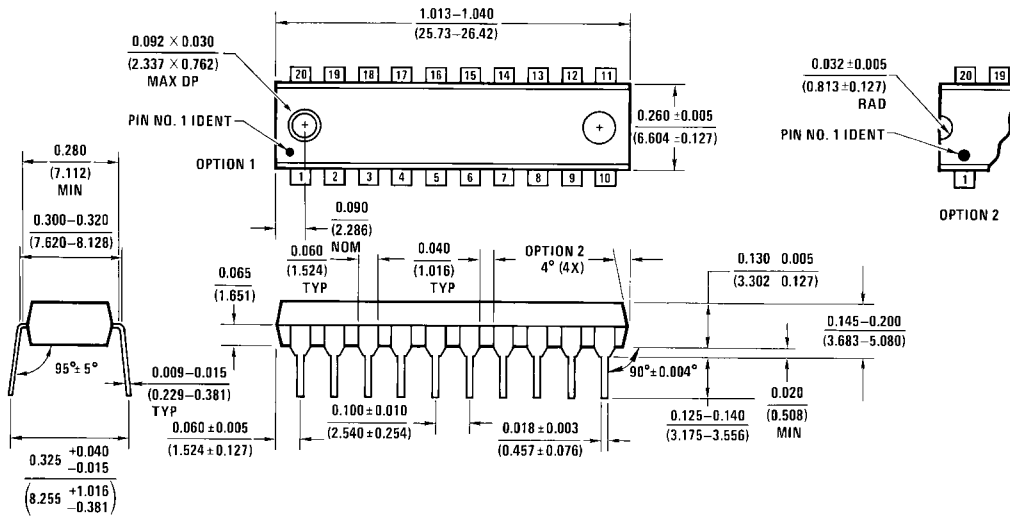
- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.



MTC20REV D1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A**

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