**FAIRCHILD**

SEMICONDUCTOR ™

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## 100397

# Quad Differential ECL/TTL Translating Transceiver with Latch

## General Description

The 100397 is a quad latched transceiver designed to convert TTL logic levels to differential F100K ECL logic levels and vice versa. This device was designed with the capability of driving a differential 25Ω ECL load with cutoff capability, and will sink a 64 mA TTL load. The 100397 is ideal for mixed technology applications utilizing either an ECL or TTL backplane.

The direction of translation is set by the direction control pin (DIR). The DIR pin on the 100397 accepts F100K ECL logic levels. An ECL LOW on DIR sets up the ECL pins as inputs and TTL pins as outputs. An ECL HIGH on DIR sets up the TTL pins as inputs and ECL pins as outputs.

A LOW on the output enable input pin (OE) holds the ECL output in a cut-off state and the TTL outputs at a high impedance level. A HIGH on the latch enable input (LE) latches the data at both inputs even though only one output is enabled at the time. A LOW on LE makes the latch transparent.

The cut-off state is designed to be more negative than a normal ECL LOW level. This allows the output emitterfollowers to turn off when the termination supply is −2.0V, presenting a high impedance to the data bus. This high impedance reduces termination power and prevents loss of low state noise margin when several loads share the bus.

The 100397 is designed with FAST® TTL output buffers, featuring optimal DC drive and capable of quickly charging and discharging highly capacitive loads. All inputs have 50 KΩ pull-down resistors.

## Features

■ Differential ECL input/output structure
■ 64 mA FAST TTL outputs
■ 25Ω differential ECL outputs with cut-off
■ Bi-directional translation
■ 2000V ESD protection
■ Latched outputs
■ 3-STATE outputs
■ Voltage compensated operating range = −4.2V to −5.7V

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 100397PC | N24E | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide |
| 100397QC | V28A | 28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square |
| 100397QI | V28A | 28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (−40°C to +85°C) |

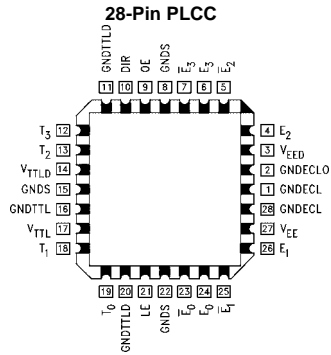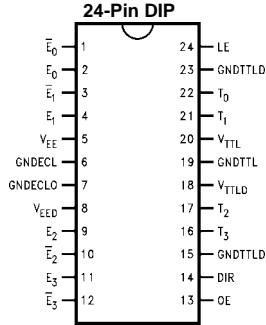Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

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## Logic Symbol
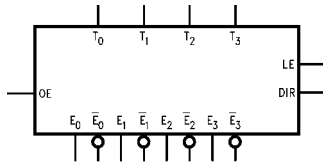


## Connection Diagrams

### 24-Pin DIP



### 28-Pin PLCC



## Pin Descriptions

| Pin Names | Description |
|---|---|
| $E_0$–$E_3$ | ECL Data I/O |
| $\overline{E}_0$–$\overline{E}_3$ | Complementary ECL Data I/O |
| $T_0$–$T_3$ | TTL Data I/O |
| OE | Output Enable Input (ECL Levels) |
| LE | Latch Enable Input (ECL Levels) |
| DIR | Direction Control Input (ECL levels) |
| GNDECL | ECL Ground |
| GNDECLO | ECL Output Ground |
| GNDS | ECL Ground-to-Substrate |
| $V_{EE}$ | ECL Quiescent Power Supply |
| $V_{EED}$ | ECL Dynamic Power Supply |
| GNDTTL | TTL Quiescent Ground |
| GNDTTLD | TTL Dynamic Ground |
| $V_{TTL}$ | TTL Quiescent Power Supply |
| $V_{TTLD}$ | TTL Dynamic Power Supply |

All pins function at 100K ECL levels except for $T_0$–$T_3$.

## Truth Table

| LE | DIR | OE | ECL Port | TTL Port | Notes |
|---|---|---|---|---|---|
| 0 | 0 | 0 | LOW (Cut-Off) | Z | |
| 0 | 0 | 1 | Input | Output | (Note 1)(Note 4) |
| 0 | 1 | 0 | LOW (Cut-Off) | Z | |
| 0 | 1 | 1 | Output | Input | (Note 2)(Note 4) |
| 1 | 0 | 0 | Input | Z | (Note 1)(Note 3) |
| 1 | 0 | 1 | Latched | X | (Note 1)(Note 3) |
| 1 | 1 | 0 | LOW (Cut-Off) | Input | (Note 2)(Note 3) |
| 1 | 1 | 1 | Latched | X | (Note 2)(Note 3) |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
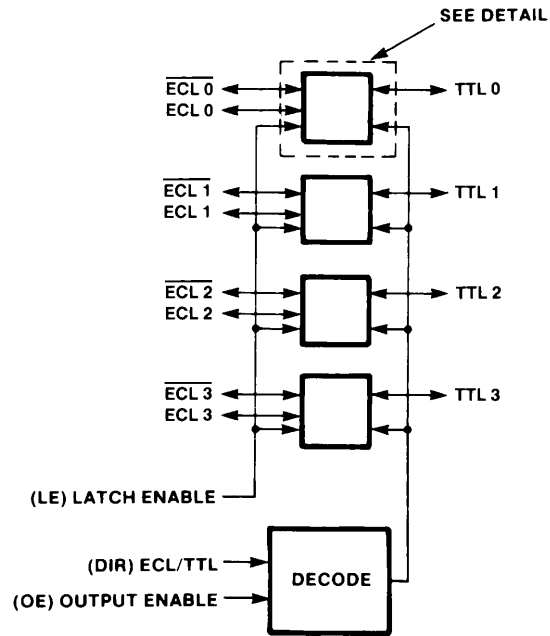Z = High Impedance

**Note 1:** ECL input to TTL output mode.

**Note 2:** TTL input to ECL output mode.
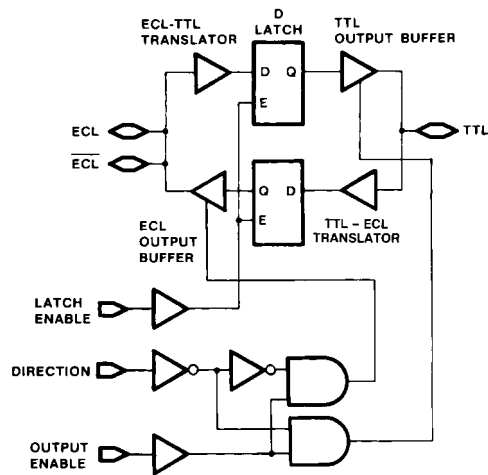
**Note 3:** Retains data present before LE set HIGH.

**Note 4:** Latch is transparent.

## Functional Diagram



**Note:** LE, DIR, and OE use ECL logic levels

## Detail

## Absolute Maximum Ratings(Note 5)

| | |
|---|---|
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Maximum Junction Temperature | |
| ($T_J$) | +150°C |
| $V_{EE}$ Pin Potential to Ground Pin | −7.0V to +0.5V |
| $V_{TTL}$ Pin Potential to Ground Pin | −0.5V to +6.0V |
| ECL Input Voltage (DC) | $V_{EE}$ to +0.5V |
| ECL Output Current | |
| (DC Output HIGH) | −50 mA |
| TTL Input Voltage (Note 7) | −0.5V to +7.0V |
| TTL Input Current (Note 7) | −30 mA to +5.0 mA |
| Voltage Applied to Output | |
| in HIGH State | |
| 3-STATE Output | −0.5V to +5.5V |
| Current Applied to TTL | |
| Output in LOW State (Max) | twice the Rated $I_{OL}$ (mA) |
| ESD (Note 6) | ≥2000V |

## Recommended Operating Conditions

| | |
|---|---|
| Case Temperature ($T_C$) | |
| Commercial | 0°C to +85°C |
| Industrial | −40°C to +85°C |
| ECL Supply Voltage ($V_{EE}$) | −5.7V to −4.2V |
| TTL Supply Voltage ($V_{TTL}$) | +4.5V to +5.5V |

**Note 5:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 6:** ESD testing conforms to MIL-STD-883, Method 3015.

**Note 7:** Either voltage limit or current limit is sufficient to protect inputs.

## Commercial Version

## TTL-to-ECL DC Electrical Characteristics (Note 8)

$V_{EE}$ = −4.2V to −5.7V, GND = 0V, $T_C$ = 0°C to +85°C, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1025 | −955 | −870 | mV | $V_{IN}$ = $V_{IH(Max)}$ or $V_{IL(Min)}$ |
| $V_{OL}$ | Output LOW Voltage | −1830 | −1705 | −1620 | mV | Loading with 50Ω to − 2V |
| | Cutoff Voltage | | −2000 | −1950 | mV | OE and LE Low, DIR High $V_{IN}$ = $V_{IH(Max)}$ or $V_{IL}$(Min), Loading with 50Ω to −2V |
| $V_{OHC}$ | Output HIGH Voltage Corner Point High | −1035 | | | mV | $V_{IN}$ = $V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V |
| $V_{OLC}$ | Output LOW Voltage Corner Point Low | | | −1610 | mV | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 5.0 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $V_{IL}$ | Input LOW Voltage | 0 | | 0.8 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $I_{IH}$ | Input HIGH Current | | | 5.0 | μA | $V_{IN}$ = +2.7V |
| $I_{BVIT}$ | Input HIGH Current Breakdown (I/O) | | | 0.5 | mA | $V_{IN}$ = 5.5V |
| $I_{IL}$ | Input LOW Current | −1.0 | | | mA | $V_{IN}$ = +0.5V |
| $V_{FCD}$ | Input Clamp Diode Voltage | −1.2 | | | V | $I_{IN}$ = −18 mA |
| $I_{EE}$ | $V_{EE}$ Supply Current | −99 | | −50 | | LE Low, OE and DIR HIGH Inputs Open |
| $I_{EEZ}$ | $V_{EE}$ Supply Current | −159 | | −90 | | LE and OE Low, Dir HIGH Inputs Open |

**Note 8:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## Commercial Version (Continued)
## ECL-to-TTL DC Electrical Characteristics (Note 9)

$V_{EE}$ = −4.2V to −5.7V, GND = 0V, $T_C$ = 0°C to +85°C, $C_L$ = 50 pF, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.1 | | V | $I_{OH}$ = −3 mA, $V_{TTL}$ = 4.75V |
| | | 2.4 | 2.9 | | V | $I_{OH}$ = −3 mA, $V_{TTL}$ = 4.50V |
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.5 | V | $I_{OL}$ = 24 mA, $V_{TTL}$ = 4.50V |
| $V_{IH}$ | Input HIGH Voltage | −1165 | | −870 | mV | Guaranteed HIGH Signal for All Inputs |
| $V_{IL}$ | Input LOW Voltage | −1830 | | −1475 | mV | Guaranteed LOW Signal for All Inputs |
| $V_{DIFF}$ | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| $V_{CM}$ | Common Mode Voltage | GNDECL − 2.0 | | GNDECL − 0.5 | V | |
| $I_{IH}$ | Input HIGH Current $E_0$–$E_3$, $\overline{E}_0$–$\overline{E}_3$ | | | 240 | μA | $V_{IN}$ = $V_{IH(Max)}$ |
| | OE, LE, DIR | | | 35 | | |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | μA | $V_{OUT}$ = $V_{TTL}$ |
| $I_{ZZ}$ | Bus Drainage Test | | | 500 | μA | $V_{OUT}$ = 5.25V $V_{TTL}$ = 0.0V |
| $I_{IL}$ | Input LOW Current | 0.50 | | | μA | $V_{IN}$ = $V_{IL(Min)}$ |
| $I_{OZHT}$ | 3-STATE Current Output High | | | 70 | μA | $V_{OUT}$ = +2.7V |
| $I_{OZLT}$ | 3-STATE Current Output Low | −650 | | | μA | $V_{OUT}$ = +0.5V |
| $I_{OS}$ | Output Short-Circuit Current | −100 | | −225 | mA | $V_{OUT}$ = 0.0V, $V_{TTL}$ = +5.5V |
| $I_{TTL}$ | $V_{TTL}$ Supply Current | | | 39 | mA | TTL Outputs LOW |
| | | | | 27 | mA | TTL Outputs HIGH |
| | | | | 39 | mA | TTL Outputs in 3-STATE |

**Note 9:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

## DIP and PCC TTL-to-ECL AC Electrical Characteristics

$V_{EE}$ = −4.2V to −5.7V, $V_{TTL}$ = +4.5V to +5.5V

| Symbol | Parameter | $T_C$ = 0°C | | $T_C$ = 25°C | | $T_C$ = 85°C | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum Clock Frequency | 180 | | 180 | | 180 | | MHz | |
| $t_{PLH}$ $t_{PHL}$ | $T_n$ to $E_n$, $\overline{E}_n$ (Transparent) | 0.9 | 2.1 | 0.8 | 2.2 | 0.7 | 2.5 | ns | Figures 1, 3 |
| $t_{PLH}$ $t_{PHL}$ | LE to $E_n$, $\overline{E}_n$ | 1.2 | 2.3 | 1.3 | 2.4 | 1.4 | 2.5 | ns | Figures 1, 3 |
| $t_{PZH}$ | OE to $E_n$, $\overline{E}_n$ (Cutoff to HIGH) | 2.5 | 4.5 | 2.5 | 4.5 | 2.5 | 4.6 | ns | Figures 1, 3 |
| $t_{PHZ}$ | OE to $E_n$, $\overline{E}_n$ (HIGH to Cutoff) | 2.1 | 3.8 | 2.3 | 4.0 | 2.5 | 4.5 | ns | Figures 1, 3 |
| $t_{PHZ}$ | DIR to $E_n$, $\overline{E}_n$ (HIGH to Cutoff) | 2.0 | 3.5 | 2.1 | 3.7 | 2.3 | 4.2 | ns | Figures 1, 3 |
| $t_S$ | $T_n$ to LE | 0.8 | | 0.8 | | 0.8 | | ns | Figures 1, 3 |
| $t_H$ | $T_n$ to LE | 0.6 | | 0.6 | | 0.6 | | ns | Figures 1, 3 |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.8 | 2.8 | 0.8 | 2.8 | 0.8 | 2.8 | ns | Figures 1, 3 |

## Commercial Version (Continued)
## DIP and PCC ECL-to-TTL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{TTL} = +4.5V$ to $+5.5V$, $C_L = 50$ pF

| Symbol | Parameter | $T_C = 0°C$ | | $T_C = 25°C$ | | $T_C = 85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum Clock Frequency | 75 | | 75 | | 75 | | MHz | |
| $t_{PLH}$ $t_{PHL}$ | $E_n$, $\overline{E}_n$ to $T_n$ (Transparent) | 1.7 | 4.9 | 1.7 | 5.1 | 1.8 | 5.8 | ns | Figures 2, 4 |
| $t_{PLH}$ $t_{PHL}$ | LE to $T_n$ | 2.2 3.3 | 4.0 5.2 | 2.2 3.4 | 4.0 5.4 | 2.3 3.8 | 4.1 6.1 | ns | Figures 2, 4 |
| $t_{PZH}$ $t_{PZL}$ | OE to $T_n$ (Enable Time) | 3.2 4.9 | 5.6 8.3 | 3.3 5.1 | 5.7 8.5 | 3.6 5.6 | 6.3 9.2 | ns | Figures 2, 5 |
| $t_{PHZ}$ $t_{PLZ}$ | OE to $T_n$ (Disable Time) | 3.6 3.4 | 8.6 6.9 | 3.5 3.5 | 8.3 6.7 | 3.5 3.6 | 7.5 6.7 | ns | Figures 2, 5 |
| $t_{PHZ}$ $t_{PLZ}$ | DIR to $T_n$ (Disable Time) | 3.5 3.4 | 8.1 6.8 | 3.5 3.4 | 8.1 6.7 | 3.5 3.6 | 7.6 6.7 | ns | Figures 2, 6 |
| $t_S$ | $E_n$, $\overline{E}_n$ to LE | 0.6 | | 0.6 | | 0.6 | | ns | Figures 2, 4 |
| $t_H$ | $E_n$, $\overline{E}_n$ to LE | 0.7 | | 0.7 | | 0.7 | | ns | Figures 2, 4 |
| $t_{PW}(L)$ | Pulse Width LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 2, 4 |

## Industrial Version

## TTL-to-ECL DC Electrical Characteristics (Note 10)

$V_{EE} = -4.2V$ to $-5.7V$, GND = 0V, $T_C = -40°C$ to $+85°C$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | −1085 | −955 | −870 | mV | $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$ |
| $V_{OL}$ | Output LOW Voltage | −1830 | −1705 | −1575 | mV | Loading with 50Ω to −2V |
| | Cutoff Voltage | | −2000 | −1900 | mV | OE and LE LOW, DIR HIGH $V_{IN} = V_{IH(Max)}$ or $V_{IL(Min)}$, Loading with 50Ω to −2V |
| $V_{OHC}$ | Output HIGH Voltage Corner Point HIGH | −1095 | | | mV | $V_{IN} = V_{IH(Min)}$ or $V_{IL(Max)}$ Loading with 50Ω to −2V |
| $V_{OLC}$ | Output LOW Voltage Corner Point LOW | | | −1565 | mV | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | 5.0 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $V_{IL}$ | Input LOW Voltage | 0 | | 0.8 | V | Over $V_{TTL}$, $V_{EE}$, $T_C$ Range |
| $I_{IH}$ | Input HIGH Current | | | 5.0 | μA | $V_{IN} = +2.7V$ |
| $I_{BVIT}$ | Input HIGH Current Breakdown (I/O) | | | 0.5 | mA | $V_{IN} = 5.5V$ |
| $I_{IL}$ | Input LOW Current | −1.0 | | | mA | $V_{IN} = +0.5V$ |
| $V_{FCD}$ | Input Clamp Diode Voltage | −1.2 | | | V | $I_{IN} = -18$ mA |
| $I_{EE}$ | $V_{EE}$ Supply Current | −99 | | −40 | | LE Low, OE and DIR HIGH Inputs Open |
| $I_{EEZ}$ | $V_{EE}$ Supply Current | −159 | | −90 | | LE and OE LOW, Dir HIGH Inputs Open |

**Note 10:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

# Industrial Version (Continued)
## ECL-to-TTL DC Electrical Characteristics (Note 11)

$V_{EE} = -4.2V$ to $-5.7V$, GND = 0V, $T_C = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | 2.7 | 3.1 | | V | $I_{OH} = -3$ mA, $V_{TTL} = 4.75V$ |
| | | 2.4 | 2.9 | | V | $I_{OH} = -3$ mA, $V_{TTL} = 4.50V$ |
| $V_{OL}$ | Output LOW Voltage | | 0.3 | 0.5 | V | $I_{OL} = 24$ mA, $V_{TTL} = 4.50V$ |
| $V_{IH}$ | Input HIGH Voltage | −1170 | | −870 | mV | Guaranteed HIGH Signal for All Inputs |
| $V_{IL}$ | Input LOW Voltage | −1830 | | −1480 | mV | Guaranteed LOW Signal for All Inputs |
| $V_{DIFF}$ | Input Voltage Differential | 150 | | | mV | Required for Full Output Swing |
| $V_{CM}$ | Common Mode Voltage | GNDECL − 2.0 | | GNDECL − 0.5 | V | |
| $I_{IH}$ | Input HIGH Current $E_0$–$E_3$, $\overline{E}_0$–$\overline{E}_3$ OE, LE, DIR | | | 300 35 | µA | $V_{IN} = V_{IH(Max)}$ |
| $I_{CEX}$ | Output HIGH Leakage Current | | | 50 | µA | $V_{OUT} = V_{TTL}$ |
| $I_{ZZ}$ | Bus Drainage Test | | | 500 | µA | $V_{OUT} = 5.25V$ $V_{TTL} = 0.0V$ |
| $I_{IL}$ | Input LOW Current | 0.50 | | | µA | $V_{IN} = V_{IL(Min)}$ |
| $I_{OZHT}$ | 3-STATE Current Output HIGH | | | 70 | µA | $V_{OUT} = +2.7V$ |
| $I_{OZLT}$ | 3-STATE Current Output LOW | −650 | | | µA | $V_{OUT} = +0.5V$ |
| $I_{OS}$ | Output Short-Circuit Current | −100 | | −225 | mA | $V_{OUT} = 0.0V$, $V_{TTL} = +5.5V$ |
| $I_{TTL}$ | $V_{TTL}$ Supply Current | | | 39 | mA | TTL Outputs LOW |
| | | | | 27 | mA | TTL Outputs HIGH |
| | | | | 39 | mA | TTL Outputs in 3-STATE |

**Note 11:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.
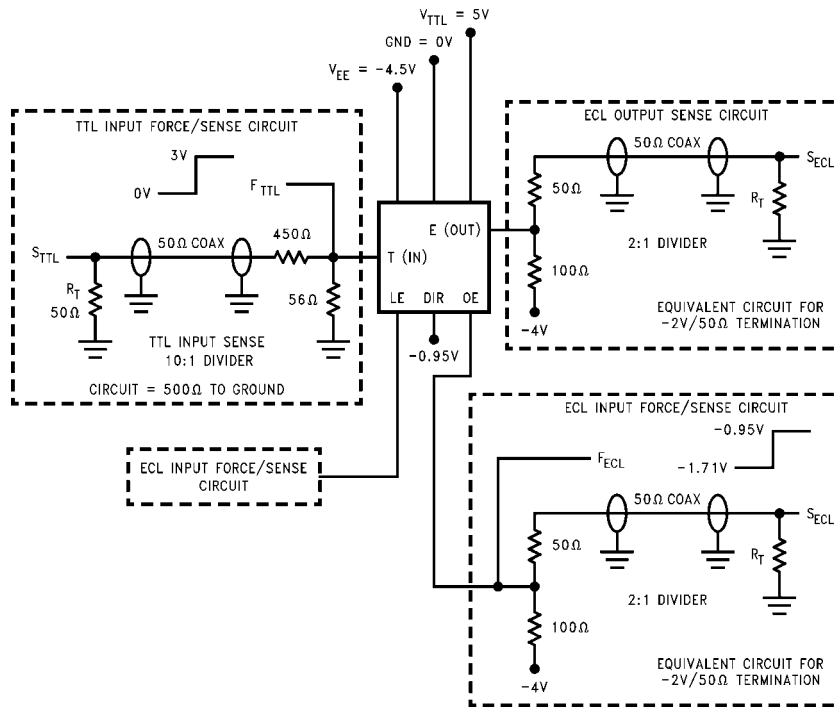
## PCC TTL-to-ECL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{TTL} = +4.5V$ to $+5.5V$

| Symbol | Parameter | $T_C = -40°C$ Min | $T_C = -40°C$ Max | $T_C = +25°C$ Min | $T_C = +25°C$ Max | $T_C = +85°C$ Min | $T_C = +85°C$ Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | 180 | | 180 | | 180 | | MHz | |
| $t_{PLH}$ $t_{PHL}$ | $T_n$ to $E_n$, $\overline{E}_n$ (Transparent) | 0.9 | 2.4 | 0.8 | 2.2 | 0.7 | 2.5 | ns | Figures 1, 3 |
| $t_{PLH}$ $t_{PHL}$ | LE to $E_n$, $\overline{E}_n$ | 1.2 | 2.3 | 1.3 | 2.4 | 1.4 | 2.5 | ns | Figures 1, 3 |
| $t_{PZH}$ | OE to $E_n$, $\overline{E}_n$ (Cutoff to HIGH) | 1.9 | 3.8 | 2.5 | 4.5 | 2.5 | 4.6 | ns | Figures 1, 3 |
| $t_{PHZ}$ | OE to $E_n$, $\overline{E}_n$ (HIGH to Cutoff) | 2.5 | 4.7 | 2.3 | 4.0 | 2.5 | 4.5 | ns | Figures 1, 3 |
| $t_{PHZ}$ | DIR to $E_n$, $\overline{E}_n$ (HIGH to Cutoff) | 1.8 | 3.5 | 2.1 | 3.7 | 2.3 | 4.2 | ns | Figures 1, 3 |
| $t_S$ | $T_n$ to LE | 0.8 | | 0.8 | | 0.8 | | ns | Figures 1, 3 |
| $t_H$ | $T_n$ to LE | 0.6 | | 0.6 | | 0.6 | | ns | Figures 1, 3 |
| $t_{TLH}$ $t_{THL}$ | Transition Time 20% to 80%, 80% to 20% | 0.8 | 2.8 | 0.8 | 2.8 | 0.8 | 2.8 | ns | Figures 1, 3 |

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## Industrial Version (Continued)
## PCC ECL-to-TTL AC Electrical Characteristics

$V_{EE} = -4.2V$ to $-5.7V$, $V_{TTL} = +4.5V$ to $+5.5V$, $C_L = 50$ pF

| Symbol | Parameter | $T_C = -40°C$ | | $T_C = +25°C$ | | $T_C = +85°C$ | | Units | Conditions |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| $f_{MAX}$ | Maximum Clock Frequency | 75 | | 75 | | 75 | | MHz | |
| $t_{PLH}$ | $E_n$, $\overline{E}_n$ to $T_n$ | 1.7 | 4.9 | 1.7 | 5.1 | 1.8 | 5.8 | ns | Figures 2, 4 |
| $t_{PHL}$ | (Transparent) | | | | | | | | |
| $t_{PLH}$ | LE to $T_n$ | 2.2 | 4.3 | 2.2 | 4.0 | 2.3 | 4.1 | ns | Figures 2, 4 |
| $t_{PHL}$ | | 3.3 | 5.2 | 3.4 | 5.4 | 3.8 | 6.1 | | |
| $t_{PZH}$ | OE to $T_n$ | 3.1 | 5.6 | 3.3 | 5.7 | 3.6 | 6.3 | ns | Figures 2, 5 |
| $t_{PZL}$ | (Enable Time) | 4.8 | 8.3 | 5.1 | 8.5 | 5.6 | 9.2 | | |
| $t_{PHZ}$ | OE to $T_n$ | 3.5 | 9.2 | 3.5 | 8.3 | 3.5 | 7.5 | ns | Figures 2, 5 |
| $t_{PLZ}$ | (Disable Time) | 3.2 | 7.3 | 3.5 | 6.7 | 3.6 | 6.7 | | |
| $t_{PHZ}$ | DIR to $T_n$ | 3.5 | 8.8 | 3.5 | 8.1 | 3.5 | 7.6 | ns | Figures 2, 6 |
| $t_{PLZ}$ | (Disable Time) | 3.2 | 7.2 | 3.4 | 6.7 | 3.6 | 6.7 | | |
| $t_S$ | $E_n$, $\overline{E}_n$ to LE | 0.6 | | 0.6 | | 0.6 | | ns | Figures 2, 4 |
| $t_H$ | $E_n$, $\overline{E}_n$ to LE | 0.7 | | 0.7 | | 0.7 | | ns | Figures 2, 4 |
| $t_{PW}(L)$ | Pulse Width LE | 2.0 | | 2.0 | | 2.0 | | ns | Figures 2, 4 |

# Test Circuitry (TTL-to-ECL)



**Notes:**

$R_t$ = 50Ω termination. When an input or output is being monitored by a scope, $R_t$ is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, and external 50Ω resistance must be applied to serve as $R_t$.

TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

$V_{TTL}$ is decoupled to ground with 0.1 μF to ground, $V_{EE}$ is decoupled to ground with 0.01 μF and GND is connected to ground.

For ECL input pins, the equivalent force/sense circuitry is optional.

**FIGURE 1. TTL-to-ECL AC Test Circuit**

# Switching Waveforms (TTL-to-ECL)
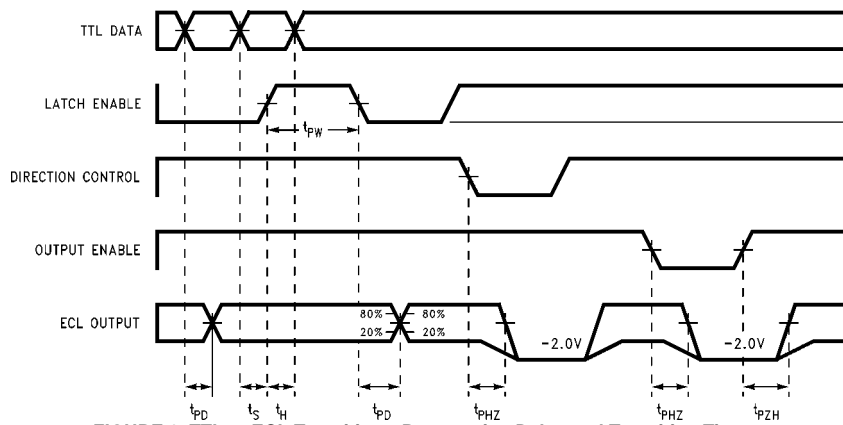


**FIGURE 2. TTL to ECL Transition—Propagation Delay and Transition Times**
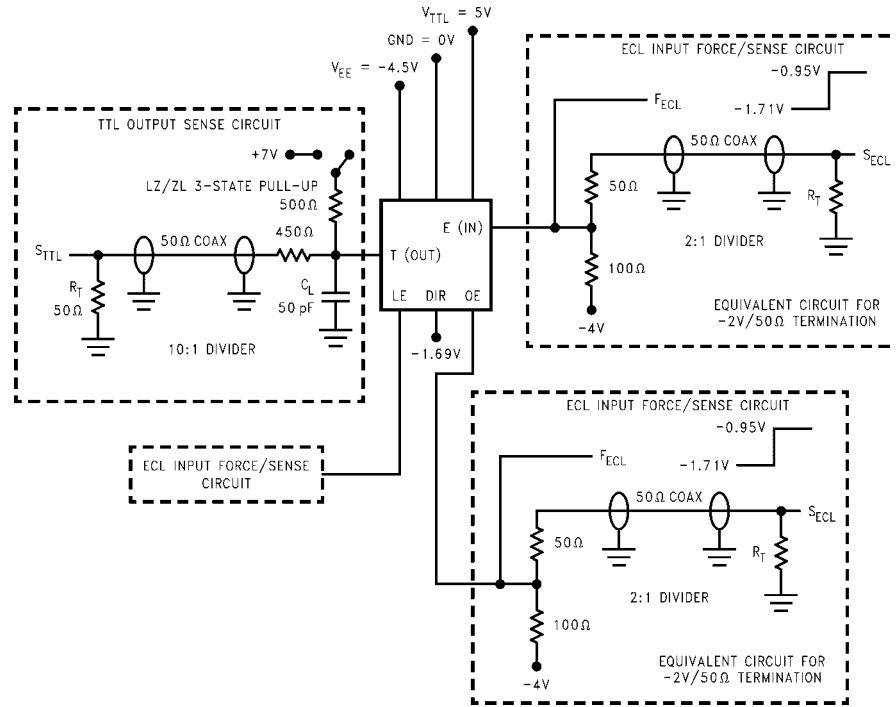
# Test Circuitry (ECL-to-TTL)



**Notes:**

$R_t$ = 50Ω termination. When an input or output is being monitored by a scope, $R_t$ is supplied by the scope's 50Ω resistance. When an input or output is not being monitored, and external 50Ω resistance must be applied to serve as $R_t$.

The TTL 3-STATE pull up switch is connected to +7V only for ZL and LZ tests.

TTL and ECL force signals are brought to the DUT via 50Ω coax lines.

$V_{TTL}$ is decoupled to ground with 0.1 µF to ground, $V_{EE}$ is decoupled to ground with 0.01 µF and GND is connected to ground.
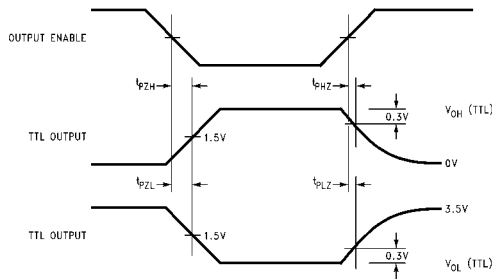
**FIGURE 3. ECL-to-TTL AC Test Circuit**
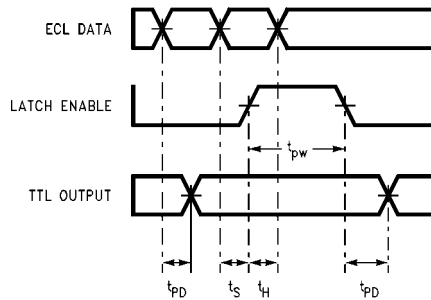


**Note:**
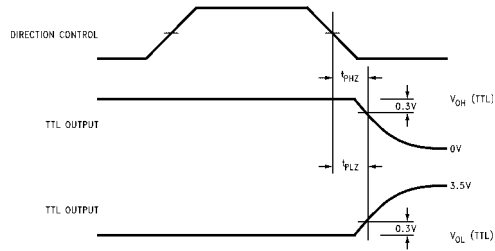
DIR is LOW, and OE is HIGH

**FIGURE 4. ECL-to-TTL Transition—Propagation Delay and Transition Times**

## Test Circuitry (ECL-to-TTL) (Continued)



**Note:**

DIR is LOW, LE is HIGH

**FIGURE 5. ECL-to-TTL Transition, OE to TTL Output, Enable and Disable Times**



**Note:**

OE is HIGH, LE is HIGH

**FIGURE 6. ECL-to-TTL Transition, DIR to TTL Output, Disable Time**

## Applications



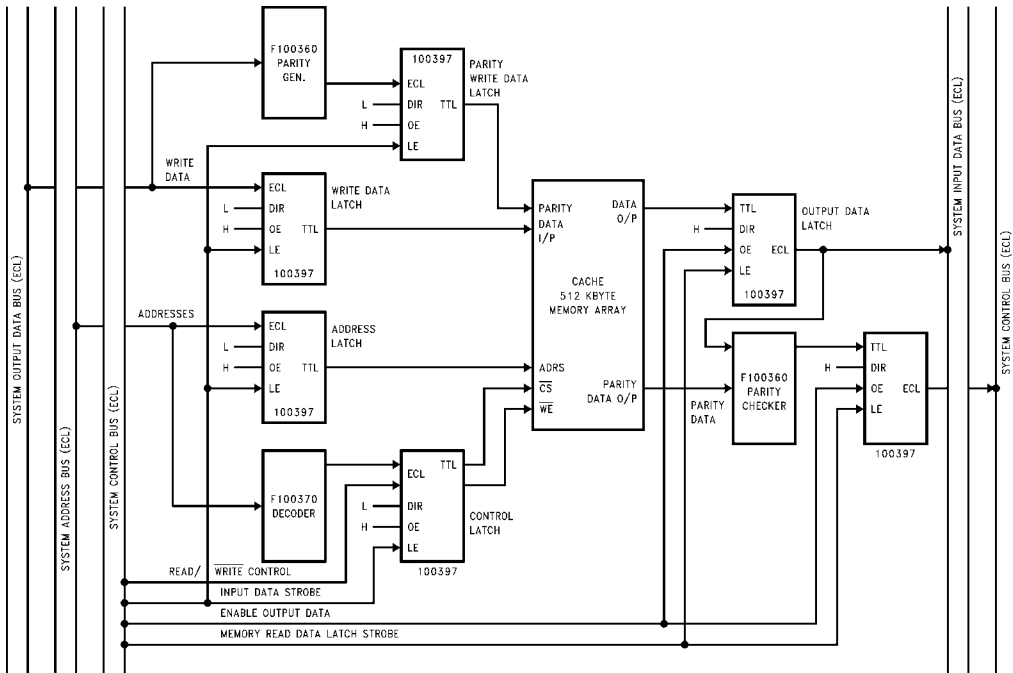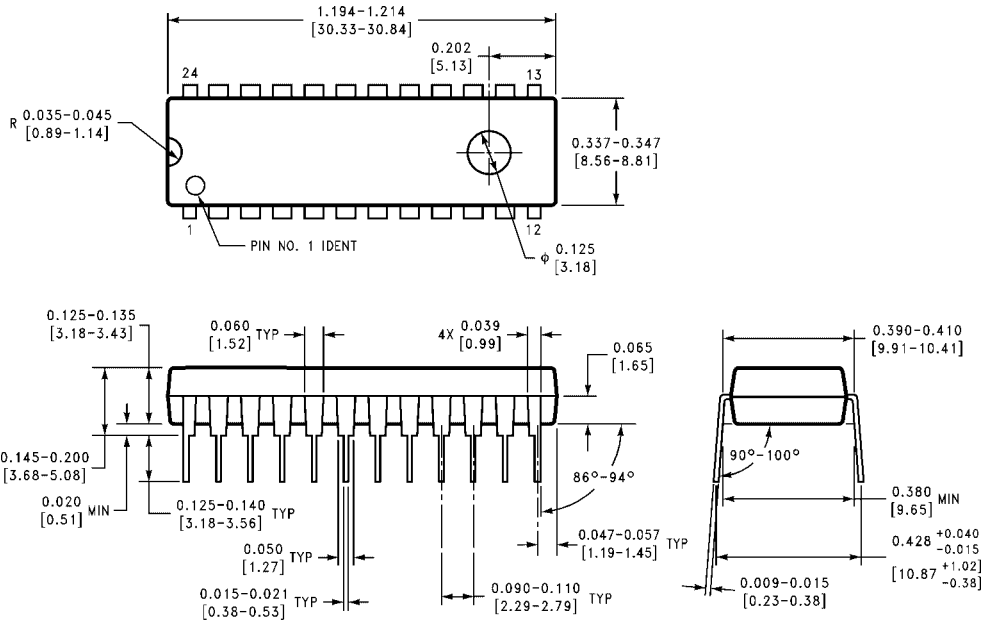**FIGURE 7. Applications Diagram—MOS/TTL SRAM Interface Using 100397 ECL–TTL Latched Translator**

# Physical Dimensions inches (millimeters) unless otherwise noted



1.194−1.214
[30.33−30.84]

0.202
[5.13]

24   13

R 0.035−0.045
[0.89−1.14]

0.337−0.347
[8.56−8.81]

1   12

PIN NO. 1 IDENT

φ 0.125
[3.18]

0.125−0.135
[3.18−3.43]

0.060 TYP
[1.52]

4X 0.039
[0.99]

0.065
[1.65]

0.390−0.410
[9.91−10.41]

0.145−0.200
[3.68−5.08]

0.020 MIN
[0.51]

0.125−0.140 TYP
[3.18−3.56]

86°−94°

90°−100°

0.380 MIN
[9.65]

0.050 TYP
[1.27]

0.047−0.057 TYP
[1.19−1.45]

0.428 +0.040 −0.015
[10.87 +1.02 −0.38]

0.015−0.021 TYP
[0.38−0.53]

0.090−0.110 TYP
[2.29−2.79]

0.009−0.015
[0.23−0.38]

N24E (REV A)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide**
**Package Number N24E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
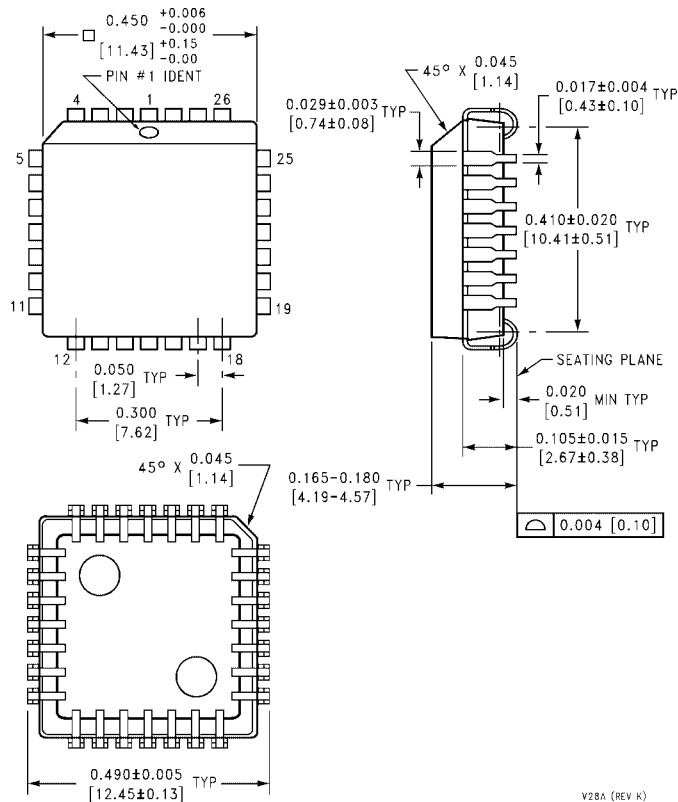


**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square**
**Package Number V28A**

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