

FEATURES

- 12-Bit Resolution
- 10 MSPS Sampling Rate
- On Chip Bandgap Reference
- $DNL = \pm 0.4 \text{ LSB}$, $INL = \pm 1.7 \text{ LSB}$
- Internal S/H Function
- Single Power Supply: 5V
- Differential Input
- 100% Digital Test Coverage
- Low Power: 360mW
- Latch-Up Free

- ESD Protection: 2kV Minimum
- Power Down Mode (<1mW)
- 3 State Digital Outputs

APPLICATIONS

- Digital Scanners and Cameras
- Digital Copiers
- IR Image Digitizers
- Wireless Communications
- Video Capture
- XDSL Applications

GENERAL DESCRIPTION

The XRD6621 is a 12-bit Analog-to-Digital Converter. Designed using a standard 5V CMOS process, this part offers excellent performance, low power consumption and latch-up free operation.

The XRD6621 uses a fully pipelined architecture. Each stage is composed of a 1-bit analog-to-digital sub-converter (ADSC), a 1-bit digital-to-analog sub-converter (DASC), and a summing interstage amplifier (IAMP). By using stages with low resolution, high speed operation is possible. Digital correction logic removes any nonlinearity that would normally be caused by IAMP or ADSC offset. Overall ADC linearity depends only on capacitor ratio accuracy, thereby reducing performance variation with

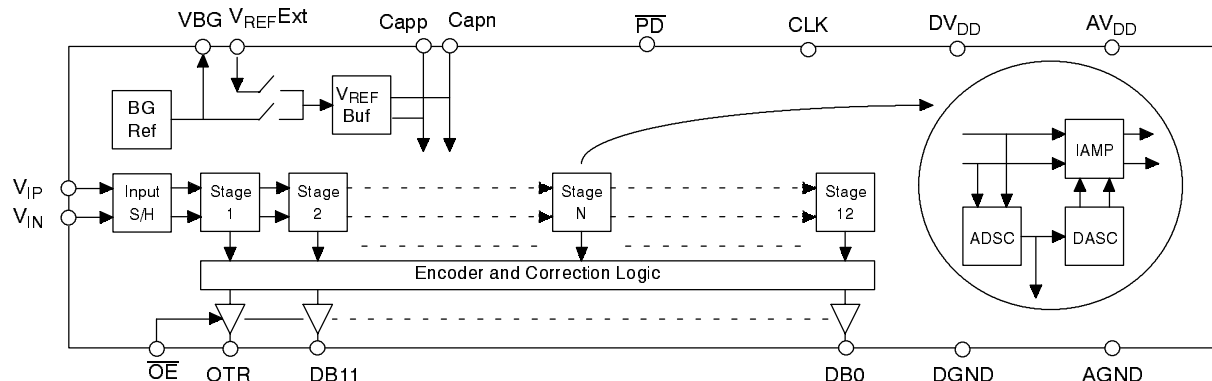
temperature. All internal circuitry is fully differential for improved noise rejection.

An on-chip sample-and-hold (S/H) minimizes the input "kick-back", thereby reducing ADC input driver requirements and improves accuracy for high frequency inputs. A high accuracy on-chip reference is also provided.

The device operates from a single +5V supply. Typical power consumption is 360mW at FS=10MSPS.

The XRD6621 is specified for operation over the industrial (0 to +85°C) temperature range.

BLOCK DIAGRAM

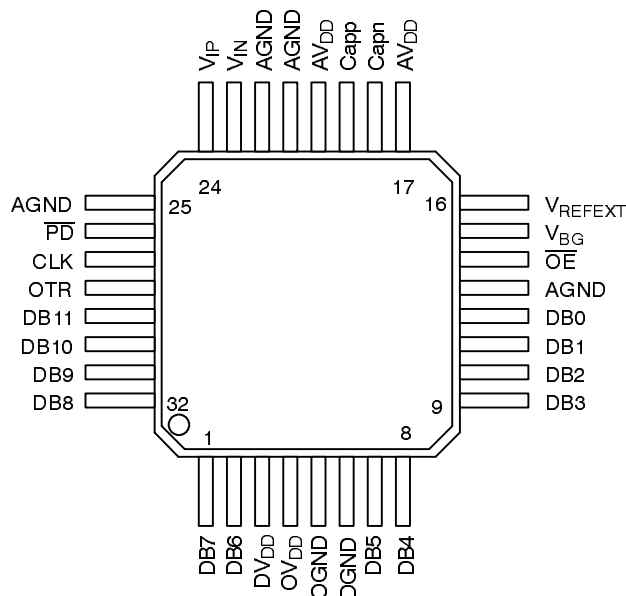


Graph 1 . Block Diagram

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XRD6621AI/Q	32-pin TQFP (7 x 7 x 1.4mm)	0 to +85°C
XRD6621AI/Q44	44-pin QFP (10 x 10 x 2.0mm)	0 to +85°C

PIN CONFIGURATION



32 Lead TQFP (7 x 7 x 1.4mm)

PIN DESCRIPTION

32 Pin TQFP

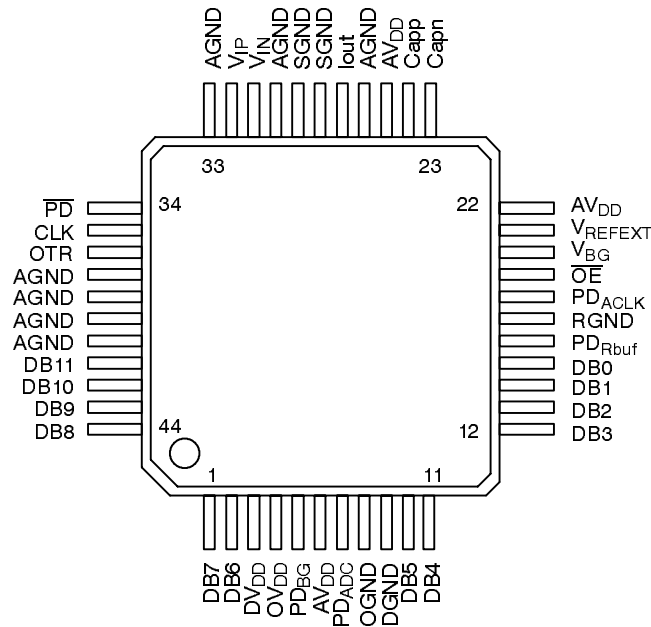
Pin #	Symbol	Description
1	DB7	Data Output Bit 7.
2	DB6	Data Output Bit 6.
3	DV _{DD}	Digital Power Supply (Internal Decode Logic).
4	OV _{DD}	Digital Power Supply (Output Drivers).
5	OGND	Digital Ground (Output Drivers).
6	DGND	Digital Ground (Internal Decode Logic).
7	DB5	Data Output Bit 5.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
8	DB4	Data Output Bit 4.
9	DB3	Data Output Bit 3.
10	DB2	Data Output Bit 2.
11	DB1	Data Output Bit 1.
12	DB0	Data Output Bit 0 (LSB).
13	AGND	Analog Ground.
14	\overline{OE}	Output Enable Control.
15	V _{BG}	Internal Bandgap Reference Voltage.
16	V _{REFEXT}	External Reference Input.
17	A _V DD	Analog Power Supply.
18	Capn	Connect External Decoupling Cap for Negative Reference.
19	Capp	Connect External Decoupling Cap for Positive Reference.
20	A _V DD	Analog Power Supply.
21	AGND	Analog Ground.
22	AGND	Analog Ground.
23	V _{IN}	Differential Negative Input.
24	V _{IP}	Differential Positive Input.
25	AGND	Analog Ground.
26	\overline{PD}	Power Down Control.
27	CLK	Sampling Clock.
28	OTR	Out of Range Indicator.
29	DB11	Data Output Bit 11 (MSB).
30	DB10	Data Output Bit 10.
31	DB9	Data Output Bit 9.
32	DB8	Data Output Bit 8.

PIN DESCRIPTION (CONT'D)

32 Pin TQFP



44 Lead QFP (10mm x 10mm)

PIN DESCRIPTION

44 Pin QFP

Pin #	Symbol	Description
1	DB7	Data Output Bit 7.
2	DB6	Data Output Bit 6.
3	DV _{DD}	Digital Power Supply (Internal Decode Logic).
4	OV _{DD}	Digital Power Supply (Output Drivers).
5	PD _{BG}	Power Down Control for Bandgap Voltage Reference.
6	AV _{DD}	Analog Power Supply.
7	PD _{ADC}	Power Down Control for ADC Core.
8	OGND	Digital Ground (Output Drivers).
9	DGND	Digital Ground (Internal Decode Logic).
10	DB5	Data Output Bit 5.
11	DB4	Data Output Bit 4.
12	DB3	Data Output Bit 3.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
13	DB2	Data Output Bit 2.
14	DB1	Data Output Bit 1.
15	DB0	Data Output Bit 0 (LSB).
16	PD _{RBUF}	Power Down Control for Reference Buffer.
17	RGND	Analog Ground for Chopper-Stabilized Bandgap Reference.
18	PD _{ACLK}	Power Down Control for ADC Clock Generator.
19	\overline{OE}	Output Enable Control.
20	V _{BG}	Internal Bandgap Reference Voltage Output.
21	V _{REFEXT}	External Reference Input.
22	AV _{DD}	Analog Power Supply.
23	Capn	Connect External Decoupling Cap for Negative Reference.
24	Capp	Connect External Decoupling Cap for Positive Reference.
25	AV _{DD}	Analog Power Supply.
26	AGND	Analog Ground.
27	I _{out}	Internal Bias Current Measurement Point. (Default is no Connect).
28	SGND	Analog Ground (Connected to Substrate).
29	SGND	Analog Ground (Connected to Substrate).
30	AGND	Analog Ground.
31	V _{IN}	Differential Negative Input.
32	V _{IP}	Differential Positive Input.
33	AGND	Analog Ground.
34	\overline{PD}	Power Down Control.
35	CLK	Sampling Clock.
36	OTR	Out of Range Indicator.
37	AGND	Analog Ground.
38	AGND	Analog Ground.
39	AGND	Analog Ground.
40	AGND	Analog Ground.
41	DB11	Data Output Bit 11 (MSB).
42	DB10	Data Output Bit 10.
43	DB9	Data Output Bit 9.
44	DB8	Data Output Bit 8.

ELECTRICAL CHARACTERISTICS

Test Conditions: Unless otherwise specified: $AV_{DD} = DV_{DD} = 5V$, FS = 10MHz (50% Duty Cycle); ADCFS = 4VPP,
Using External Reference = 2.48V, $T_A = 25^{\circ}C$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Key Features						
FS	Resolution	12			Bits	
	Maximum Sampling Rate	10			MSPS	
Accuracy						
DNL	Differential Non-Linearity	-0.7	± 0.4	+0.7	LSB	Best Fit
INL	Integral Non-Linearity		± 1.7		LSB	
CMRR	Input Referred Offset		50		mV	$F_{IN}=100KHz$
	Input Referred Gain Error		2		%FS	
	Common Mode Rejection Ratio		64		dB	
	DC PSRR from AV_{DD}		50		dB	
	DC PSRR from DV_{DD}		80		dB	
	Zero Error Drift		15		$\mu V/^{\circ}C$	
	Gain Error Drift		0.003		%FS/ $^{\circ}C$	
Bandgap Reference						
V_{REF}	Reference Voltage	1.10	1.24	1.30	V	
TC_{BG}	TempCo		60		ppm/ $^{\circ}C$	
	Output Impedance		100		k Ω	
Reference Buffer						
TC_{RB}	Gain		1/1.24		V/V	
	TempCo		40		ppm/ $^{\circ}C$	
	Input Impedance		50		k Ω	
Analog Input						
BW	Bandwidth(-1dB)		600		MHz	4VPP full scale max.
V_{ID}	Differential Input Range			$\pm V_{REF}/1.24$	V	
V_{ICM}	Common Mode Input Range	0		AV_{DD}	V	*See Graph 5 .
V_{REFExt}	External Reference Voltage	0.5		2.5	V	
R_{IN}	Input Resistance		*			
C_{IN}	Input Capacitance			10	pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
AC Parameters						
SNR	Signal-to-Noise Ratio ($F_{IN}=1.0\text{MHz}$)	64 63	67 66		dB dB	XRD6621AIQ44 XRD6621AIQ
SNR	Signal-to-Noise Ratio ($F_{IN}=3.6\text{MHz}$)	62	66		dB	Both packages
SNR	Signal-to-Noise Ratio ($F_{IN} = 10\text{MHz}$)		62		dB	
THD	Total Harmonic Distortion ($F_{IN}=1.0\text{MHz}$)	70			dB	
THD	Total Harmonic Distortion ($F_{IN}=3.6\text{MHz}$)	60			dB	
SINAD	SNR + Distortion ($F_{IN} = 1.0\text{ MHz}$)	63 62	66 65		dB dB	XRD6621AIQ44 XRD6621AIQ
SINAD	SNR + Distortion ($F_{IN} = 3.6\text{ MHz}$)	60	64		dB	Both packages
SINAD	SNR + Distortion ($F_{IN} = 10\text{ MHz}$)		60		dB	
ENOB	Effective Bits ($F_{IN}=1.0\text{MHz}$)		10.7		Bits	
ENOB	Effective Bits ($F_{IN}=3.6\text{MHz}$)		10.7		Bits	
ENOB	Effective Bits ($F_{IN} = 10\text{MHz}$)		9.7		Bits	
IMD	Intermodulation Distortion	-64	-67		dBc	
SFDR	Spurious-Free Dynamic Range	75	80		dBc	$F_{IN} = 1.0\text{MHz}$
DG	Differential Gain		0.5		%	
DP	Differential Phase		0.1		°	
FPBW	Full Power Bandwidth		70		MHz	
t_{AP}	Aperture Delay Time		3		ns	
Δt_a	Aperture Jitter		7		ps-rms	
Digital Inputs						
V_{IH}	Digital Input High Voltage	$AV_{DD}-1$			V	
V_{IL}	Digital Input Low Voltage			1	V	
I_{IN}	DC Leakage Currents		70		μA	
	Input Capacitance		10		pF	
Digital Outputs						
V_{OH}	Output High Voltage	$DV_{DD}-0.5$			V	$C_L = 75\text{pF}, R_L = 1\text{m}\Omega$
V_{OL}	Output Low Voltage			0.4	V	$C_L = 75\text{pF}, R_L = 1\text{m}\Omega$
C_L	Max Capacitive Load		75		pF	

ELECTRICAL CHARACTERISTICS (CONT'D)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I _{OZ}	High-Z Leakage	-10		10	μA	Relationship between CLK and data output
t _{DL}	Data Valid Delay		18		ns	
t _{DEN}	Data Enable Delay		10		ns	
t _{DHZ}	Data High-Z Delay		8		ns	
	Pipeline Delay (Latency)		6		cycles	
Power Supplies						
PDI _{DD}	Power Down (I _{DD})		500		μA	
AV _{DD}	Operating Voltage		5		V	
DV _{DD}	Digital Supply Voltage		5		V	
OV _{DD}	Digital Output Voltage				DV _{DD}	
I _{VDD}	Supply Current		72	75	mA	

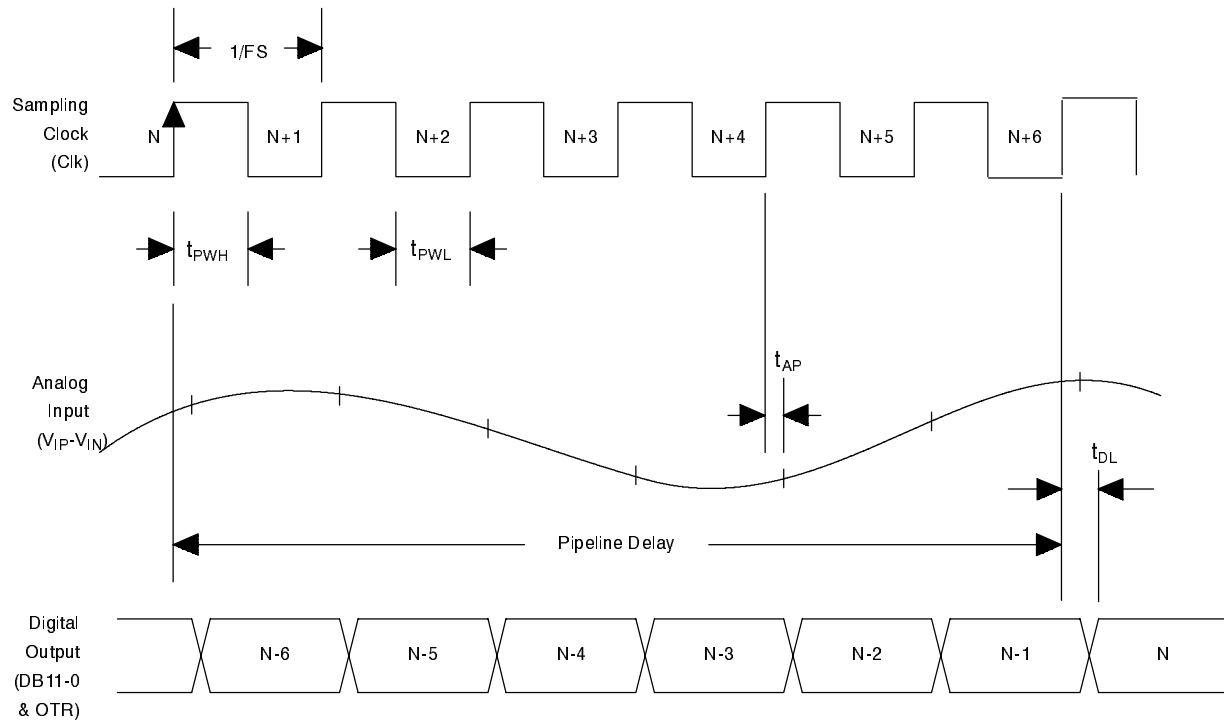
Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (TA = +25°C unless otherwise noted)^{1, 2, 3}

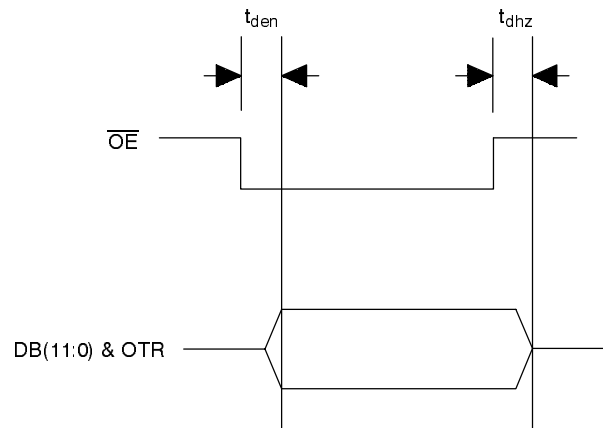
V_{DD} to GND +7.0V	Package Power Dissipation Rating to 75°C
V_{RT} & V_{RB} $V_{DD} + 0.5$ to GND -0.5V	32-pin TQFP 1000mW
V_{IN} $V_{DD} + 0.5$ to GND -0.5V	Derates above 75°C 18mW/°C
All Inputs $V_{DD} + 0.5$ to GND -0.5V	Lead Temperature (Soldering 10 seconds) .. +300°C
All Outputs $V_{DD} + 0.5$ to GND -0.5V	44-pin PQFP 110°mW
Storage Temperature -65 to +150°C	Derates above 75° C 15mW/°C
		ESD 2KV

Notes:

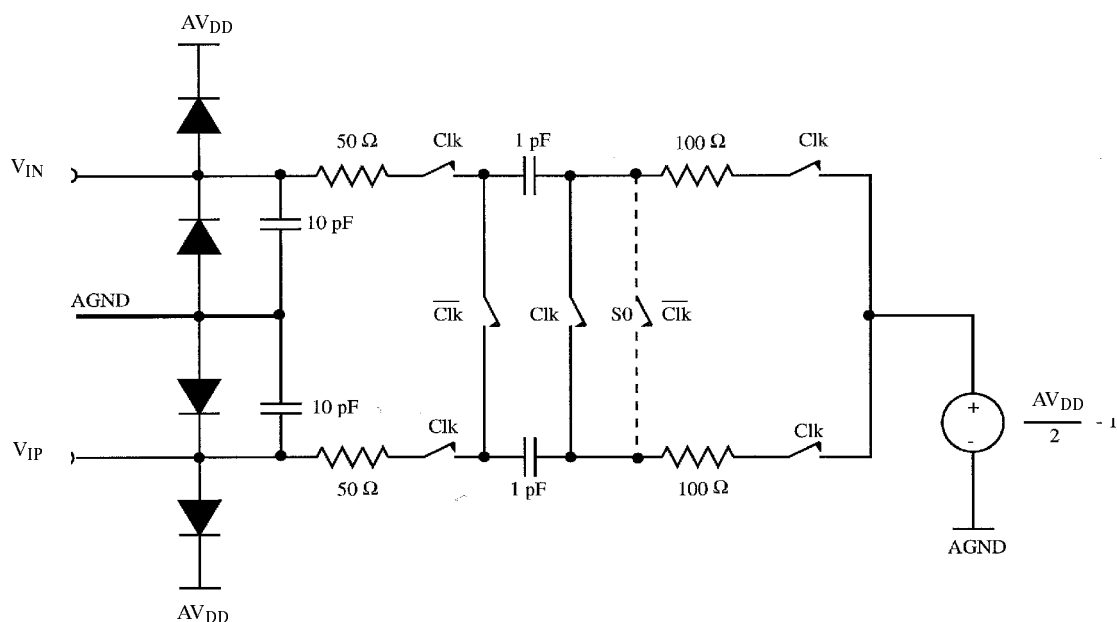
- ¹ Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
- ² Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100 μ s.
- ³ V_{DD} refers to AV_{DD} and DV_{DD} . GND refers to AGND and DGND.



Graph 2 . Timing Diagram



Graph 3 . Data Delay and Data Enable Timing



Graph 5 . Simplified Input Circuit

Out of Range Indicator (OTR)

The out of range indicator is used to indicate a fault condition. This signal will go high if the input exceeds the conversion range of the ADC, i.e. the input is above $+V_{REF}/1.24$ or below $-V_{REF}/1.24$. This bit can be combined with the MSB to indicate if the input is too positive or too negative. This bit will also go high if the correction range of the digital correction logic is exceeded. This is typically caused by running the ADC with a V_{ref} that is too small.

Output Enable ($\overline{\text{OE}}$)

This signal controls the tri-state drivers on the digital outputs DB11-DB0 and OTR. During normal operation $\overline{\text{OE}}$ should be held low so that all outputs are enabled. If $\overline{\text{OE}}$ is driven high DB11-0 and OTR go into high impedance mode. This control operates asynchronous to the clock and will only control the output drivers. The internal output registers will get updated independent of $\overline{\text{OE}}$ setting.

Power Down Control (PD's)

Depending on the package, the XRD6621 has a number of power down modes available. In the 32-pin package, the only control is \overline{PD} . Pulling \overline{PD} signal low will disconnect the input clock, turn off all internal cells and set the output word DB11-0 and OTR to DGND. If high impedance outputs are desired in \overline{PD} mode, \overline{OE} should be pulled high. The turn on time from switching out of power down mode will be set by the time it takes for the internal V_{REF} buffer to charge up the external decoupling caps connected to Capp and Capn. Typically for 2.2 μ F decoupling caps this time will be about 30ms. In the 44-pin package, there are four more power down controls available for different internal cells. Typically these controls would be used only for debugging purposes. Table 1 explains which cell each power down option controls.

Pin Name	Effected Cell
PD _{ADC}	The bias current to the core ADC is shut-down. The master bias generator, reference buffer and bandgap reference will still operate. (44 pin package only)
PD _{RBuf}	The bias current to the reference buffer is shutdown. This allows for an external reference buffer to be used. (44 pin package only)
PD _{BG}	The bias current and clock input to the chopper stabilized bandgap reference is shut off. This reduces power supply noise from the F _{CLK} /20 chopper. (44 pin package only)
PD _{ACLK}	The main input clock is shut off. The bandgap clock is unaffected. (44 pin package only)
\overline{PD}	PD _{BG} , PD _{ACLK} are activated and the output register clock is shut off.

Table 1. Power Down Controls

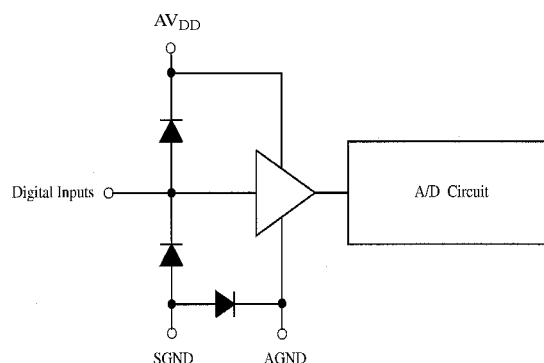
Power Supplies

Internally the XRD6621 contains several independent power supplies. One set of supplies is AV_{DD} and AGND. These supplies connect to all of the sensitive analog and digital circuitry. This circuitry includes the core of the ADC (ADC op-amps and comparators), the master bias generator, the bandgap reference, bandgap reference buffer, and master clock generator. The next supply is DV_{DD} and DGND. This supply is connected to the digital

correction logic. OV_{DD} may be connected to a lower power supply (such as 3.3V or 3.0V) to simplify interfacing to lower voltage logic. DGND may also be lifted above AGND. All of the inputs to the ADC are relative to AV_{DD} . This was done to avoid generating non-50% duty cycle clocks with slow rise/fall time sampling clocks. RGND should be connected to AGND, (44 pin package only). This is the reference ground for V_{BG} and V_{refExt} .

Internally, the bulk node of all NMOS devices (i.e. the substrate) is connect to a separate supply line called SGND. This separate supply line is used to help isolate power supply coupling from AGND and DGND. In the 32-pin package, SGND is connected to AGND. DV_{DD} and DGND are connected only to the internal digital decode logic. OV_{DD} and OGND are connected only to the digital output drivers. Internally, there is also a shielding line that helps to isolate very sensitive nodes. This line is connected internally to AGND.

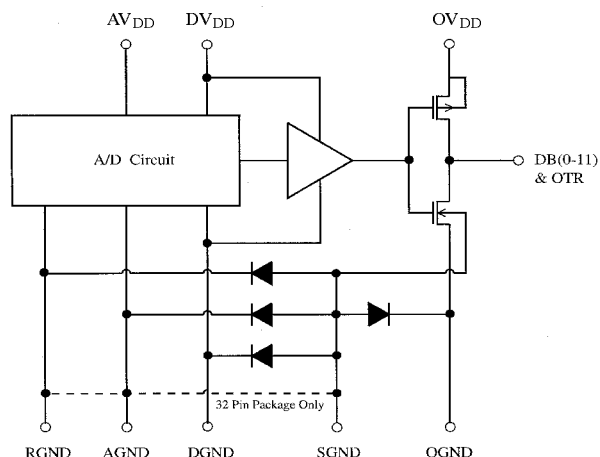
Graph 6 shows the power supply connection as it pertains to digital input pins.



Graph 6 . XRD6621 Power Supply Connection for Digital Inputs.

Logic Output Interface

The digital output drive circuitry of the XRD6621 is designed to operate from the analog and digital supplies. The OV_{DD} pin of the XRD6621 is a separate power supply dedicated to the logic output drivers. OV_{DD} is not connected internally to any of the other power supplies. Graph 7 illustrates the power supply circuitry of the XRD6621.



Graph 7 . XRD6621 Power Supply Circuit Provides a Separate Supply Line for Digital Output Pins

OV_{DD} and OGND connected directly to the digital output pins. OGND is not common to the XRD6621 substrate. The XRD6621 substrate is common to the packages' SGND pins for the 44-pin QFP package and AGND pins for the 32-pin TQFP. Best Spectral performance is obtained with OV_{DD} lowered to 3.3V.

Reference Control (V_{BG}, V_{refExt}, C_{app}, C_{apn})

The XRD6621 includes an onboard chopper stabilized bandgap reference with a nominal output voltage of V_{ref}. The bandgap will not function when the ADC is not clocked.

A high impedance output version of internal bandgap voltage is available on pin V_{BG}. This voltage must be buffered, and should be decoupled to RGND (AGND 32 pin package), before it is used. An external override control is available. If an input below approximately AV_{DD}-1V is applied to V_{refExt} then the external applied voltage is used for V_{ref}. This option allows the use of an alternate bandgap reference or the use of an external op-amp to gain up or to attenuate V_{BG} to change the full scale range of the ADC. V_{REFExt} should be pulled up to AV_{DD} to select the internal bandgap reference voltage.

V_{REF} (either externally applied or from the bandgap reference) is buffered by the reference buffer. This buffer has a nominal gain of 1/1.24 resulting in an input to the ADC of 1V when using the internal reference. A 1V input corresponds to a 2VPP full scale voltage on the ADC. The pins C_{app} and C_{apn} connect to the output of the reference buffer and must be bypassed with capacitors. A parallel combination of a 2.2μF tantalum and a 0.1μF low inductance ceramic capacitor is recommended.

In the 44 pin package it is possible to shut off the reference buffer and connect an external buffer. The reference buffer is shut off by pulling PD_{RBUF} high. In this mode of operation, the external buffer must generate a differential reference voltage centered near AV_{DD}/2.

Digital Testing

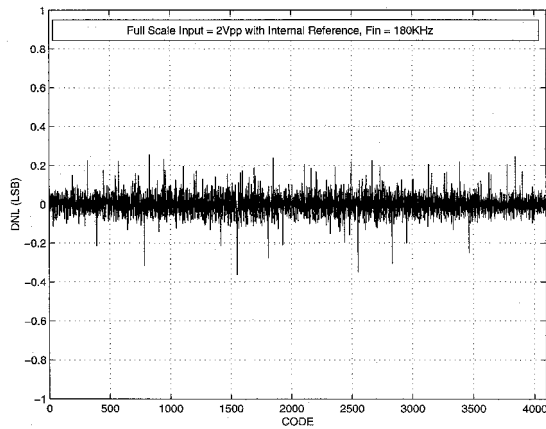
As with any ADC that includes error correction, it is possible that a fault in the digital correction logic would not be detected with standard all codes testing. The XRD6621 includes a special mode that will guarantee 100% stuck-at-fault coverage. To initiate the test, V_{BG} should be pulled to AV_{DD} and a positive full scale input should be applied. The output code should be verified to be DB11=1, DB10-0=0. That, in combination with the standard all codes test, will ensure 100% stuck-at-fault coverage. This test is performed on all parts shipped.

Default Modes

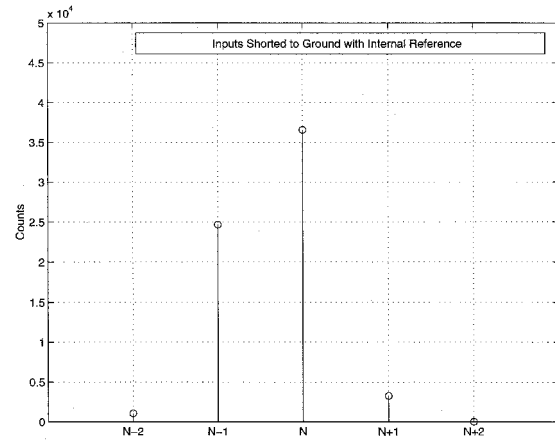
Default settings are provided for all options through the use of internal 100kΩ equivalent pull-up or pull-down resistors. Table 2 shows the default settings.

Pin Name	Default Setting
PD _{ADC}	SGND - Core of ADC is on
PD _{Rbuf}	SGND - Reference buffer is on
PD _{BG}	SGND - Bandgap reference is on
PD _{ACLK}	SGND - Two phase clock generator is running
\overline{OE}	SGND - Outputs are enabled
\overline{PD}	AV _{DD} - part is powered on

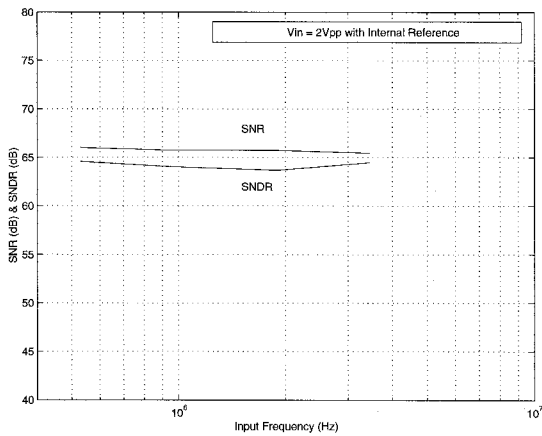
Table 2. Default Digital Control Settings



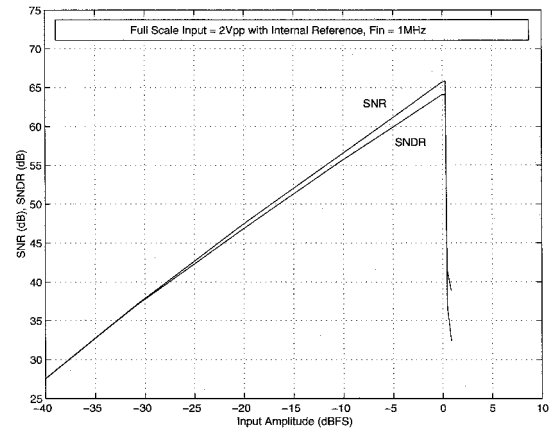
Graph 1 . DNL Vs. Code



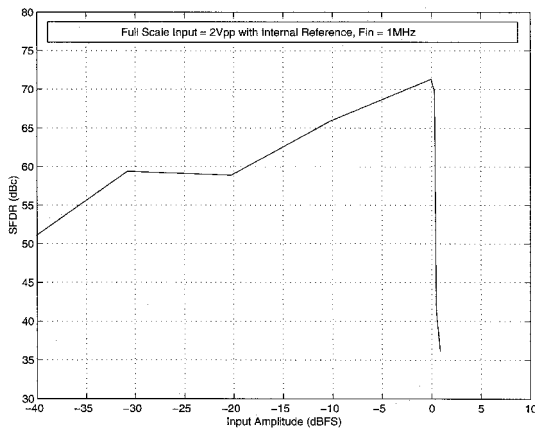
Graph 4 . SFDR vs. Input Amplitude



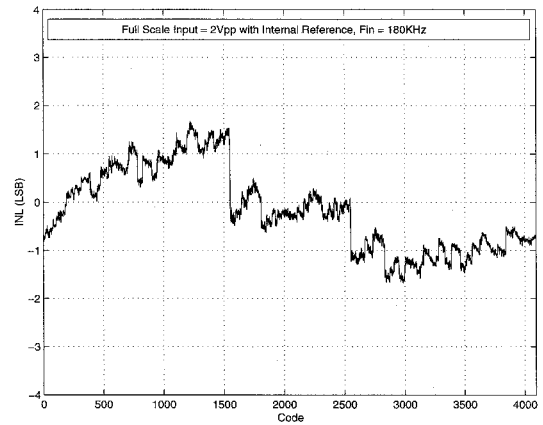
Graph 2 . SNR and SNDR vs. Fin, Internal Reference



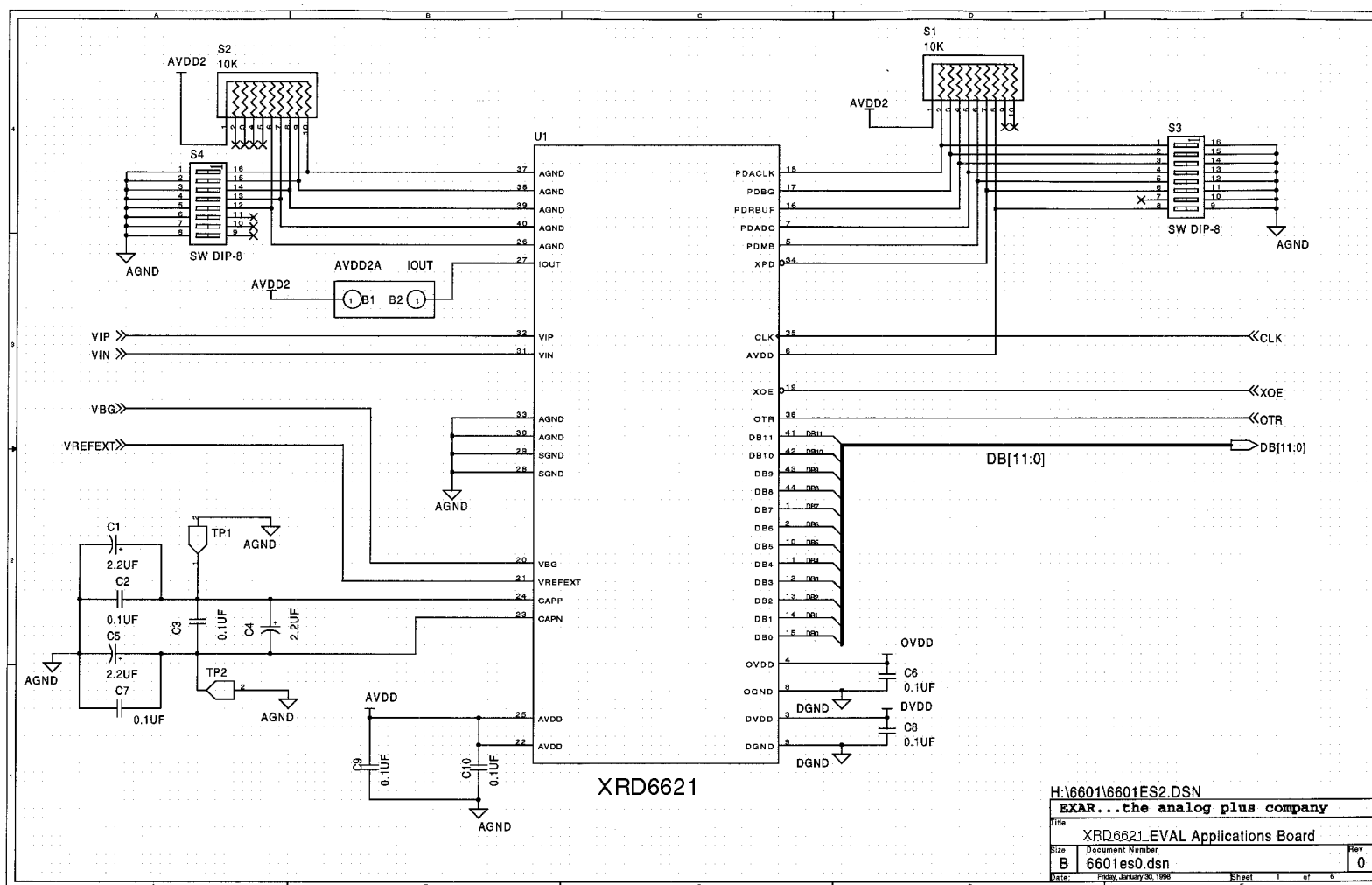
Graph 5 . Best Fit INL Vs. Code

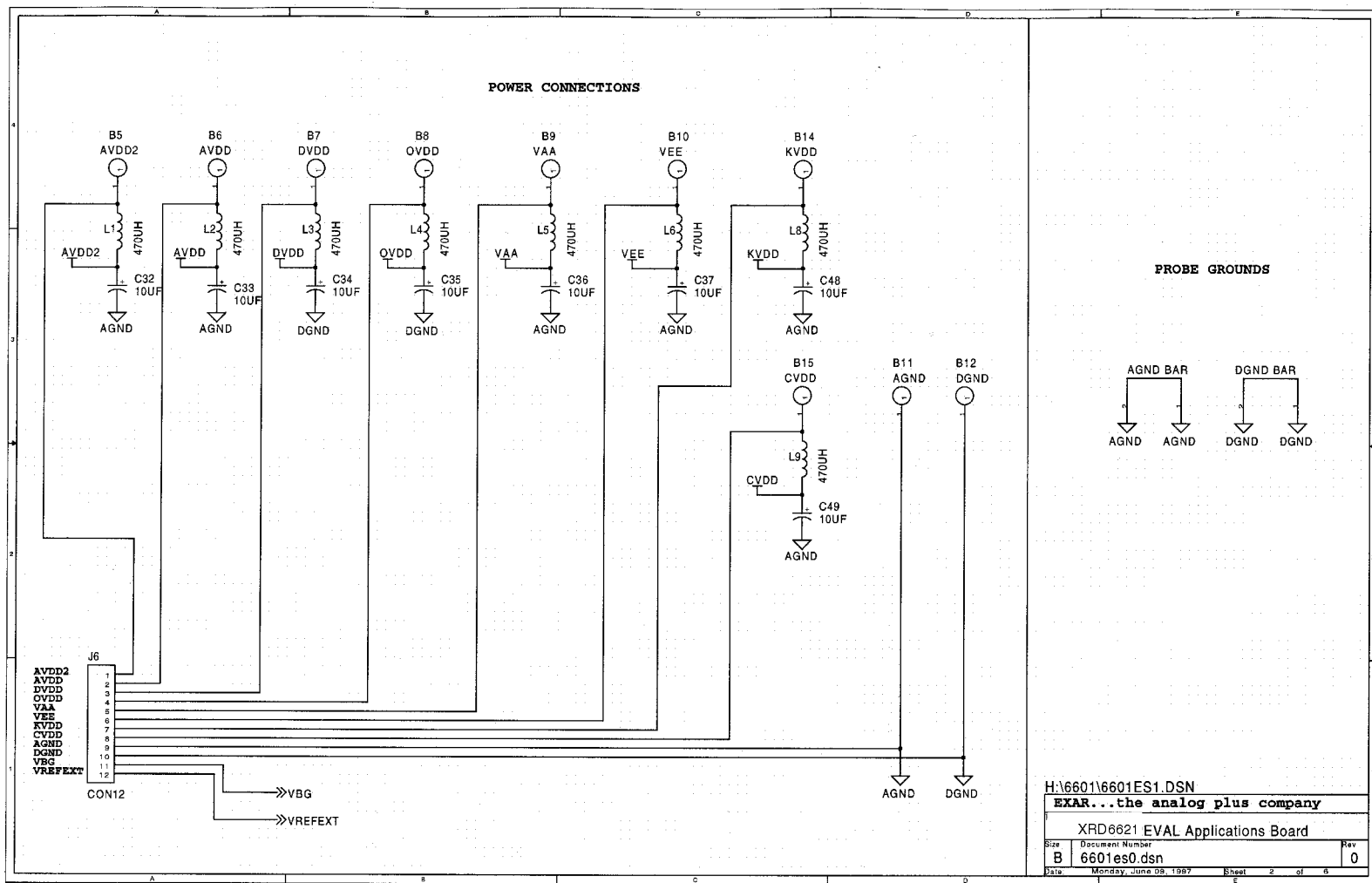


Graph 3 . SNR and SNDR vs. Fin, Input Amplitude



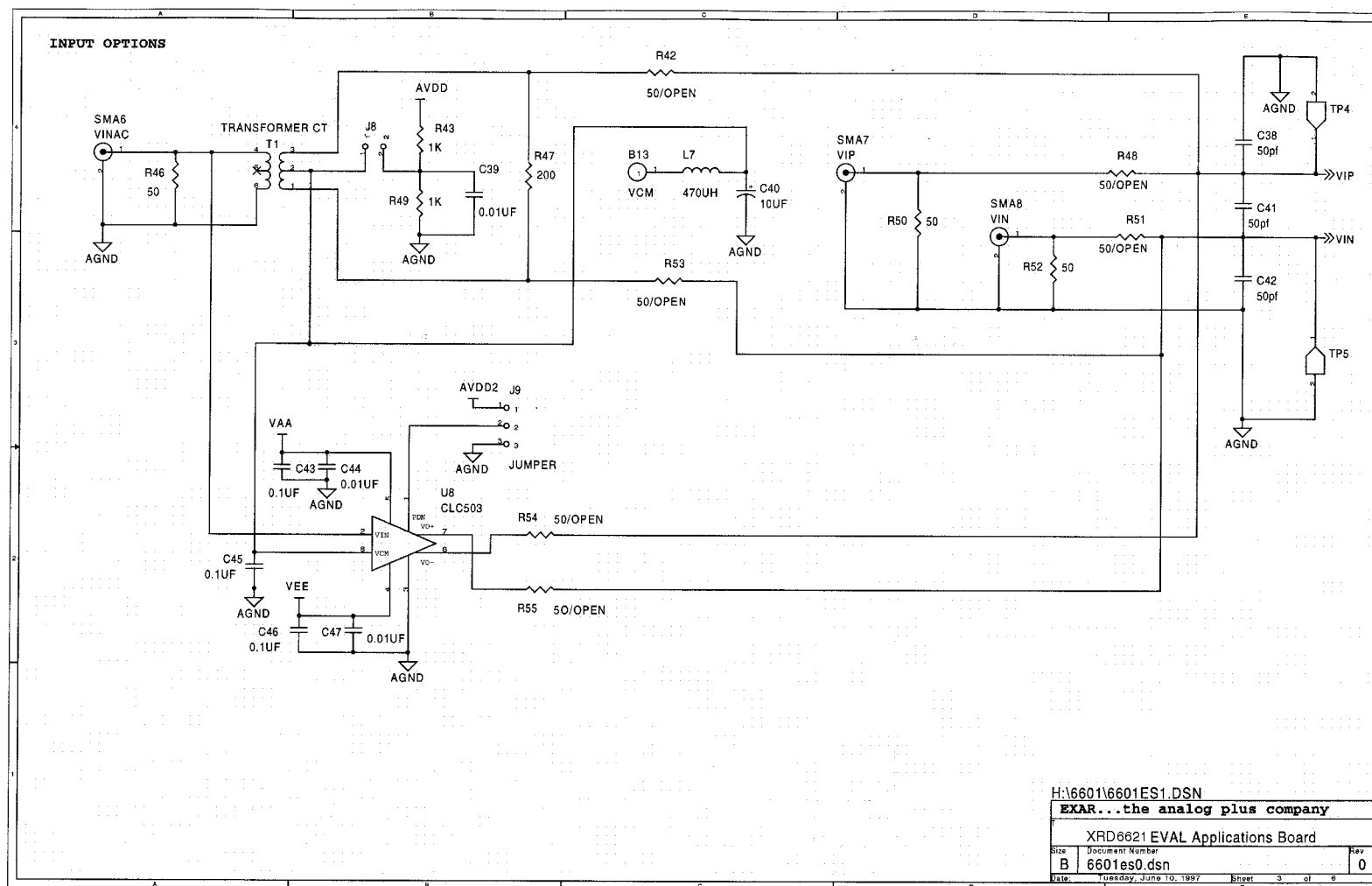
Graph 6 . Output Noise Histogram





H:\6601\6601ES1.DSN		
EXAR...the analog plus company		
XRD6621 EVAL Applications Board		
Size	Document Number	Rev
B	6601es0.dsn	0
Date	Monday, June 08, 1997	Sheet 2 of 6

Graph 8 . Application Schematic Sheet 2 of 6

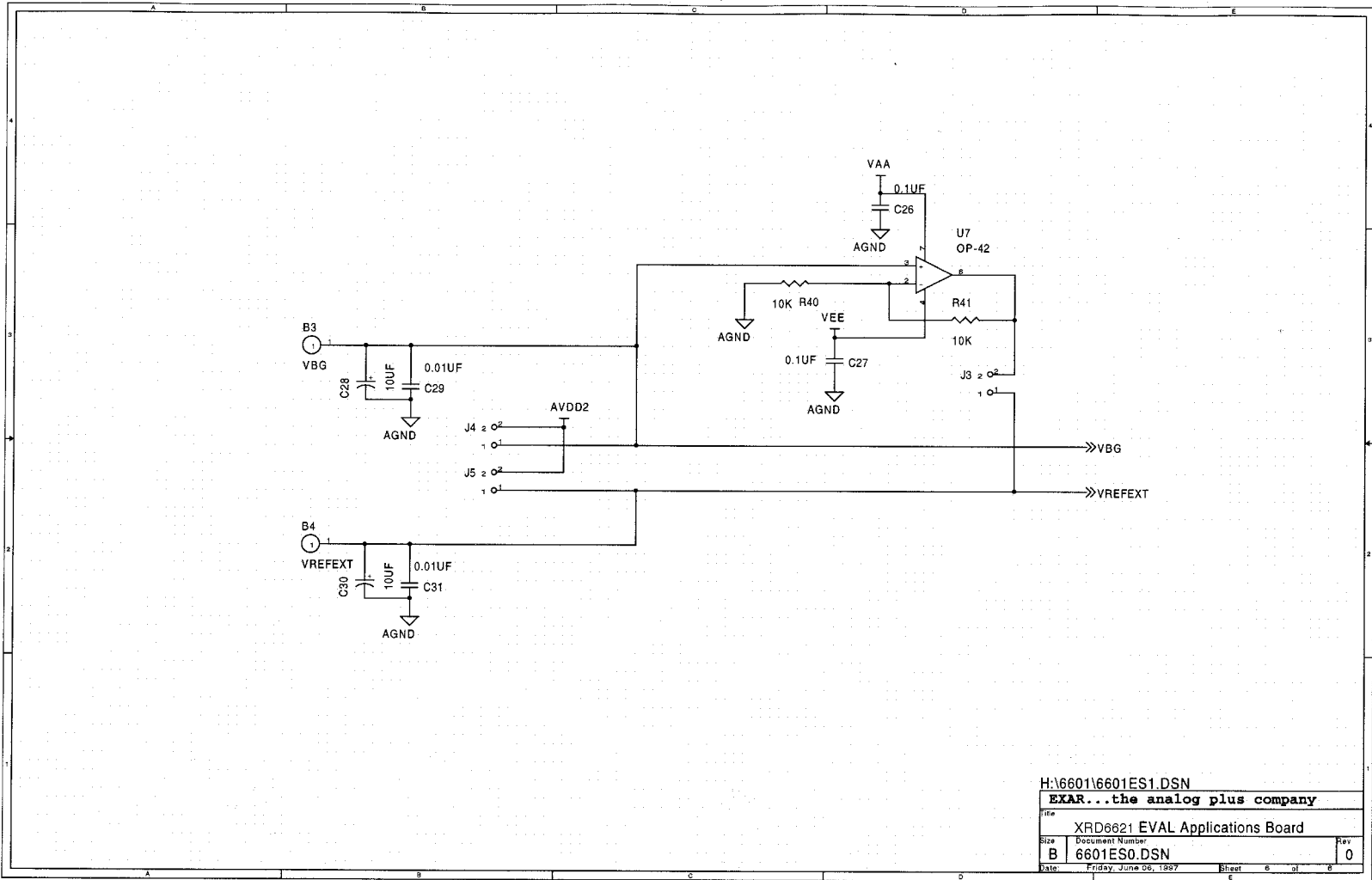


Graph 9 . Application Schematic Sheet 3 of 6



Graph 10 . Application Schematic Sheet 4 of 6

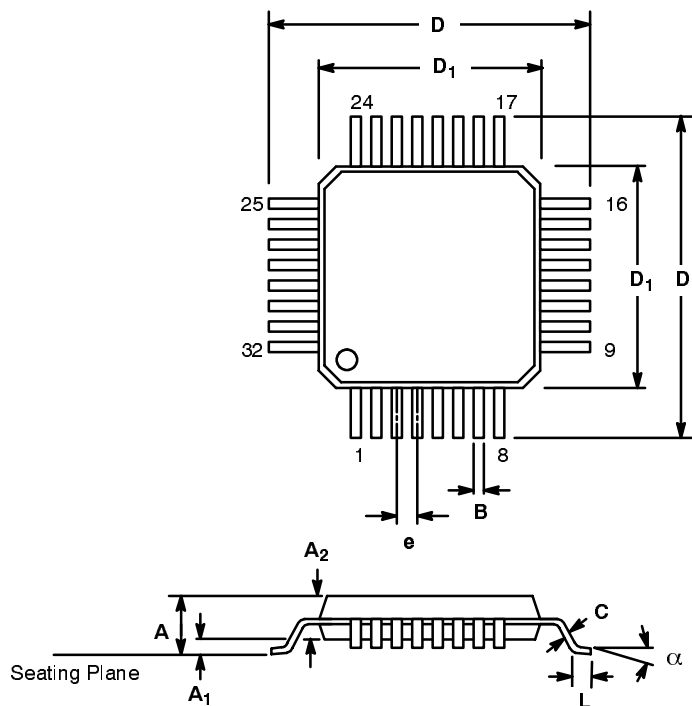




Graph 12 . Application Schematic Sheet 6 of 6

**32 LEAD THIN QUAD FLAT PACK
(7 x 7 x 1.4 mm TQFP)**

Rev. 2.00

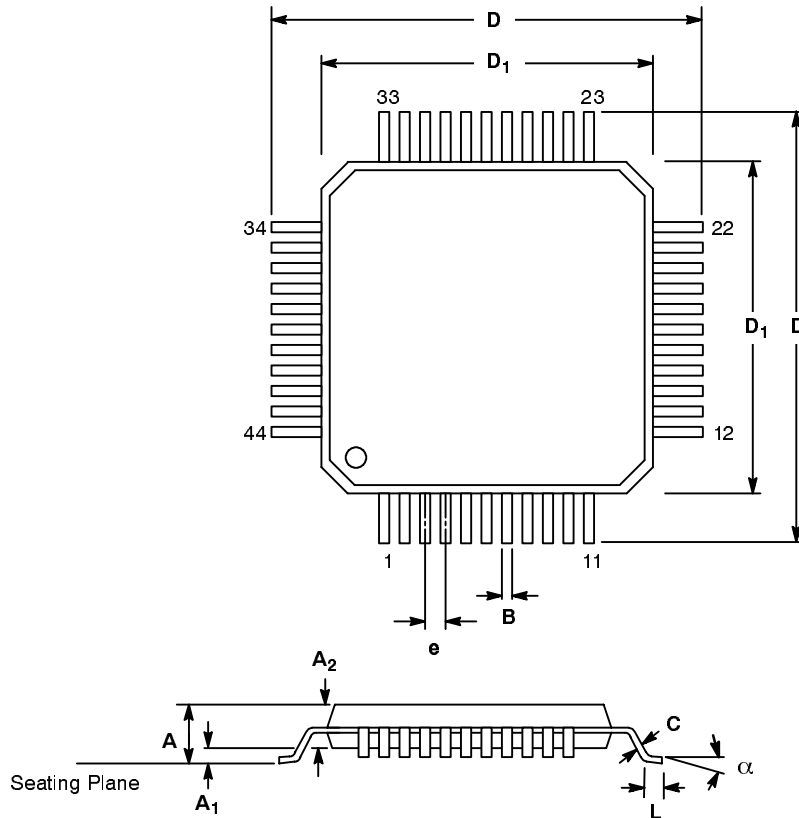


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A ₁	0.002	0.006	0.05	0.15
A ₂	0.053	0.057	1.35	1.45
B	0.012	0.018	0.30	0.45
C	0.004	0.008	0.09	0.20
D	0.346	0.362	8.80	9.20
D ₁	0.272	0.280	6.90	7.10
e	0.0315 BSC		0.80 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

44 LEAD PLASTIC QUAD FLAT PACK (10 mm X 10 mm X 2.0 mm, QFP)

Rev. 1.00



1.95 mm Form

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.078	0.085	1.97	2.35
A ₁	0.001	0.010	0.02	0.25
A ₂	0.077	0.083	1.95	2.00
B	0.012	0.018	0.30	0.45
C	0.005	0.009	0.13	0.23
D	0.537	0.557	13.65	14.15
D ₁	0.390	0.398	9.90	10.10
e	0.0315 BSC		0.80 BSC	
L	0.026	0.037	0.65	0.95
α	0°	7°	0°	7°

Note: The control dimension is the millimeter column

Notes

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 1998 EXAR Corporation
Datasheet January 1998

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.