V96BMC Rev. D

HIGH PERFORMANCE BURST DRAM CONTROLLER FOR i960Cx/Hx/Jx® PROCESSORS

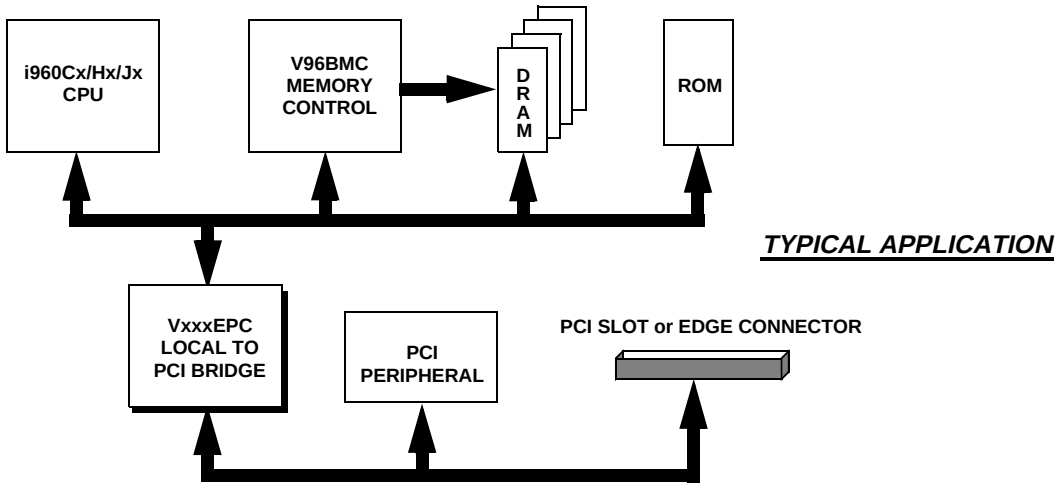
- Pin/Software compatible with earlier V96BMC.
- Direct interfaces to i960Cx/Hx/Jx processors.
- 3.3V DRAM interface support.
- Near SRAM performance achieved with DRAM.
- Supports up to 512Mb of DRAM.
- Interleaved or non-interleaved operation.
- Supports symmetric and non-symmetric arrays.
- Software-configured operational parameters.
- Integrated Page Cache Management.
- 2Kbyte burst transaction support.
- On chip memory address multiplexer/drivers.
- Two 24-bit timers, 8-bit bus watch timer.
- Up to 40MHz operation.
- Low cost 132-pin PQFP package.

The V96BMC Revision D Burst DRAM Controller is an enhanced version of the previous V96BMC with improved timing and provides dedicated Power and Ground rails to support the increasingly popular 3.3V DRAM modules. Timing parameters are also improved over the older versions of the device.

The V96BMC provides the DRAM access protocols, buffer signals, data multiplexer signals, and bus timing resources required to work with DRAM. By using the V96BMC, system designers can replace tedious design work, expensive FPGAs and valuable board space with a single, high-performance, easily configured device. The processor interface of the V96BMC implements the bus protocol of the i960Cx/Hx/Jx. The pin naming convention has been duplicated on the V96BMC; simply wire like-named pins together to create the interface.

The V96BMC supports a total DRAM memory subsystem size of 512Mbytes. The array may be organized as 1 or 2 leafs of 32-bits each. Standard memory sizes of 256Kbit to 64Mbit devices are supported and 8, 16, and 32-bit accesses are allowed. The V96BMC takes advantage of Fast Page Mode or EDO DRAMs and row comparison logic to achieve static RAM performance using dynamic RAMs. Control signals required for optional external data path buffers/latches are also provided by the V96BMC. The V96BMC provides an 8-bit bus watch timer to detect and recover from accesses to unpopulated memory regions.Two 24-bit counters/timers can supply an external interrupt signal at a constant frequency relative to the system clock. The V96BMC is packaged in a low-cost 132-pin PQFP package and is available in 25, 33, or 40MHz versions.

This document contains the product codes, pinouts, package mechanical information, DC characteristics, and AC characteristics for the V96BMC. Detailed functional information is contained in the User's Manual.



TYPICAL APPLICATION

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1.0 Product Codes

Table 1: Product Codes

Product Code	Processor	Bus Type	Package	Frequency
V96BMC-33LP	i960Cx/Hx/Jx	32-bit multiplexed/ demultiplexed	132-pin PQFP	33MHz
V96BMC-40LP	i960Cx/Hx/Jx	32-bit multiplexed/ demultiplexed	132-pin PQFP	40MHz

2.0 Pin Description and Pinout

Table 2 below lists the pin types found on the V96BMC. Table 3 describes the function of each pin on the V96BMC. Table 4 lists the pins by pin number. Figure 1 shows the pinout for the 132-pin PQFP package and Figure 2 shows the mechanical dimensions of the package.

Table 2: Pin Types

Pin Type	Description
I/O_{12}	TTL I/O pin with 12 mA output drive
I	TTL input only pin
O_{12}	TTL Output pin with 12 mA output drive
O_{12-3}	TTL Output pin with 12 mA output drive that can be configured for either 5 volt or 3.3 volt signaling, These outputs can be configured for 3.3V operation by connecting the Vcc3 power pins to a 3.3V power plane (Vcc should always be connected to a 5V supply). Vcc3 can also be connected to the 5V plane if 5V signaling is desired.

Table 3: Signal Descriptions

Memory Interface Signals			
Signal	**Type**	**R[a]**	**Description**
AA[11:0] AB[11:0]	O_{12-3}	X	Leaf A and B row and column address, multiplexed on the same pins. When non-interleaved operation is selected, only address bus AA should be used.
$\overline{\text{RASA[3:0]}}$ $\overline{\text{RASB[3:0]}}$	O_{12-3}	H	Row Address Strobe. These strobes indicate the presence of a valid row address on busses AA(B)[11:0]. These signals are to be connected one to each 32-bit leaf of memory.
$\overline{\text{CASA[3:0]}}$ $\overline{\text{CASB[3:0]}}$	O_{12-3}	H	Column Address Strobe. These strobes latch a column address from AA(B)[11:0]. They are assigned one to each byte in a leaf.
$\overline{\text{MWEA}}$ $\overline{\text{MWEB}}$	O_{12-3}	H	Memory Write Enable. These are the DRAM write strobes. One is supplied for each leaf to minimize signal loading.
$\overline{\text{RFS}}$/AUXT	O_{12}	H	Refresh in progress. This output is multi-function signal. The signal name, as it appears on the logic symbol, is the default signal names. This signal gives notice that a refresh cycle is to be executed. The timing leads RAS only refresh by one cycle. The output may also function as AUX timer interrupt.

Configuration			
Signal	**Type**	**R**	**Description**
$\overline{\text{HMODE}}$	I		Connected to Vcc (for i960Cx) or GND (for i960Hx/Jx).

Buffer Controls Signals			
Signal	**Type**	**R**	**Description**
$\overline{\text{TXA}}$ $\overline{\text{TXB}}$	O_{12}	H	Data Transmit A and B. These outputs are multi-function signals. The signal names, as they appear on the logic symbol, are the default signal names (Mode 0). The purpose of these outputs is to control buffer output enables during data read transactions and, in effect, control the multiplexing of data from each memory leaf onto the i960Cx/Hx/Jx data bus.
$\overline{\text{LEA}}$ $\overline{\text{LEB}}$	O_{12}	L	These outputs are mode independent, however, the timing of the signals change for different operational modes. They control transparent latches that hold data transmitted during a write transaction. In modes 0 and 1, the latch controls follow the timing of $\overline{\text{CAS}}$ for each leaf, while in modes 2 and 3 the timing of $\overline{\text{LEA}}$ and $\overline{\text{LEB}}$ is shortened to 1/2 clock.
Local Bus Interface			

Table 3: Signal Descriptions (cont'd)

Signal	Type	R	Description
A[31:2]	I		Local address bus.
ALE	I		Address Latch Enable: controls a set of transparent latches on the address bus. When asserted high, the address input flows through the latch. When ALE is low, the internal address holds the previous value. With an i960Cx/Hx processor ALE is not typically used and has an internal pull-up resistor that will keep it high when not connected (to provide backward pin compatibility with earlier versions).
D/$\overline{C}$	I		Data/$\overline{Code}$.
$\overline{BE[3:0]}$	I		Local bus byte write enables.
W/$\overline{R}$	I		Write/$\overline{Read}$.
$\overline{READY}$	O_{12}	Z	Local Bus data ready.
$\overline{ADS}$	I		Asserted low to indicate the beginning of a bus cycle
$\overline{DEN}$	I		Data Enable. This input is monitored by the Bus Watch Timer to detect a bus access not returning $\overline{READY}$.
$\overline{SUP}$	I		Indicates supervisor mode. Required for access to configuration registers.
$\overline{BLAST}$	I		Burst last.
$\overline{BTERM}$	O_{12}	Z	Burst terminate. (this signal requires a nominal pull up resistor so that the signal is deasserted when $\overline{RESET}$ goes inactive)
$\overline{BERR}$	O_{12}	H	Bus Time-out error.
$\overline{INT}$	O_{12}	H	Local interrupt request. This signal is asserted when the 24-bit counter reaches terminal count, and interrupt out is enabled. May be programmed for pulse or level operation.
$\overline{RESET}$	I		Local bus reset signal.
PCLK	I		Local bus clock.
ID[2:0]	I		These inputs select the address offset of the configuration registers.
Power and Ground Signals			
Signal	**Type**	**R**	**Description**
Vcc	-		POWER leads intended for external connection to a 5V Vcc plane
Vcc3	-		POWER for DRAM control outputs. Can be connected to 3.3V or 5V.
GND	-		GROUND leads intended for external connection to a GND plane.

a. **R** indicates state during reset.

Table 4: Pin Assignments

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
1	A14	34	$\overline{ADS}$	67	AA10	100	AB9
2	A15	35	$\overline{BE2}$	68	AA11	101	AB10
3	A16	36	$\overline{BE3}$	69	Vcc3	102	AB11
4	Vcc	37	$\overline{BTERM}$	70	GND	103	Vcc3
5	A17	38	$\overline{READY}$	71	$\overline{CASA0}$	104	GND
6	A19	39	ID0	72	$\overline{CASA1}$	105	$\overline{CASB0}$
7	A20	40	ID1	73	$\overline{CASA2}$	106	$\overline{CASB1}$
8	A18	41	ID2	74	$\overline{CASA3}$	107	$\overline{CASB2}$
9	A21	42	$\overline{RFS}$/AUXT	75	Vcc3	108	$\overline{CASB3}$
10	A24	43	$\overline{LEA}$	76	GND	109	Vcc3
11	A22	44	$\overline{LEB}$	77	$\overline{RASA0}$	110	GND
12	A23	45	$\overline{TXA}$	78	$\overline{RASA1}$	111	$\overline{RASB0}$
13	A26	46	$\overline{TXB}$	79	$\overline{RASA2}$	112	$\overline{RASB1}$
14	A25	47	Vcc	80	$\overline{RASA3}$	113	$\overline{RASB2}$
15	A27	48	GND	81	Vcc3	114	$\overline{RASB3}$
16	ALE	49	$\overline{HMODE}$	82	$\overline{MWEA}$	115	Vcc
17	-	50	-	83	-	116	-
18	-	51	-	84	-	117	GND[1]
19	A31	52	-	85	-	118	$\overline{MWEB}$
20	A28	53	AA0	86	GND	119	GND
21	A29	54	AA1	87	AB0	120	$\overline{RESET}$
22	A30	55	AA2	88	AB1	121	A2
23	D/$\overline{C}$	56	AA3	89	AB2	122	A3
24	$\overline{SUP}$	57	Vcc3	90	AB3	123	A4
25	PCLK	58	GND	91	Vcc3	124	A5
26	$\overline{INT}$	59	AA4	92	GND	125	A6
27	$\overline{BERR}$	60	AA5	93	AB4	126	A7

Table 4: Pin Assignments (cont'd)

PIN #	Signal	PIN #	Signal	PIN #	Signal	PIN #	Signal
28	W/$\overline{R}$	61	AA6	94	AB5	127	A8
29	$\overline{BE0}$	62	AA7	95	AB6	128	A9
30	$\overline{DEN}$	63	Vcc3	96	AB7	129	A10
31	$\overline{BLAST}$	64	GND	97	Vcc3	130	A11
32	$\overline{BE1}$	65	AA8	98	GND	131	A12
33	GND	66	AA9	99	AB8	132	A13

1. We recommend connecting PIN # 117 to GND but it is not a must especially for those who are replacing V96BMC rev D in rev AB socket. (This pin was unconnected in rev AB)

Figure 1: Pinout for 132-pin PQFP (top view)

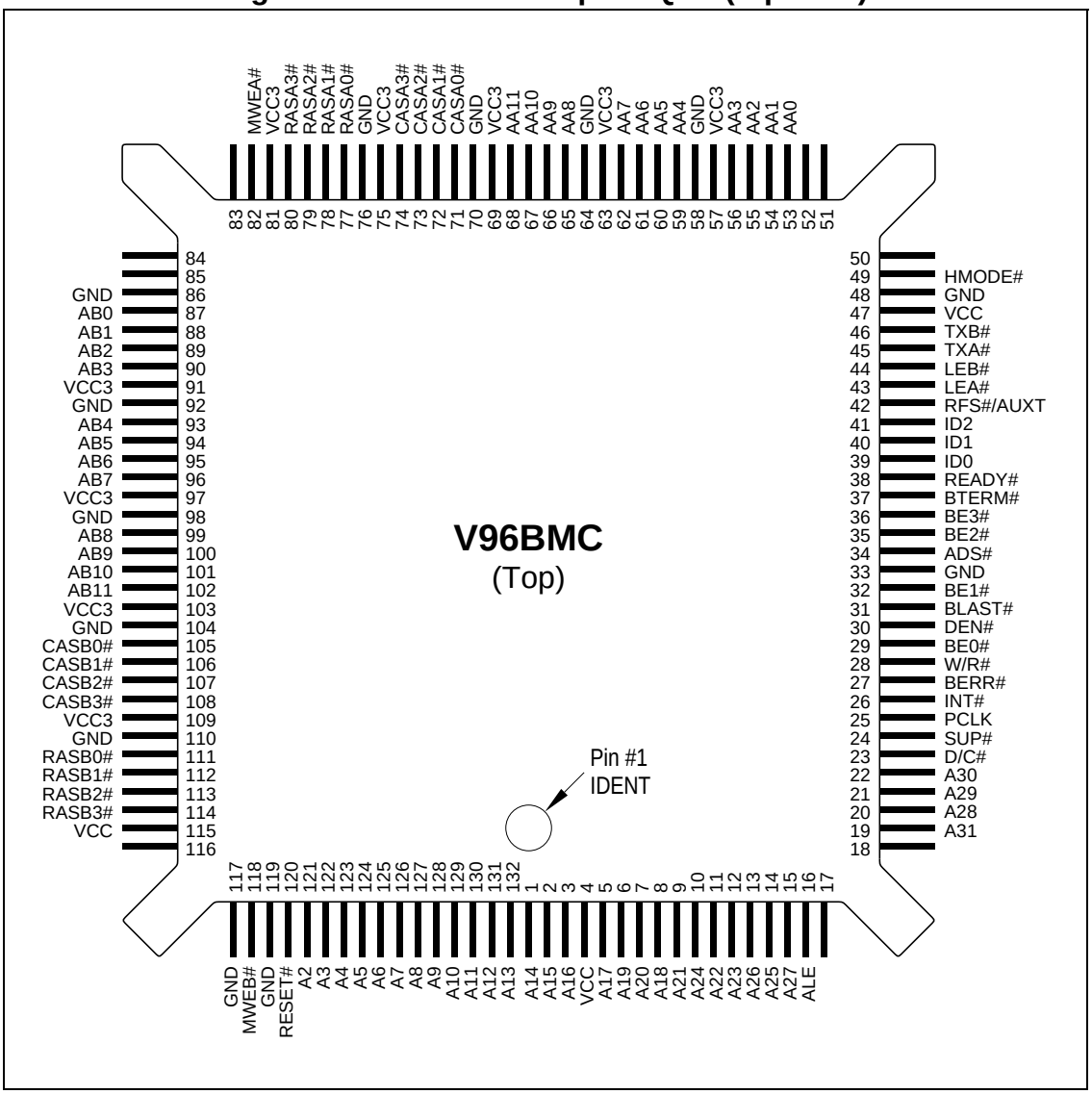
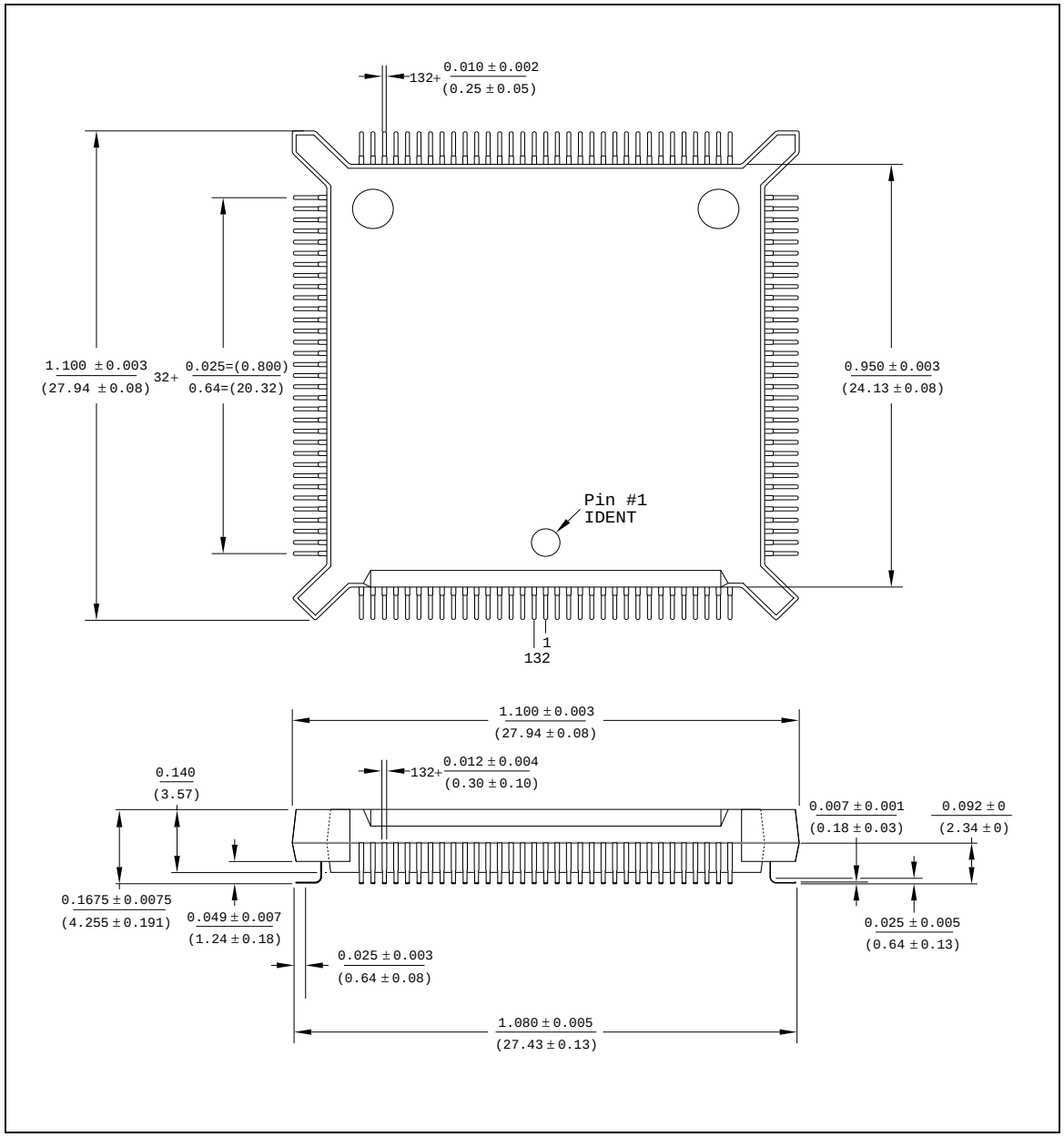


Figure 2: 132-pin PQFP mechanical details



3.0 DC Specifications

Table 5: Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Supply voltage	-0.3 to +7	V
V_{IN}	DC input voltage	-0.3 to V_{CC}+0.3	V
I_{IN}	DC input current	± 50	mA
T_{STG}	Storage temperature	-65 to +150	°C

Table 6: Guaranteed Operating Conditions

Symbol	Parameter	Rating	Units
V_{CC}, V_{CC3}	Supply voltage	4.75 to 5.25	V
V_{CC3}	Supply voltage for 3.3 Volt DRAM interface[1]. Vcc is still as above	3.0 to 3.6	V
T_A	Ambient temperature range	0 to 70	°C

1. For 3.3 Volt DRAM intreface operation.(See also note 8 table 11)

Table 7: DC Operating Specifications Vcc=5Volt and Vcc3=5 Volt

Symbol	Description	Conditions	Min	Max	Units
V_{IL}	Low level input voltage	Vcc = 4.75V		0.8	V
V_{IH}	High level input voltage	Vcc = 5.25V	2.0		V
I_{IL}	Low level input current	V_{IN} = GND, V_{CC} = 5.25V	-10		µA
I_{IH}	High level input current	V_{IN} = V_{CC} = 5.25V		10	µA
V_{OL}	Low level output voltage	V_{IN} = V_{IL} or V_{IH} I_{OL} = -12 mA		0.4	V
V_{OH}	High level output voltage	V_{IN} = V_{IL} or V_{IH} I_{OL} = -12 mA	V_{CC} -1.0		V
I_{OZL}	Low level float input leakage	V_{IN} = V_{IL} or V_{IH} V_O = GND	-20		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{IL} or V_{IH} V_O = 5.25V		20	µA
I_{CC} (max)	Maximum supply current	Continuous simple access Continuous burst access		100 30	mA
C_{IO}	Input and output capacitance			20	pF

Table 8: DC Operating Specifications Vcc3=3.3 Volt and Vcc=5 Volt

Symbol	Description	Conditions	Min	Max	Units
V_{OL}	Low level output voltage	V_{IN} = Vcc3 I_{OL} = 12 mA		0.4	V
V_{OH}	High level output voltage	V_{IN} = Vcc3 I_{OL} = -12 mA	2.4		V
I_{OZL}	Low level float input leakage	V_{IN} = Vcc2 V_O = GND	-10		µA
I_{OZH}	High level float input leakage	V_{IN} = V_{IL} or V_{IH} V_O =4.46V		10	µA
I_{CC} (max)	Maximum supply current	Continuous simple access Continuous burst access		140 40	mA

4.0 AC Specifications

Table 9: AC Test Conditions

Symbol	Parameter	Limits	Units
Vcc3/Vcc	Supply voltage	4.75 to 5.25	V
V_{CC3}	Supply voltage when 3.3 Volt DRAM interface operation[1] (Vcc is still as above)	3.0 to 3.6	V
V_{IN}	Input low and high voltages	0.4 and 4.25	V
C_{OUT}	Capacitive load on output and I/O pins	50	pF

1. For 3.3 Volt DRAM intreface operation.(See also note 8 table 11)

Table 10: Capacitive Derating for Output and I/O Pins

Output Drive Limit	Supply voltage	Derating
12 mA	Vcc=5 Volt, Vcc3=3.3 Volt	0.06 ns/pF for loads > 50 pF
12 mA	Vcc=5 Volt, Vcc3=5 Volt	0.04 ns/pF for loads > 50 pF

Table 11: Timing Parameters for V96BMC Vcc=5 Volts +/- 5% and Vcc3= 5 or 3.3 [8]Volts +/- 5%

			33 MHz		40 MHz		
Symbol	**Description**	**Note**	**Min**	**Max**	**Min**	**Max**	**Units**
t_C	PCLK period		30		25		ns
t_{CH}	PCLK high time		12		11		ns
t_{CL}	PCLK low time		12		11		ns
t_{SU}	Synchronous input setup		9		8		ns
t_H	Synchronous input hold			1		0.5	ns
t_H	Synchronous input hold (RESET#)			3		3	ns
t_{RZH}	$\overline{\text{READY}}$ 3-state to valid delay	1	3	13	3	10	ns
t_{RHL}	$\overline{\text{READY}}$ synchronous assertion delay		3	13	3	11	ns
t_{RLH}	$\overline{\text{READY}}$ synchronous de-assertion delay		3	13	3	11	ns
t_{RHZ}	$\overline{\text{READY}}$ valid to 3-state delay	1	3	10	3	7	ns
t_{BHL}	$\overline{\text{BTERM}}$ synchronous assertion delay		3	14	3	12	ns
t_{BLH}	$\overline{\text{BTERM}}$ synchronous de-assertion delay		3	13	3	11	ns
t_{EHL}	$\overline{\text{BERR}}$ synchronous assertion delay		3	13	3	11	ns
t_{ELH}	$\overline{\text{BERR}}$ synchronous de-assertion delay		3	12	3	10	ns
t_{IHL}	$\overline{\text{INT}}$ synchronous assertion delay		3	13	3	11	ns
t_{ILH}	$\overline{\text{INT}}$ synchronous de-assertion delay		3	12	3	10	ns
t_{ARA1}	Address Input to Row Address output delay (Interleaved)		3	14	3	12	ns
t_{ARA2}	Address Input to Row Address output delay (Non-interleaved)		4	18	4	15	ns
t_{RAH}	Row address hold from $\overline{\text{RAS}}$ assertion	2	t_M	t_M+2	t_M	t_M+2	ns
t_{CAV}	Column address valid from $\overline{\text{RAS}}$ assertion	2	t_M+1	t_M+4	t_M+1	t_M+4	ns
t_{CAH}	Column address hold from $\overline{\text{CAS}}$ assertion		t_C		t_C		ns
t_{BCAV}	Column address valid delay from previous $\overline{\text{CAS}}$ assertion (Burst)			t_C+3		t_C+3	ns
t_{RHL}	PCLK to $\overline{\text{RAS}}$ asserted delay		3	13	3	11	ns
t_{RLH}	PCLK to $\overline{\text{RAS}}$ de-asserted delay		3	13	3	11	ns
t_{RAS}	$\overline{\text{RAS}}$ pulse width	3	$3t_C$-1		$3t_C$-1		ns
t_{RSH}	$\overline{\text{RAS}}$ hold from last $\overline{\text{CAS}}$ assertion	4	t_N		t_N		ns
t_{RP}	$\overline{\text{RAS}}$ precharge time	5	t_P-2		t_P-2		ns
t_{CHL}	PCLK to $\overline{\text{CAS}}$ asserted delay	1	3	13	3	12	ns
t_{CLH}	PCLK to $\overline{\text{CAS}}$ de-asserted delay		4	12	3	11	ns
t_{CAS}	$\overline{\text{CAS}}$ pulse width	4	t_N-1		t_N-1		ns
t_{CPN}	$\overline{\text{CAS}}$ precharge time		$0.5t_C$		$0.5t_C$		ns
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time		$1.5t_C$-2	$1.5t_C$	$1.5t_C$-2	$1.5t_C$	ns
t_{WESU}	Write Enable setup to $\overline{\text{RAS}}$ assertion		10		9		ns

Table 11: Timing Parameters for V96BMC Vcc=5 Volts +/- 5% and Vcc3= 5 or 3.3 [8]Volts +/- 5%

t_{WEH}	Write Enable hold from $\overline{RAS}$ de-assertion		1	3	1	3	ns
t_{LED}	PCLK to Latch Enable output delay	6	3	12	3	10	ns
t_{TXHL1}	PCLK to Buffer Control fall delay	7	3	13	3	11	ns
t_{TXHL2}	PCLK to Buffer Control fall delay (Mode 2 and 3 at TXA pin only)		4	15	4	13	ns
t_{TXLH}	PCLK to Buffer Control rise delay		3	12	3	10	ns
t_{RFHL}	$\overline{REFRESH}$ synchronous assertion delay		3	13	3	11	ns
t_{RFLH}	$\overline{REFRESH}$ synchronous de-assertion delay		3	13	3	11	ns
t_{ASU}	Address setup to ALE Falling		6		5		ns
t_{AH}	Address hold from ALE Falling		5		4		ns

NOTES:
1. Specified from PCLK falling edge.
2. $t_M = t_C$ when T_MUX = 1; $t_M = 0.5 \bullet t_C$ when T_MUX = 0.
3. Maximum $\overline{RAS}$ pulse width depends on the number of burst access.
4. $t_N = 1.5 \bullet t_C$ when T_RAS = 0; $t_N = 2.5 \bullet t_C$ when T_RAS = 1.
5. $t_P = 2 \bullet t_C$ when T_RAS = 0; $t_P = 2 \bullet t_C$ when T_RAS = 1 and T_RP = 1;
$t_P = 3 \bullet t_C$ when T_RAS = 1 and T_RP = 0.
6. Rising delay is measured from PCLK falling edge, falling delay is measured from PCLK rising edge.
7. Except for Mode 2 and 3 at TXA pin.
8. In order to have 3.3 Volt DRAM interface Vcc3 pins must be connected to 3.3 Volt.
Vcc3 pins are: PIN # 91, 97, 103, 109, 57, 63, 69, 75, 81.
The power supply pins that must always be connected to 5V are Vcc.
Vcc pins are: PIN # 4, 47, 115.

Figure 3: Clock and Synchronous Signals

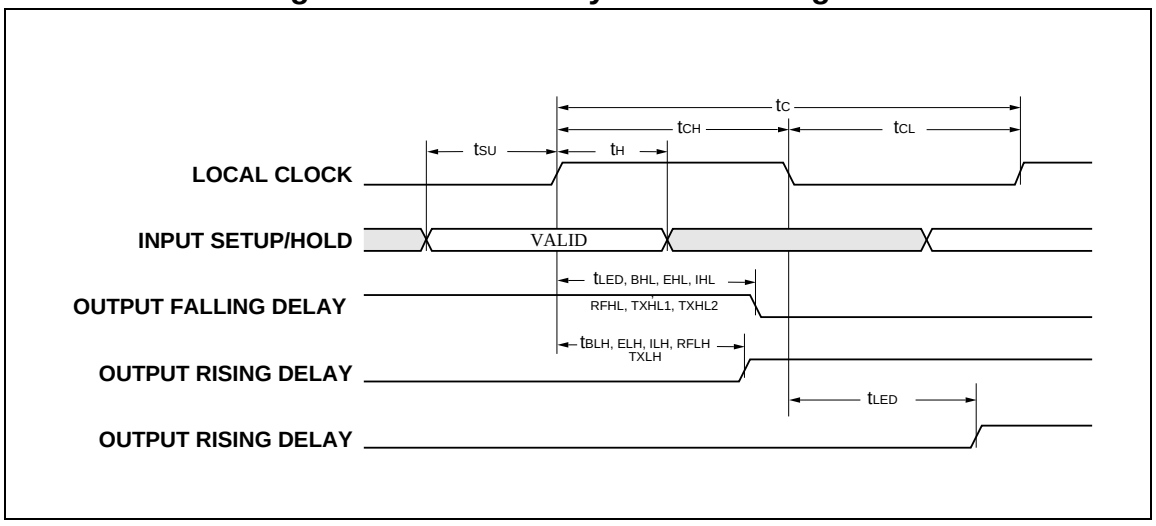


Figure 4: ALE Timing

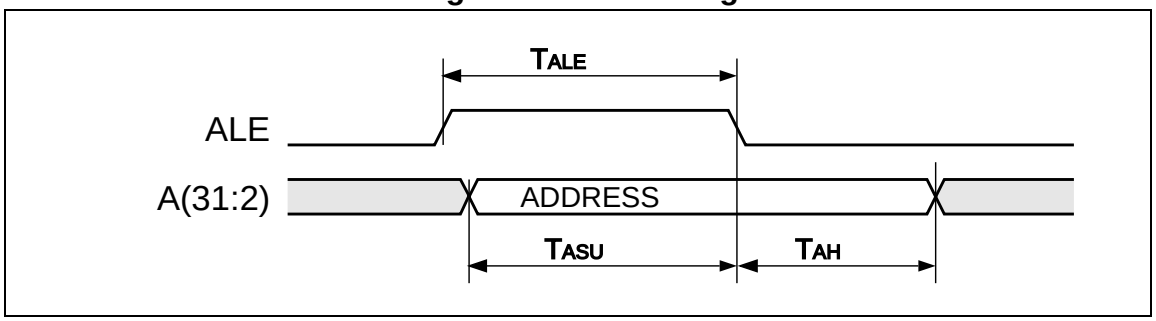


Figure 5: Basic Access Timing

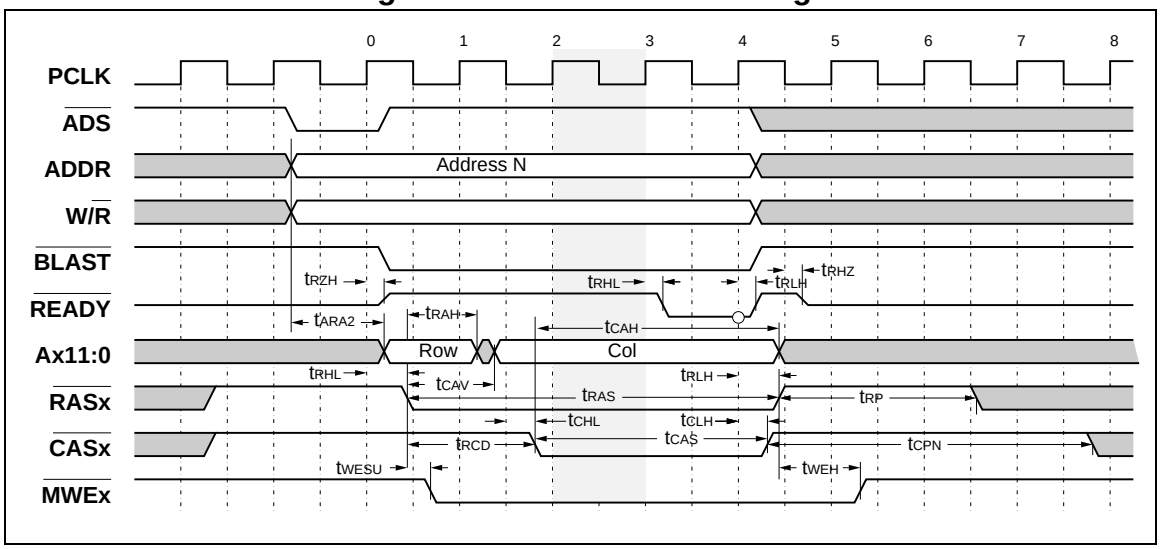
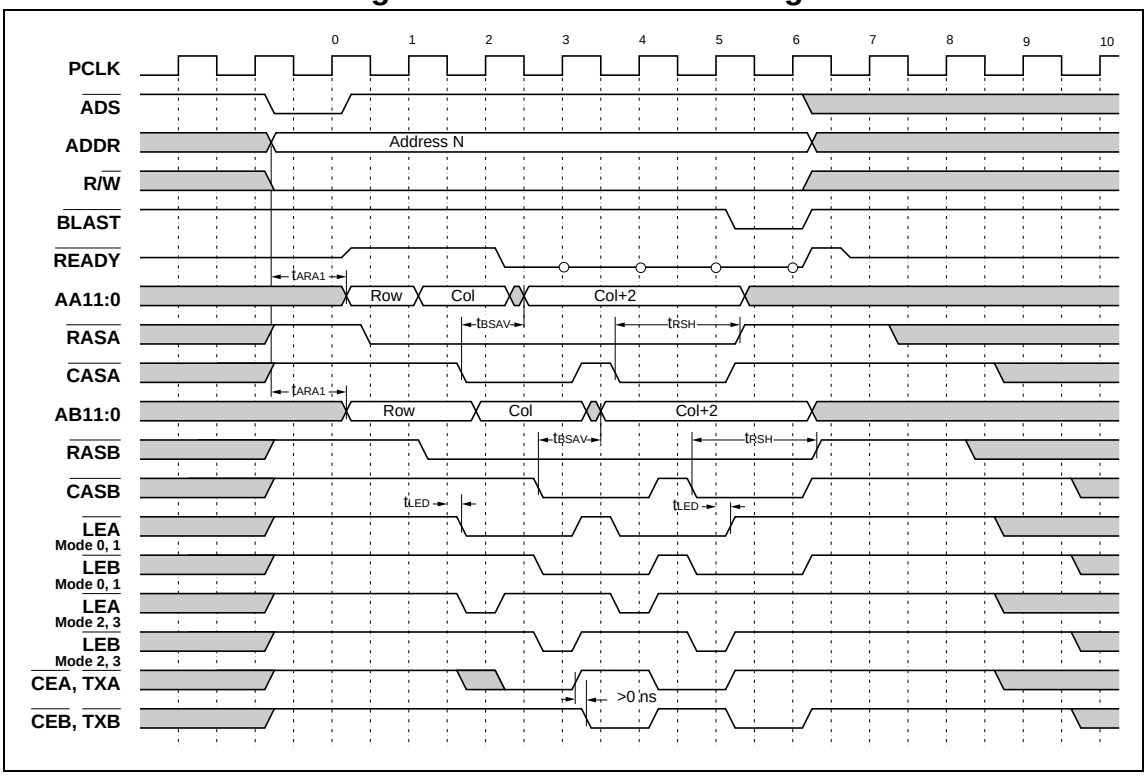


Figure 6: Burst Access Timing



5.0 Revision History

Table 12: Revision History

Revision Number	Date	Comments and Changes
3.2	7/98	V96BMC Rev D timing parameters with 3.3V DRAM support.
3.1	10/96	Data Book revision.
3.0	05/96	Updated timings to final D-step values. Simplified data sheet format.
2.0	7/92	Updated timings to final A-step values.
1.0	7/92	First pre-silicon revision of preliminary data sheet. DC and AC specs TBD. Sent only to a limited number of customers

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