Product Brief
January 30, 2002

UHC124

High Performance Four-Port Embedded USB Host Controller

Description

TransDimension's UHC124 is a four-port, single chip USB Host controller that is the first of a family of integrated low-cost, high-performance controllers optimized and specifically designed for embedded systems, mobile communication, and consumer products. It is a non-PCI controller that supports USB Specification Rev. 2.0 compliant full-speed (12Mb/s) and low-speed (1.5Mb/s) USB devices. It is the only non-PCI controller that has been proven to run at USB full speed, even running under a full USB stack. The UHC124 controller enables an embedded system to function as a USB Host, dramatically expanding the degree of interconnectivity and extending the applicability of USB into many new areas. In addition to silicon, development kits, USB Host Stack, device drivers for most products, and interface code to the UHC124 for numerous RTOS' are available via our wholly owned subsidiary, SoftConnex Technologies, Inc.

The UHC124 has unique, patent-pending features that are indispensable for achieving high data throughput and low interrupt rates. It is the only one on the market that is designed from the ground up for embedded applications with features like batch processing, multiple interrupt modes, separate data and descriptor memory, and double buffering. It is optimized for cost, performance and ease of development. The software/hardware co-designed architecture enables high performance while maintaining simplicity and flexibility that are critical for embedded applications. It can be interfaced to CISC or RISC microprocessors, microcontrollers, or digital signal processors (DSPs) and is ideal for providing USB host functions to a wide range of applications including mobile devices, cell phones, PDAs, point-of-sale systems, test equipment, set-top boxes, Internet appliances, as well as serving as an interface for USB to Bluetooth controllers.

The complete solutions offer the advantages of shortened time-to-market, simplified procurement and technical support from one source.

Features

- High performance USB host controller for embedded applications
- Supports USB Specification 2.0 compliant full-speed (12Mb/s) and low-speed (1.5Mb/s) USB devices
- Patent pending design
- Full USB bandwidth utilization with low load on system microprocessor
- Standard 8-bit microprocessor bus interface
- 2 Kbyte data memory
- Supports all four types of USB transfers (control, bulk, interrupt, and isochronous with maximum packet size of 1,023 bytes)
- Supports batch processing of up to 16 USB transactions without interrupting the MCU
- Supports scheduling of transaction batches that may "spill" over the USB frame boundaries for easy programming
- Supports "in-place" processing in the data memory – used for applications requiring peer-to-peer data transfer between USB devices
- Supports double buffering for all USB transfers
- Hardware generated Start of Frame (SOF)
- Fully qualified, market proven root hub with four ports and integrated analog transceivers.
- Individually controlled power-on and over-current circuit for each of the four downstream ports
- Power management with host suspend, remote wakeup, and power saving modes
- 6 MHz crystal/oscillator to reduce cost and EMI
- Evaulation/development kit available including C source code of the programming interface library and an interactive USB host controller Exerciser
- Embedded RTOS software available for popular microprocessors, RISC, CISC, and DSP's using WinCE, Linux, VxWorks, Nucleus, Lynx, QNX, pSOS, PowerTV, SMX, ThreadX, VRTX, ITRON, Symbian and MS-DOS operating systems with more in development
- Supports OHCI/UHCI compliant USB host stack
- USB device driver software available including printers, speakers, mass storage, hub, modems, Ethernet, mouse, keyboard, digital camera, video camera, cell phone, STB and PDA with more in development
- Industrial grade devices standard. Military and automotive grade devices available
- Single 3.3V power supply
- 64 pin LQFP package

Architecture

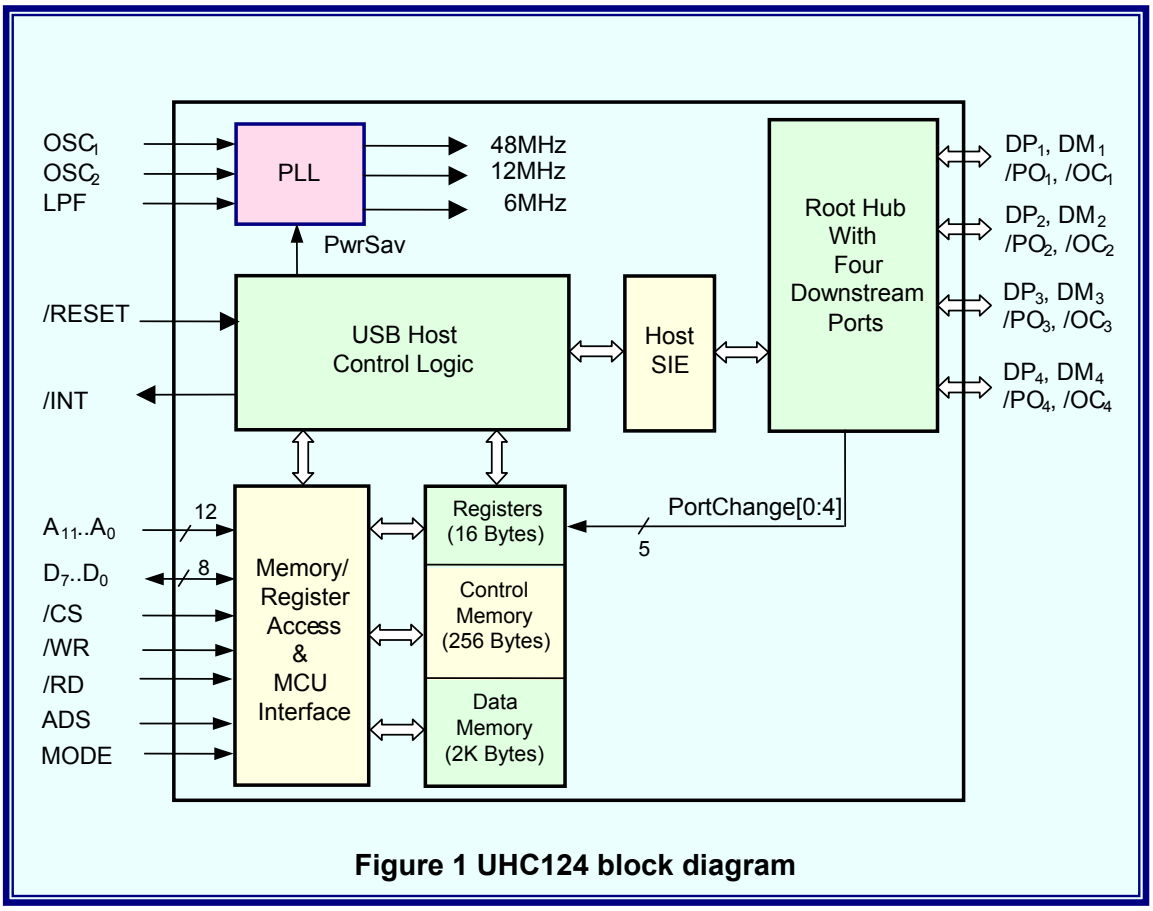

Figure 1 UHC124 block diagram

Development

Interface with MCUs: The UHC124 may be interfaced with a microprocessor using either one of two methods:

- For MCUs with standard external data bus, the UHC124 can be interfaced directly via 8 bits of its data bus and 12 bits of its address bus. When the UHC124 operates under this mode, its internal memory blocks, as well as its control/status registers, are mapped into the processor's address space.
- For MCUs without an external data bus, the UHC124 may be interfaced using an 8-bit output port and an 8-bit bi-directional port. Under this mode, a built-in, auto incrementing address register allows accessing to a large block of the UHC124 memory with a single (address) write cycle, followed by as many read/write cycles as the number of data bytes to be transferred from/to the UHC124.

Control Memory (CM): The UHC124 controller memory holds up to 16 Transaction Descriptors (XDs) used to specify up to 16 USB transactions.

Data Memory (DM): The 2,048 bytes of data memory (DM) built into the UHC124 serve as data buffers shared between the MCU and USB system.

Batch Processing: The user software may organize up to 16 USB transactions into a *transaction batch*, or simply a *batch*. A batch may contain transactions for full-speed (FS: 12 Mbit/sec) and low-speed (LS: 1.5 Mbit/sec) USB devices, of four types of endpoints (control, bulk, interrupt and isochronous) and all transaction types (SETUP, IN and OUT). Compared with other USB host controller designs, batch processing is a very important and unique feature of the UHC124. Our software/hardware co-design overcomes the serious shortcomings of other embedded USB host controller designs that require an interrupt upon completion of *every* USB transaction. These defficient designs:

- result in significant loss of USB bus bandwidth as the invocation (interrupt latency time) and execution of the interrupt service routine (ISR), (or of certain portion of the ISR at the minimum,) cannot overlap with USB bus

activity. This problem is more obvious and damaging when data packet sizes are small and spontaneous, which is typical for many embedded USB host applications, making double buffering impractical.

- waste MCU's time due to processor/RTOS overhead with frequent ISR invocation and execution.

With its batch processing capability, a single register write to the UHC124 can dispatch altogether up to 16 transactions, and a single interrupt is generated only after the completion of all of them. The system throughput is therefore significantly improved maximizing the bandwidth on the USB. At the same time, the number of interrupts to the MCU is greatly reduced, saving processor resources for non-USB activities.

Double Buffering: Double buffering, and its more general form circular buffering, are effective ways to improve the USB system throughput. The UHC124 supports dual port memory access to its entire addressing space (control registers, CM and DM). Together with its batch processing capability, double buffering becomes attractive even for transactions with small data packets.

Root Hub: The UHC124 employs a fully qualified, market proven 4-port USB hub. Analog USB transceivers are built-in for all four downstream ports. Power-on and over-current circuits are presented individually for each port.

External Crystal/Oscillator: A PLL (Phase Locked Loop) is integrated on-chip to generate, from a single 6 MHz crystal or crystal oscillator, the 48 MHz, 12 MHz and 6 MHz clock signals required by the UHC124 internal circuitry minimizing EMI.

UHCI and OHCI: The UHC124 is fully compliant with USB Specification 2.0 (for full speed and low speed operation). However, it is not a Universal Host Controller Interface/Open Host Controller Interface (UHCI/OHCI) based device because it is not intended for the PCI bus. OEMs may develop or license, a Host Controller Driver (HCD) providing a software interface that appears to the rest of the USB host stack as if there were a UHCI or an OHCI compliant host controller.

System Suspend and Resume: Under the control of user software, the UHC124 may bring the USB system into suspend state, as dictated by USB specification. While the oscillator for the UHC124 is still running, all USB bus activities, including SOF generation, are stopped. The system may be brought out of the suspend state by user software, or by a remote wakeup originating from a downstream USB device.

Power Saving Mode: Under the control of user software, the UHC124 may enter the *power saving* mode, in which all internal clocks are stopped, and the PLL is disabled. A small quiescent current (about 200 uA) is consumed by the UHC124. The UHC124 is reactivated by a hardware reset.

Software Support: TransDimension is a leader in the embedded market space, bringing both software and silicon to its customers. USB Host Stack, device drivers for most products, and interface code to the UHC124 for numerous RTOS' are available via our wholly owned subsidiary, SoftConnex Technologies, Inc. The products are geared towards mobile and post-PC products, including mobile phone, palmtop PC, PDA, set top box, home gateway, and Internet appliances.

TransDimension provides development and support packages and a wide spectrum of USB host software support in C source code to reduce development cost and time to market for its customers. USB Stack software for various real-time operating systems and device drivers for most mobile and post-PC products, as well as required interface code between the USB stack and the silicon are available by contacting your local TransDimension representative. OEMs may license from TransDimension, as part of the *UHC124 Development Kit*, an OS-independent *UHC124 Programming Interface Library*, supporting direct UHC124 operation and efficient USB host control independent of any RTOS. The *UHC124 USB Host Controller Exerciser* allows an OEM to quickly evaluate, and to develop applications for the UHC124 to operate on USB devices.

Pin Description

The UHC124 is delivered in a 64-pin LQFP package:

Pin#	Pin Name	Pin Type	Pin Description
1	**V_{DD}**	Power	3.3V Power Supply. All four VDD pins must be connected.
2	**A_0**	In	Address bus: bit 0 (least significant bit).
3	**A_1**	In	Address bus: bit 1.
4	**A_2**	In	Address bus: bit 2.
5	**A_3**	In	Address bus: bit 3.
6	**A_4**	In	Address bus: bit 4.
7	**A_5**	In	Address bus: bit 5.
8	**A_6**	In	Address bus: bit 6.
9	**A_7**	In	Address bus: bit 7.
10	**A_8**	In	Address bus: bit 8.
11	**A_9**	In	Address bus: bit 9.
12	**A_{10}**	In	Address bus: bit 10.
13	**A_{11}**	In	Address bus: bit 11.
14	**MODE**	In	Memory Access Mode. MODE = 1: Non-multiplexed memory access. MODE = 0: Multiplexed memory access with auto-incremented address.
15	**/CS**	In	Chip Select: active low.
16	**V_{SS}**	Ground	Ground. All four pins must be connected.
17	**OSC_1**	In	Oscillator Input: input to the inverting oscillator amplifier.
18	**OSC_2**	Out	Oscillator Output: output of the inverting oscillator amplifier.
19	**LPF**	Passive	PLL Filter: connecting to a passive RC network.
20	**V_{DD}**	Power	3.3V Power Supply. All four pins must be connected.
21	**$TEST_0$**	Bidir	Test Signal I/O: used only for factory testing; working in output mode during normal operation.
22	**$TEST_1$**	Bidir	Test Signal I/O: used only for factory testing; working in output mode during normal operation.
23	**$TEST_2$**	Bidir	Test Signal I/O: used only for factory testing; working in output mode during normal operation.
24	**$TEST_3$**	Bidir	Test Signal I/O: used only for factory testing; working in output mode during normal operation.
25	**/OC_1**	In	Over Current condition input for Port 1; active low.
26	**/OC_2**	In	Over Current condition input for Port 2; active low.
27	**/OC_3**	In	Over Current condition input for Port 3; active low.
28	**/OC_4**	In	Over Current condition input for Port 4; active low.
29	**/PO_1**	Out	Power On Switch for Port 1; active low.
30	**/PO_2**	Out	Power On Switch for Port 2; avtive low.
31	**/PO_3**	Out	Power On Switch for Port 3; activel low.
32	**/PO_4**	Out	Power On Switch for Port 4; activel low.
33	**V_{DD}**	Power	3.3V Power Supply. All four pins must be connected.
34	**DP_1**	Bidir	Port 1 Differential Data (+) for USB I/O.
35	**DM_1**	Bidir	Port 1 Differential Data (-) for USB I/O.

36	**V_{SS}**	Ground	Ground. All four pins must be connected.
37	**DP_2**	Bidir	Port 2 Differential Data (+) for USB I/O.
38	**DM_2**	Bidir	Port 2 Differential Data (-) for USB I/O.
39	**DP_3**	Bidir	Port 3 Differential Data (+) for USB I/O.
40	**DM_3**	Bidir	Port 3 Differential Data (-) for USB I/O.
41	**DP_4**	Bidir	Port 4 Differential Data (+) for USB I/O.
42	**DM_4**	Bidir	Port 4 Differential Data (-) for USB I/O.
43	**$TEST_4$**	Bidir	Test Signal I/O: used only for factory testing; working in output mode during normal operation.
44	**D_0**	Bidir	Data bus: Bit 0.
45	**D_1**	Bidir	Data bus: Bit 1.
46	**D_2**	Bidir	Data bus: Bit 2.
47	**D_3**	Bidir	Data bus: Bit 3.
48	**V_{DD}**	Power	3.3V Power Supply. All four pins must be connected.
49	**V_{SS}**	Ground	Ground. All four pins must be connected.
50	**D_4**	Bidir	Data bus: Bit 4.
51	**D_5**	Bidir	Data bus: Bit 5.
52	**D_6**	Bidir	Data bus: Bit 6.
53	**D_7**	Bidir	Data bus: Bit 7.
54	**/RESET**	In	Hardware Reset: resets entire USB system; active low.
55	**/WR**	In	Bus Write Strobe: active low.
56	**/RD**	In	Bus Read Strobe: active low.
57	**TMS_0**	In	Test Mode Select: used only for factory testing; connect to VSS for normal operation.
58	**TMS_1**	In	Test Mode Select: used only for factory testing; connect to VSS for normal operation.
59	**TMS_2**	In	Test Mode Select: used only for factory testing; connect to VSS for normal operation.
60	**TMS_3**	In	Test Mode Select: used only for factory testing; connect to VSS for normal operation.
61	**/INT**	Ouput	Interrupt: generated for microprocessor; active low.
62	**ADS**	In	Address/Data Select: see description of Pin MODE; When MODE = 1, this pin has no effect, and it should be tied to VSS for noise immunity.
63	**GNDP**	In	Voltage Reference: for built-in power on reset (POR), connect to VSS (ground) for normal operation.
64	**V_{SS}**	Ground	Ground. All four pins must be connected.

Package (64 pin LQFP)

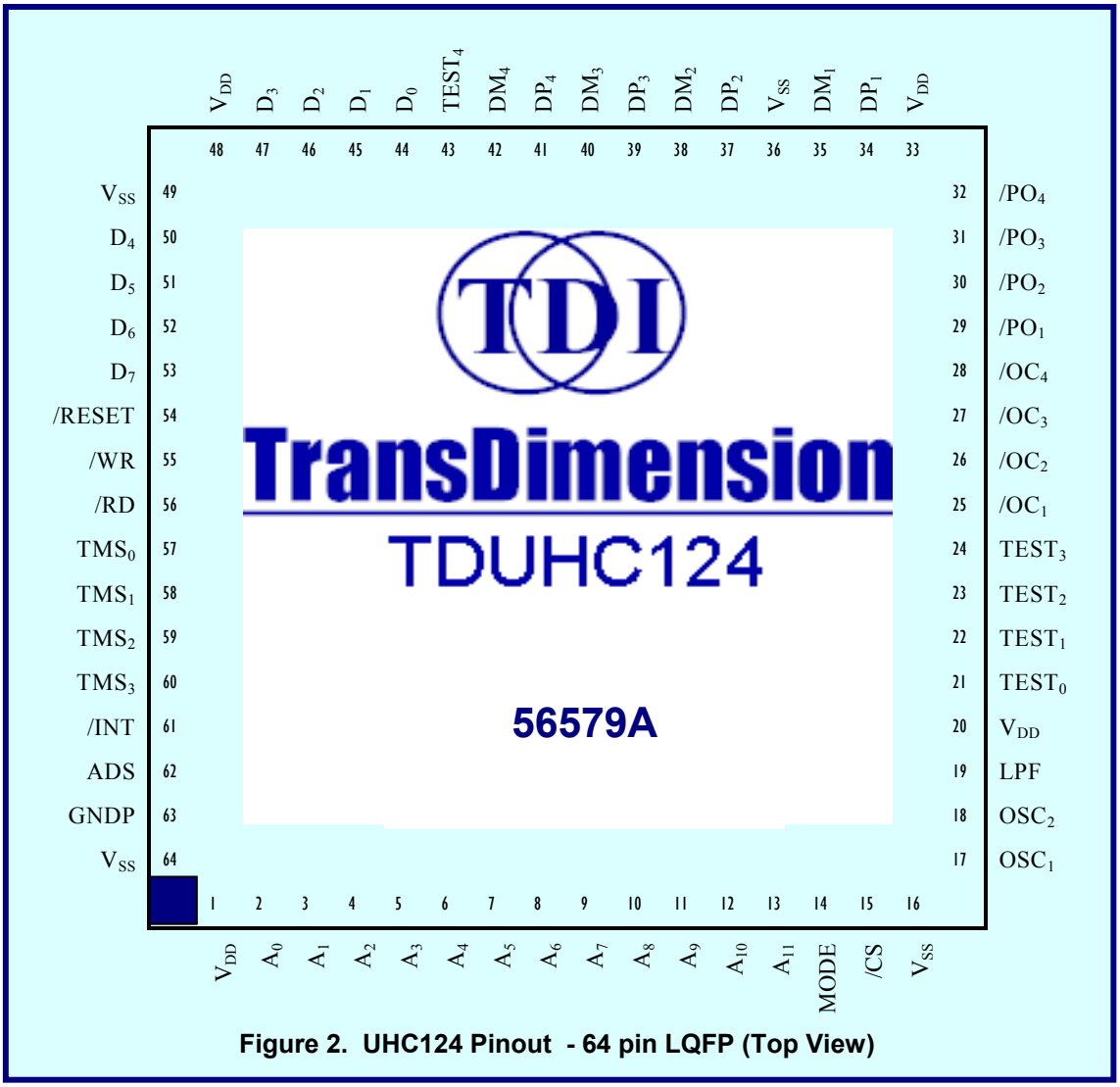

Figure 2. UHC124 Pinout - 64 pin LQFP (Top View)

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