THC63LVD824

Single(135MHz)/Dual(170MHz) Link LVDS Receiver for XGA/SXGA/SXGA+/UXGA

General Description

The THC63LVD824 receiver is designed to support Single Link transmission between Host and Flat Panel Display up to SXGA+ resolutions and Dual Link transmission between Host and Flat Panel Display up to UXGA resolutions. The THC63LVD824 converts the LVDS data streams back into 48bits of CMOS/TTL data with falling edge or rising edge clock for convenient with a variety of LCD panel controllers.

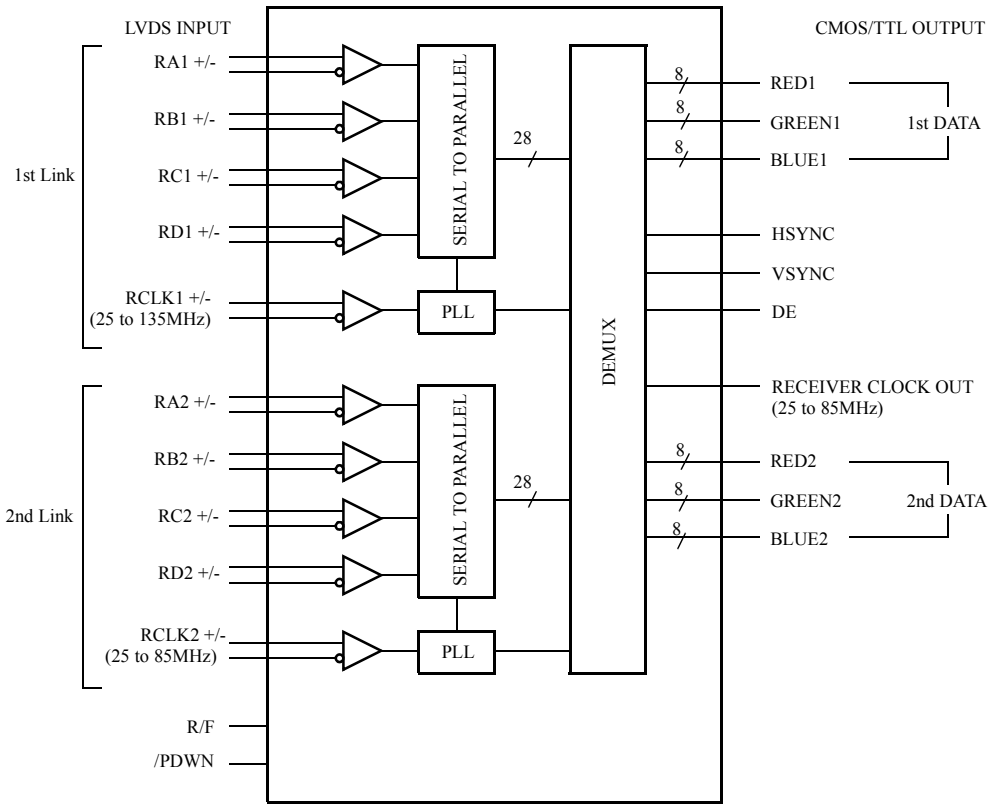
In Single Link, data transmit clock frequency of 135MHz, 48bits of RGB data are transmitted at an effective rate of 945Mbps per LVDS channel. Using a 135MHz clock, the data throughput is 472Mbytes per second.

In Dual Link, data transmit clock frequency of 85MHz, 48bits of RGB data are transmitted at an effective rate of 595Mbps per LVDS channel. Using a 85MHz clock, the data throughput is 595Mbytes per second.

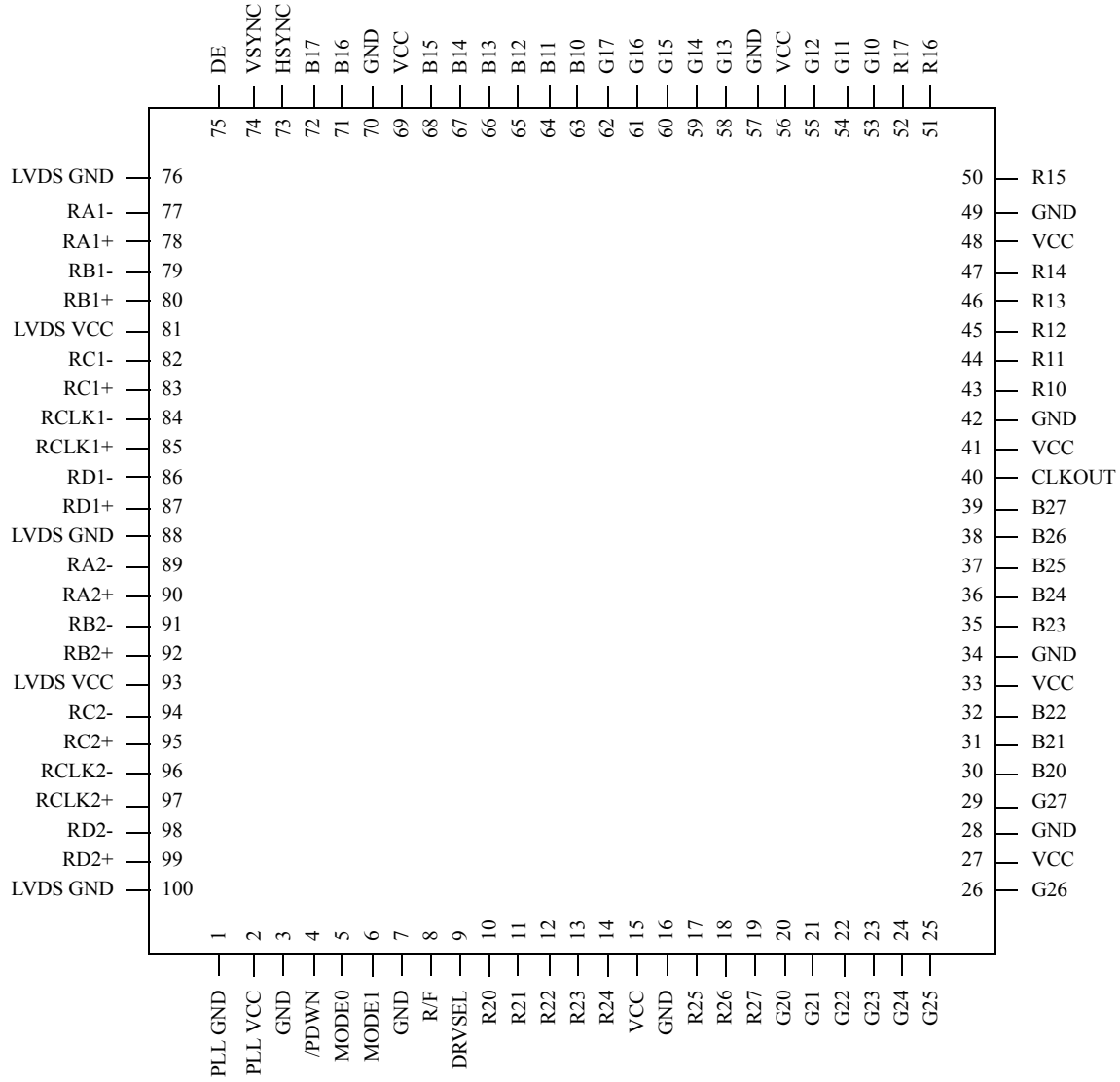
Features

- Wide dot clock range: 25-170MHz suited for VGA, SVGA, XGA, SXGA, SXGA+ and UXGA
- PLL requires No external components
- Supports Single Link up to 135MHz dot clock for SXGA+
- Supports Dual Link up to 170MHz dot clock for UXGA
- 50% output clock duty cycle
- TTL clock edge programmable
- TTL output driverbility selectable for lower EMI
- Power down mode
- Low power single 3.3V CMOS design
- 100pin TQFP
- THC63LVDF84B compatible

Block Diagram



Pin Out



Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>RA1+, RA1-</td><td>78, 77</td><td>LVDS IN</td><td rowspan="4">The 1st Link. The 1st pixel input data when Dual Link.</td></tr>
<tr><td>RB1+, RB1-</td><td>80, 79</td><td>LVDS IN</td></tr>
<tr><td>RC1+, RC1-</td><td>83, 82</td><td>LVDS IN</td></tr>
<tr><td>RD1+, RD1-</td><td>87, 86</td><td>LVDS IN</td></tr>
<tr><td>RCLK1+, RCLK1-</td><td>85, 84</td><td>LVDS IN</td><td>LVDS Clock Input for 1st Link.</td></tr>
<tr><td>RA2+, RA2-</td><td>90, 89</td><td>LVDS IN</td><td rowspan="4">The 2nd Link. These pins are disabled when Single Link.</td></tr>
<tr><td>RB2+, RB2-</td><td>92, 91</td><td>LVDS IN</td></tr>
<tr><td>RC2+, RC2-</td><td>95, 94</td><td>LVDS IN</td></tr>
<tr><td>RD2+, RD2-</td><td>99, 98</td><td>LVDS IN</td></tr>
<tr><td>RCLK2+, RCLK2-</td><td>97, 96</td><td>LVDS IN</td><td>LVDS Clock Input for 2nd Link.</td></tr>
<tr><td>R17 ~ R10</td><td>52, 51, 50, 47, 46, 45, 44, 43</td><td>OUT</td><td rowspan="3">The 1st Pixel Data Outputs.</td></tr>
<tr><td>G17 ~ G10</td><td>62, 61, 60, 59, 58, 55, 54, 53</td><td>OUT</td></tr>
<tr><td>B17 ~ B10</td><td>72, 71, 68, 67, 66, 65, 64, 63</td><td>OUT</td></tr>
<tr><td>R27 ~ R20</td><td>19, 18, 17, 14, 13, 12, 11, 10</td><td>OUT</td><td rowspan="3">The 2nd Pixel Data Outputs.</td></tr>
<tr><td>G27 ~ G20</td><td>29, 26, 25, 24, 23, 22, 21, 20</td><td>OUT</td></tr>
<tr><td>B27 ~ B20</td><td>39, 38, 37, 36, 35, 32, 31, 30</td><td>OUT</td></tr>
<tr><td>DE</td><td>75</td><td>OUT</td><td>Data Enable Output.</td></tr>
<tr><td>VSYNC</td><td>74</td><td>OUT</td><td>Vsync Output.</td></tr>
<tr><td>HSYNC</td><td>73</td><td>OUT</td><td>Hsync Output.</td></tr>
<tr><td>CLKOUT</td><td>40</td><td>OUT</td><td>Clock Output.</td></tr>
<tr><td>DRVSEL</td><td>9</td><td>IN</td><td>Output Driverbility Select.
H: High power, L: Low power.</td></tr>
<tr><td>R/F</td><td>8</td><td>IN</td><td>Output Clock Triggering Edge Select.
H: Rising edge, L: Falling edge.</td></tr>
<tr><td>MODE1, MODE0</td><td>6, 5</td><td>IN</td><td>Pixel Data Mode.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>Dual Link</td></tr>
<tr><td>L</td><td>H</td><td>Single Link</td></tr>
</table></td></tr>
<tr><td>/PDWN</td><td>4</td><td>IN</td><td>H: Normal operation,
L: Power down (all outputs are pulled to ground)</td></tr>
<tr><td>VCC</td><td>15, 27, 33, 41, 48, 56, 69</td><td>Power</td><td>Power Supply Pins for TTL outputs and digital circuitry.</td></tr>
<tr><td>GND</td><td>3, 7, 16, 28, 34, 42, 49, 57, 70</td><td>Ground</td><td>Ground Pins for TTL outputs and digital circuitry.</td></tr>
<tr><td>LVDS VCC</td><td>81,93</td><td>Power</td><td>Power Supply Pins for LVDS inputs.</td></tr>
<tr><td>LVDS GND</td><td>76, 88, 100</td><td>Ground</td><td>Ground Pins for LVDS inputs.</td></tr>
</table>

Pin Name	Pin #	Type	Description
PLL VCC	2	Power	Power Supply Pin for PLL circuitry.
PLL GND	1	Ground	Ground Pin for PLL circuitry.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
Output Current	-30mA ~ 30mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Lead Temperature (Soldering, 10sec)	+230°C
Maximum Power Dissipation @+25°C	1.0W

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH}= -2mA, -4mA (data) I_{OH}= -4mA, -8mA (clock)	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}= 2mA, 4mA (data) I_{OL}= 4mA, 8mA (clock)			0.4	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	µA

LVDS Receiver DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input High Threshold	V_{OC}= 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{OC}= 1.2V	-100			mV
I_{INL}	Input Current	V_{IN}= 2.4V / 0V V_{CC}= 3.6V			±20	µA

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

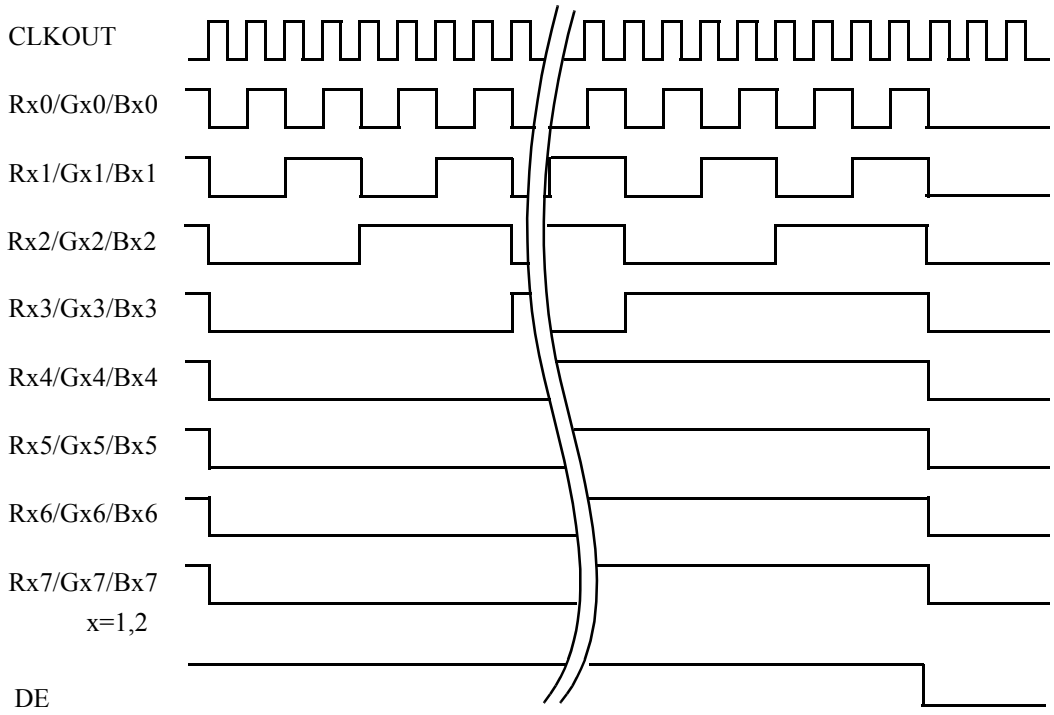
Supply Current

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

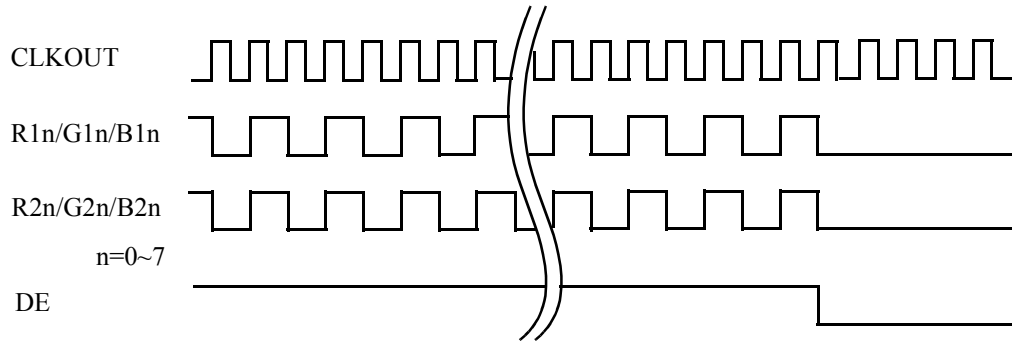
Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I_{RCCG}	Receiver Supply Current (256 Gray Scale Pattern)	VESA SXGA (60Hz), f_{CLKOUT} = 54MHz	MODE<1:0>=LH CL=8pF, Vcc=3.3V	57	66	mA
		VESA UXGA (60Hz), f_{CLKOUT} = 81MHz	MODE<1:0>=LL CL=8pF, Vcc=3.3V	85	97	mA
I_{RCCW}	Receiver Supply Current (Double Checker Pattern)	VESA SXGA (60Hz), f_{CLKOUT} = 54MHz	MODE<1:0>=LH CL=8pF, Vcc=3.3V	87	99	mA
		VESA UXGA (60Hz), f_{CLKOUT} = 81MHz	MODE<1:0>=LL CL=8pF, Vcc=3.3V	148	173	mA
I_{RCCS}	Receiver Power Down Supply Current	/PDWN = L			10	µA

(*) VESA is a trademark of the Video Electronics Standards Association.

256 Gray Scale Pattern



Double Checker Pattern



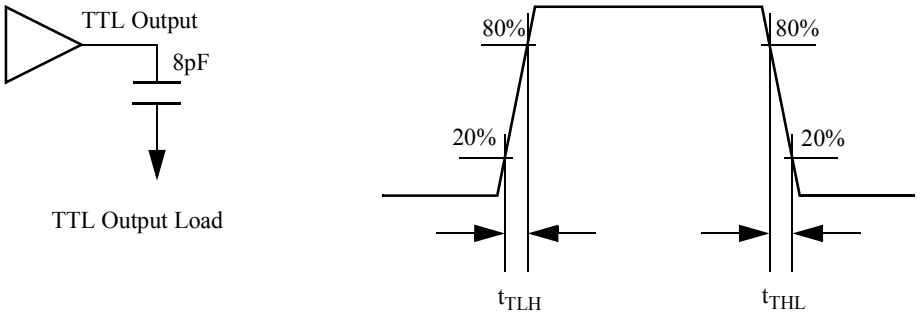
Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{RCP}	CLKOUT Period	Dual-in / Dual-out	11.76	t_{RCIP}	40.0	ns
		Single-in / Dual-out	14.8	$2t_{RCIP}$	80.0	ns
t_{RCH}	CLKOUT High Time			$\frac{t_{RCP}}{2}$		ns
t_{RCL}	CKLOUT Low Time			$\frac{t_{RCP}}{2}$		ns
t_{RS}	TTL Data Setup to CLKOUT		$0.3t_{RCP}$			ns
t_{RH}	TTL Data Hold from CKLOUT		$0.3t_{RCP}$			ns
t_{TLH}	TTL Low to High Transition Time			3.0	5.0	ns
t_{THL}	TTL High to Low Transition Time			3.0	5.0	ns
t_{RIP1}	Input Data Position0 (t_{RCIP} = 7.4ns)		-0.25	0.0	+0.25	ns
t_{RIP0}	Input Data Position1 (t_{RCIP} = 7.4ns)		$\frac{t_{RCIP}}{7} - 0.25$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP6}	Input Data Position2 (t_{RCIP} = 7.4ns)		$2\frac{t_{RCIP}}{7} - 0.25$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP5}	Input Data Position3 (t_{RCIP} = 7.4ns)		$3\frac{t_{RCIP}}{7} - 0.25$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP4}	Input Data Position4 (t_{RCIP} = 7.4ns)		$4\frac{t_{RCIP}}{7} - 0.25$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP3}	Input Data Position5 (t_{RCIP} = 7.4ns)		$5\frac{t_{RCIP}}{7} - 0.25$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RIP2}	Input Data Position6 (t_{RCIP} = 7.4ns)		$6\frac{t_{RCIP}}{7} - 0.25$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + 0.25$	ns
t_{RPLL}	Phase Lock Loop Set				10.0	ms
t_{RCIP}	CLKIN Period		7.4		40.0	ns
t_{CK12}	Skew Time between RCLK1 and RCLK2				$\pm 0.3t_{RCIP}$	ns

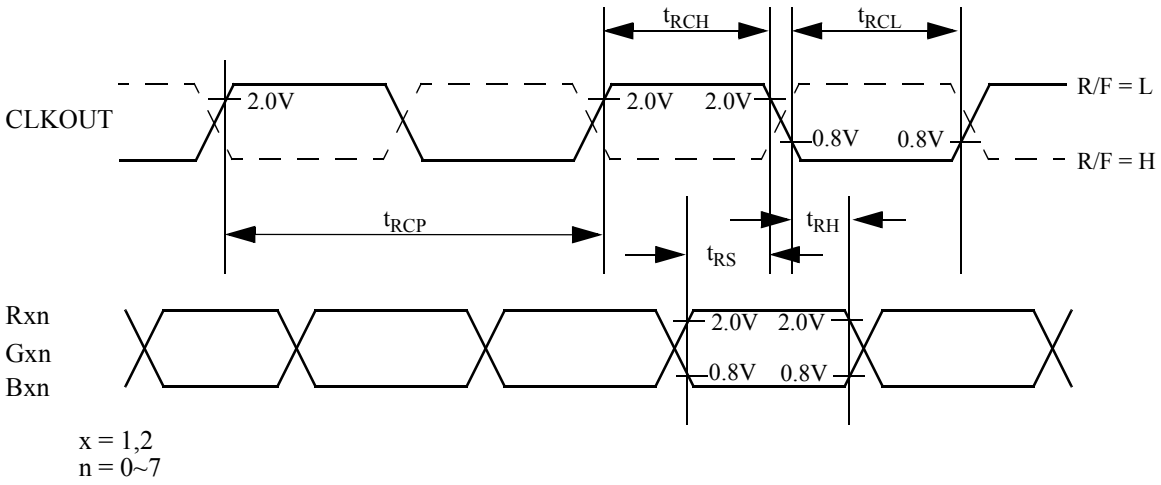
AC Timing Diagrams

TTL Outputs



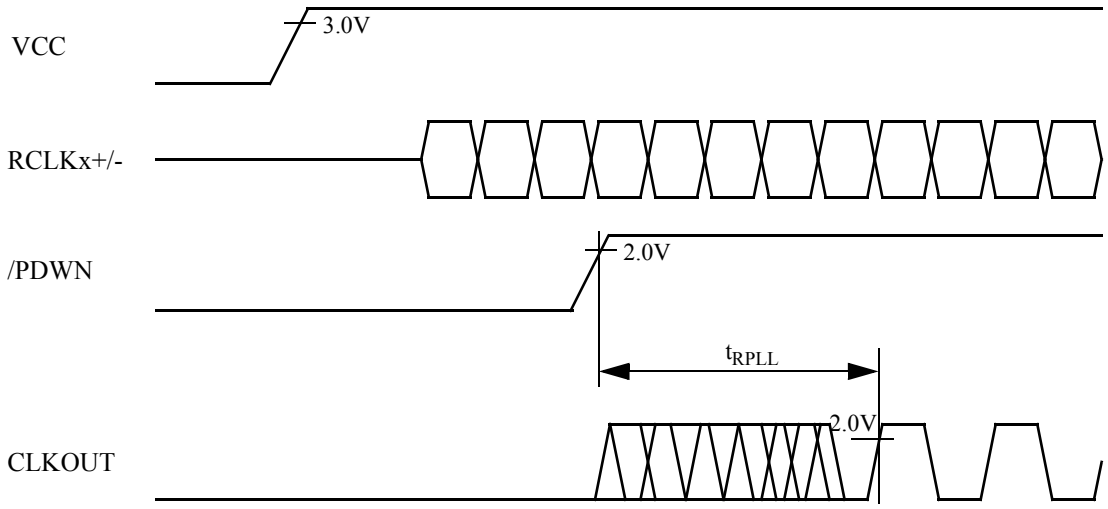
AC Timing Diagrams

TTL Outputs



x = 1,2
n = 0~7

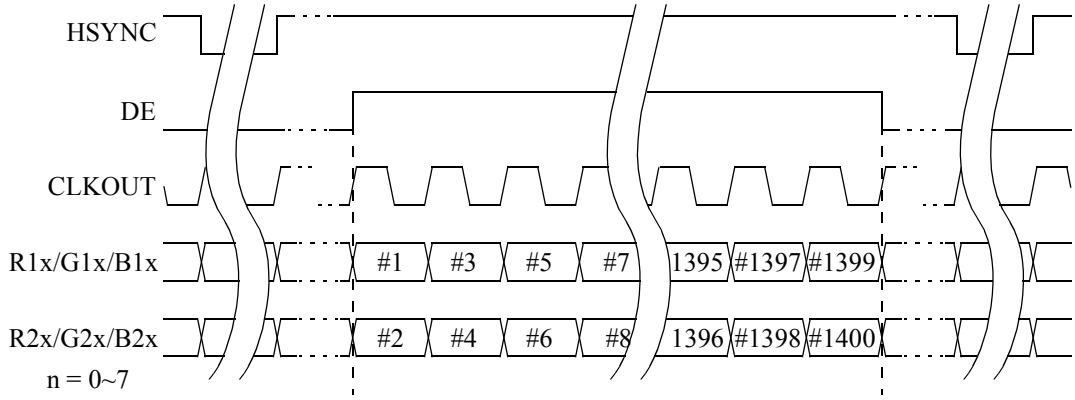
Phase Lock Loop Set Time

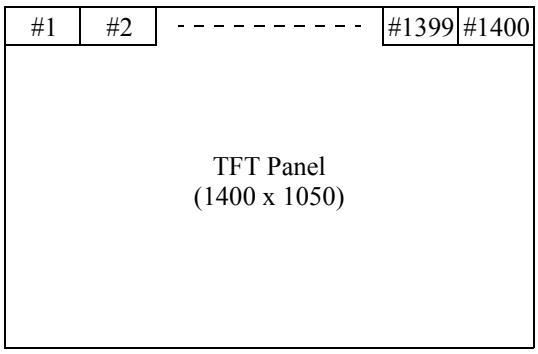


Pixel Map Table for Single/Dual Link

1st Pixel Data				2nd Pixel Data			
824 TTL Output Pin	TFT Panel Data			824 TTL Output Pin	TFT Panel Data		
		24Bit	18Bit			24Bit	18Bit
R10	LSB	R10	-	R20	LSB	R20	-
R11		R11	-	R21		R21	-
R12		R12	R10	R22		R22	R20
R13		R13	R11	R23		R23	R21
R14		R14	R12	R24		R24	R22
R15		R15	R13	R25		R25	R23
R16		R16	R14	R26		R26	R24
R17	MSB	R17	R15	R27	MSB	R27	R25
G10	LSB	G10	-	G20	LSB	G20	-
G11		G11	-	G21		G21	-
G12		G12	G10	G22		G22	G20
G13		G13	G11	G23		G23	G21
G14		G14	G12	G24		G24	G22
G15		G15	G13	G25		G25	G23
G16		G16	G14	G26		G26	G24
G17	MSB	G17	G15	G27	MSB	G27	G25
B10	LSB	B10	-	B20	LSB	B20	-
B11		B11	-	B21		B21	-
B12		B12	B10	B22		B22	B20
B13		B13	B11	B23		B23	B21
B14		B14	B12	B24		B24	B22
B15		B15	B13	B25		B25	B23
B16		B16	B14	B26		B26	B24
B17	MSB	B17	B15	B27	MSB	B27	B25

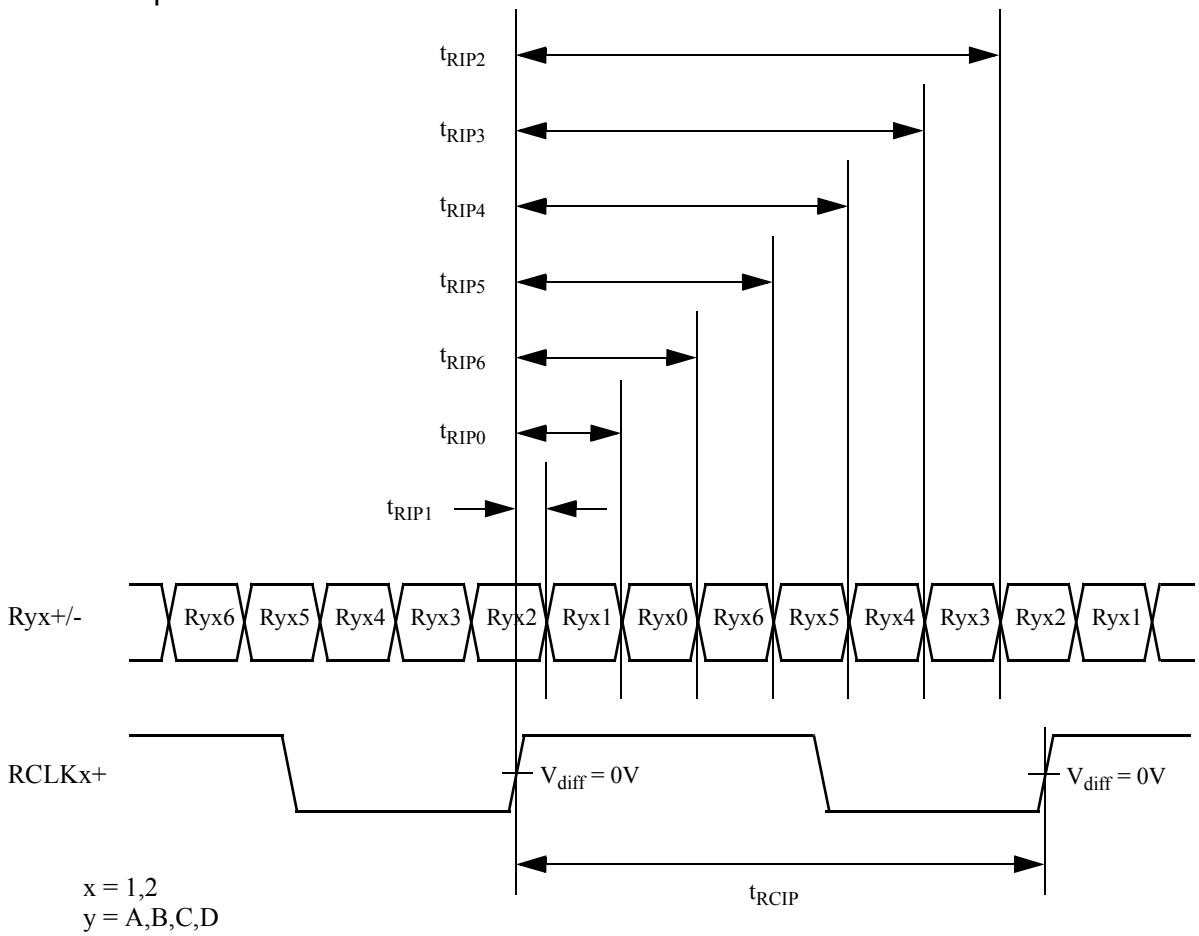
824 TTL Data Output Timing for Single/Dual Link
Example : SXGA+(1400 x 1050)



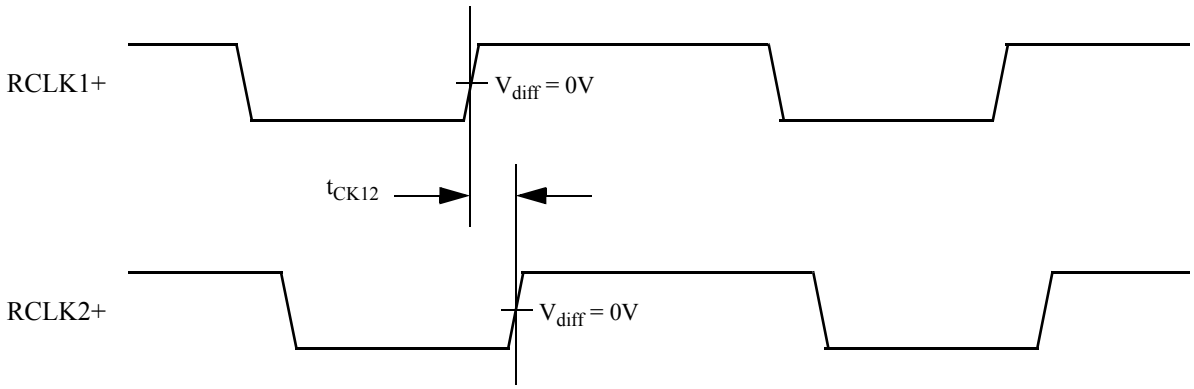


AC Timing Diagrams

LVDS Inputs

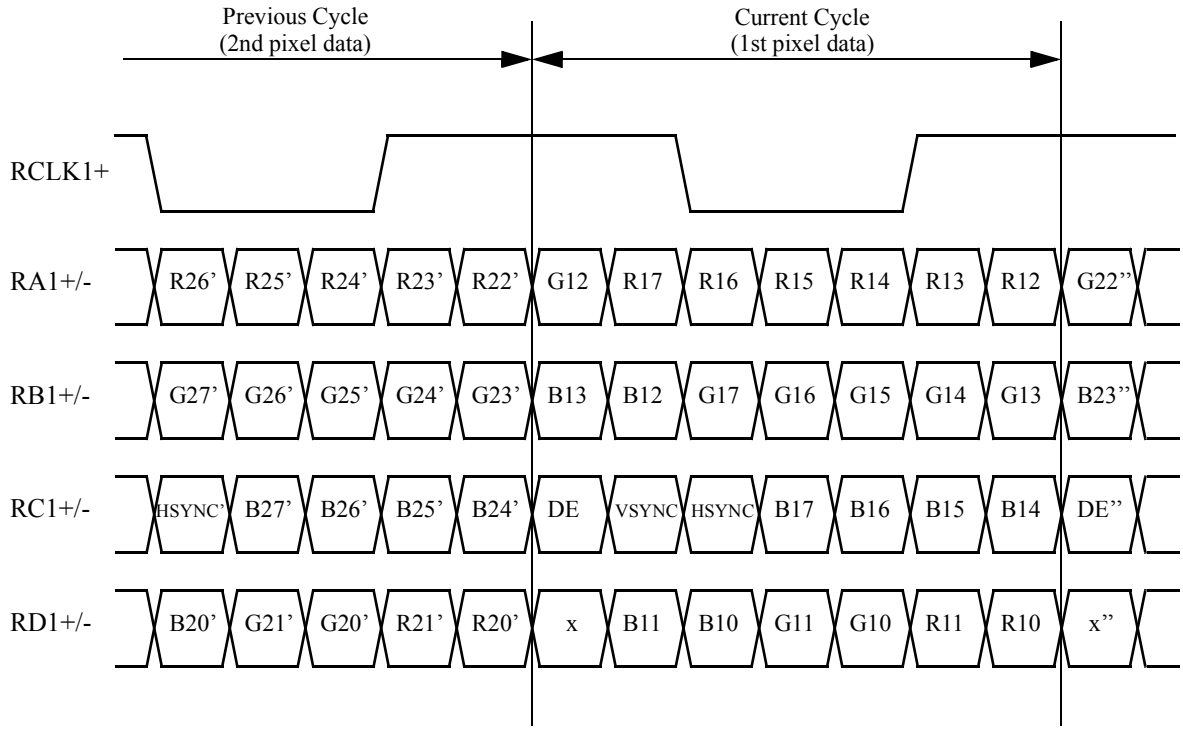


x = 1,2
y = A,B,C,D



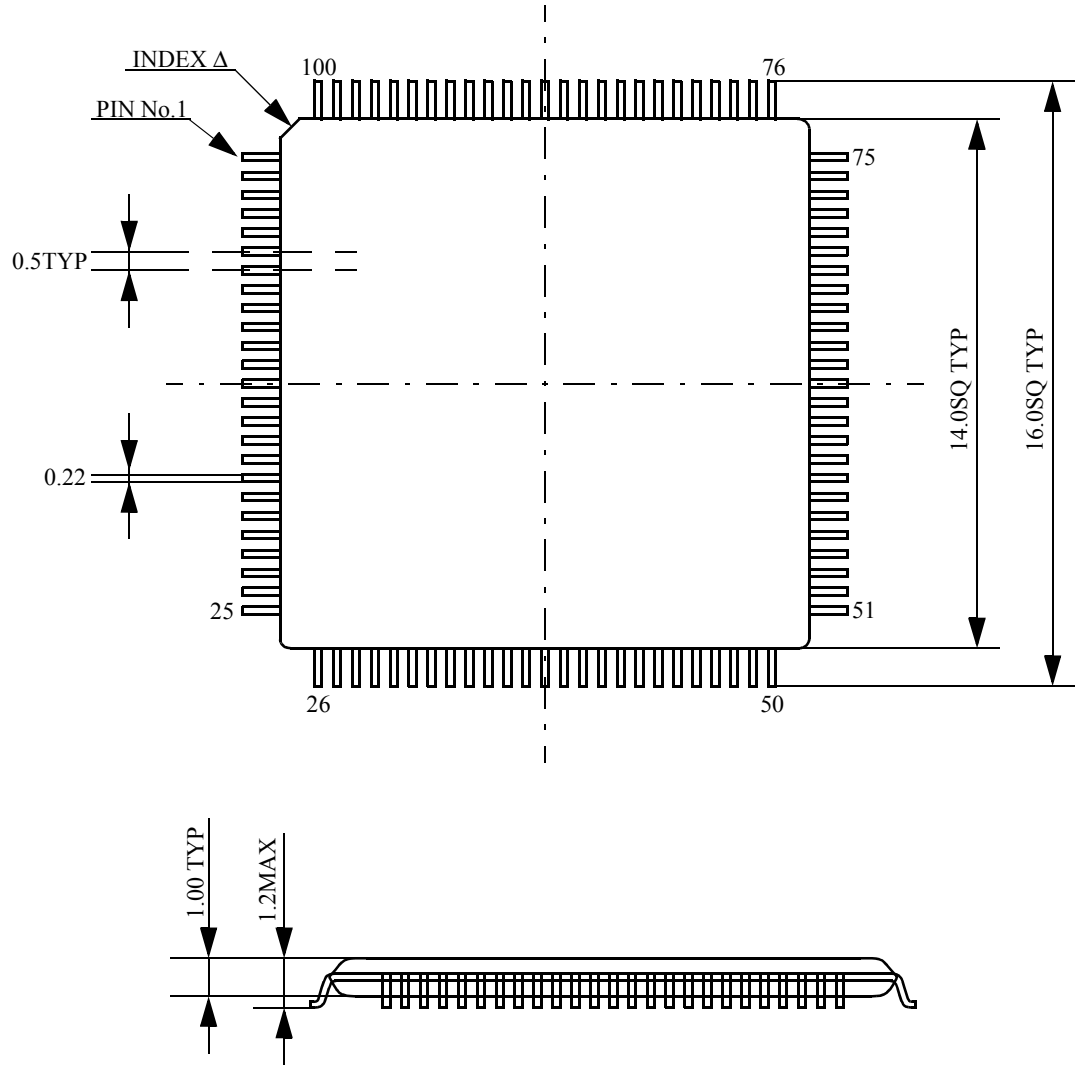
Note:
V_{diff} = (Ryx+) - (Ryx-), (RCLKx+) - (RCLKx-)

LVDS Data Inputs Timing Diagrams in Single Link



LVDS Data Inputs Timing Diagrams in Dual Link

Package



UNITS:mm

Notes to Users:

1. The contents of this data sheet are subject to change without prior notice.
2. Circuit diagrams shown in this data sheet are examples of application. Therefore, please pay sufficient attention when designing circuits. Even if there are incorrect descriptions, we are not responsible for any problem due to them. Please note that incorrect descriptions sometimes cannot be corrected immediately if found.
3. Our copyright and know-how are included in this data sheet. Duplication of the data sheet and disclosure to other persons are strictly prohibited without our permission.
4. We are not responsible for any problems of industrial proprietorship occurring during THC63LVD824 use, except for those directly related to THC63LVD824's structure, manufacture or functions. THC63LVD824 is designed on the premise that it should be used for ordinary electronic devices. Therefore, it shall not be used for applications that require extremely high-reliability (space equipment, nuclear control equipment, medical equipment that affects people's lives, etc.). In addition, when using THC63LVD824 for traffic signals, safety devices and control/safety units in transportation equipment, etc., appropriate measures should be taken.
5. We are making the utmost effort to improve the quality and reliability of our products. However, there is a very slight possibility of failure in semiconductor devices. To avoid damage to social or official organizations, much care should be taken to provide sufficient redundancy and fail-safe design.
6. No radiation-hardened design is incorporated in THC63LVD824.
7. Judgment on whether THC63LVD824 comes under strategic products prescribed by the Foreign Exchange and Foreign Trade Control Law is the user's responsibility.
8. This technical document was provisionally created during development of THC63LVD824, so there is a possibility of differences between it and the product's final specifications. When designing circuits using THC63LVD824, be sure to refer to the final technical documents.

THine Electronics, Inc.
Wakamatsu Bldg, 6F
3-3-6, Nihombashi-Honcho,
Chuo-ku, Tokyo, 103-0023 Japan
Tel: 81-3-3270-0666
Fax: 81-3-3270-0688