



Register table

Address	Register symbol	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	Control 1	TEST	0	STOP	0	TEST	0	0	0
1	Control 2	0	0	0	TI/TP	AF	TF	AIE	TIE
2	Sec	VL	S 40	S 20	S 10	S 8	S 4	S 2	S 1
3	Min	*	Min 40	Min 20	Min 10	Min 8	Min 4	Min 2	Min 1
4	Hour	*	*	Hour 20	Hour 10	Hour 8	Hour 4	Hour 2	Hour 1
5	Day	*	*	Day 20	Day 10	Day 8	Day 4	Day 2	Day 1
6	Week	*	*	*	*	*	W 4	W 2	W 1
7	Month/Century	C	*	*	Month 10	Month 8	Month 4	Month 2	Month 1
8	Year	Year 80	Year 40	Year 20	Year 10	Year 8	Year 4	Year 2	Year 1
9	Minutes Alarm	AE	A-Min 40	A-Min 20	A-Min 10	A-Min 8	A-Min 4	A-Min 2	A-Min 1
A	Hours Alarm	AE	A-Hr 40	A-Hr 20	A-Hr 10	A-Hr 8	A-Hr 4	A-Hr 2	A-Hr 1
B	Day Alarm	AE	*	A-Day 20	A-Day 10	A-Day 8	A-Day 4	A-Day 2	A-Day 1
C	Week Alarm	AE	*	*	*	*	A-W 4	A-W 2	A-W 1
D	CLKOUT frequency	FE	*	*	*	*	*	FD1	FD0
E	Timer control	TE	*	*	*	*	*	TD1	TD0
F	Timer	128	64	32	16	8	4	2	1

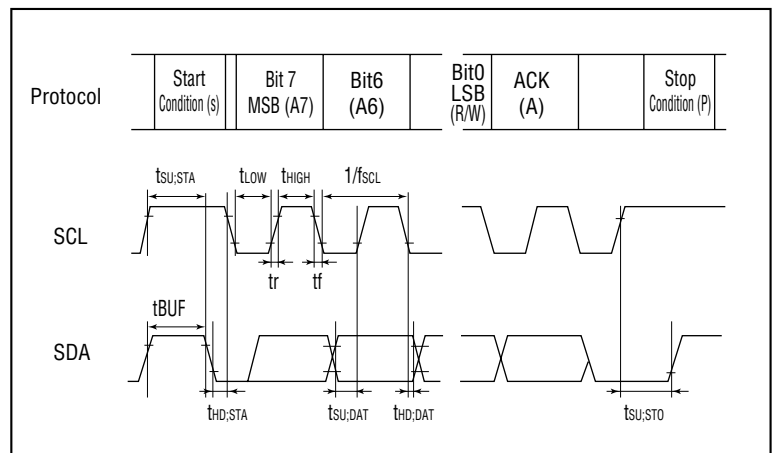
0 : Always set this bit to "0".

Switching characteristics

(V<sub>DD</sub>=1.8 to 5.5 V, T<sub>a</sub>=-40 °C to +85 °C)

Item	Symbol	Min.	Max.	Unit
SCL clock frequency	f <sub>SCL</sub>	—	400	kHz
Tolerance spike time on bus	t <sub>SW</sub>	—	50	ns
Start condition set-up time	t <sub>SU;STA</sub>	0.6	—	μs
Start condition Hold time	t <sub>HD;STA</sub>			
SCL "L" time	t <sub>LOW</sub>			
SCL "H" time	t <sub>HIGH</sub>	0.3	—	μs
SCL and SDA rise time	t <sub>r</sub>			
SCL and SDA fall time	t <sub>f</sub>	—	—	—
Date set-up time	t <sub>SU;DAT</sub>	100	—	ns
Date hold time	t <sub>HD;DAT</sub>	0		
Stop condition set-up time	t <sub>SU;STO</sub>	4.0		

Timing chart



Block diagram

