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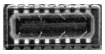
LIS-1024 High Performance Linear CMOS Image Sensor

The LIS-1024 image sensor is a high performance, very low noise linear image sensor designed for a wide variety of applications including:



P/N: LIS-1024D-LG
16-pin LCC package

- **Spectroscopy**
- **Bar Code Reading**
- **Edge Detection**
- **Contact Scanning**
- **Optical Character Recognition**
- **Encoding**
- **Position Detection**
- **And more.....**

Description

The LIS-1024 Image Sensor consist of an array of ultra low dark current photo-diode pixels with performance exceeding most Charge-Coupled Devices (CCD's). The device has multiple read out modes, including: Non-Destructive, Dynamic Pixel Reset™ (DPR), and Frame Reset.

The Non-destructive mode enables extremely low noise measurements (approaching a single electron) through the use of signal averaging, enabling the system to achieve near single electron noise performance, making the device ideally suited for any high performance measurement application. In DPR mode, each pixel is reset as it is read, ensuring each pixel integrates for the same amount of time. Other reset modes are also provided to give exceptional control over exposure time and pixel read out. The Sensor also operates over an extended power supply range of 2.8-5.0 VDC.

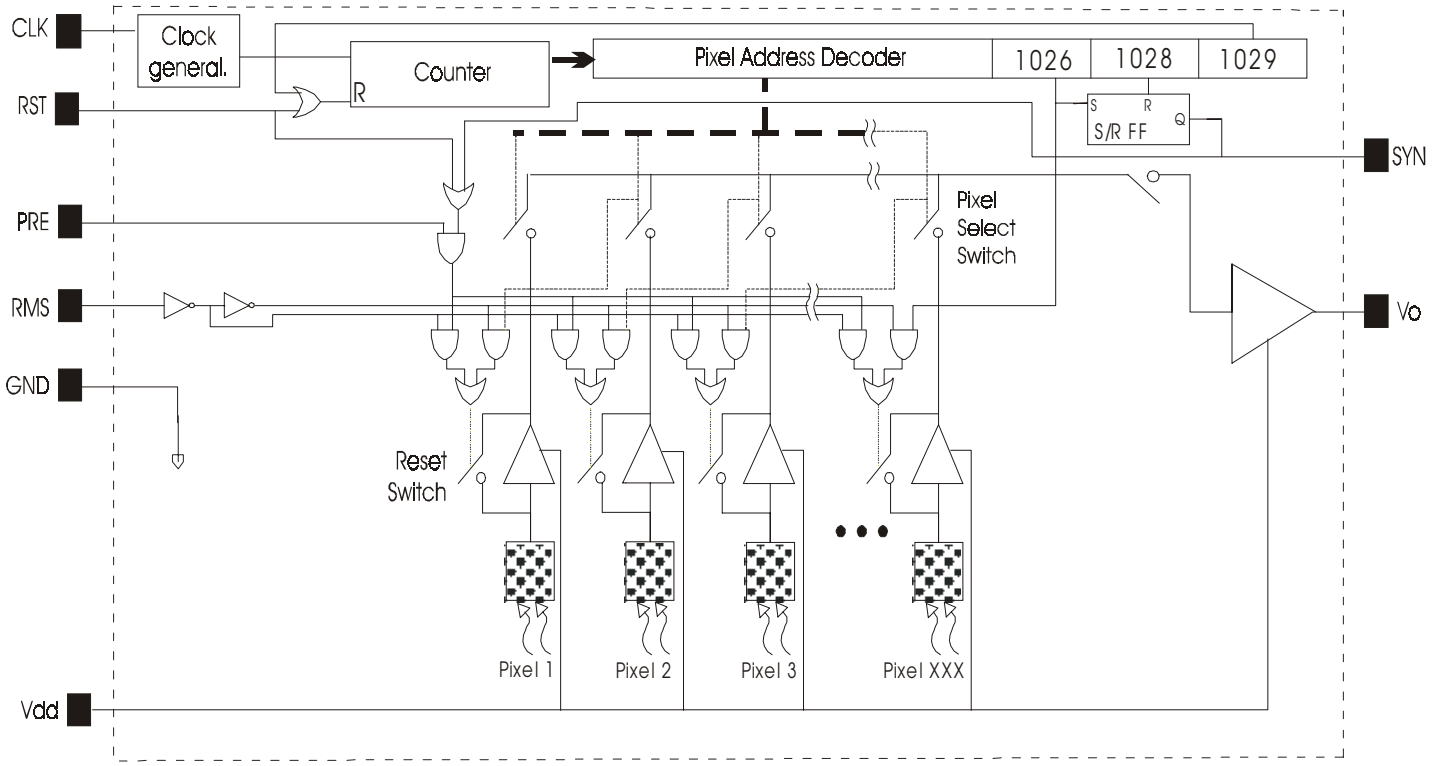
Operation is simplified by on-chip logic. The only external signals required are a clock with a frequency equal to the desired pixel read rate, a reset mode selection, and an external reset to initiate read-out when running asynchronously.

The LIS-1024 is supplied in a 16-pin LCC package as shown above.

Key Features

- Low Cost
- Single Supply Operation
- Multiple read out modes
- Ultra Low Noise (≅ 1 e^- via signal averaging)
- High Signal to Noise
- Non-Destructive read capable
- 1.0 kHz to 20.0 MHz Operation
- Very Low Dark Current
- Completely integrated Timing and Control
- Replaces CCD systems, not just the sensor
- 1 x 1024 pixel resolution
- 7.8 micron pitch x 125 microns tall
- Photo-active area: 7.988 mm x 125 microns

Functional Block Diagram



Absolute maximum ratings, T A = 25°C unless otherwise noted, see Note 1, below. †

Supply voltage range, V_{DD}---------- 0 V to 5.25 V
Digital input current range, I ---------- –20 mA to 20 mA
Input signal overshoot ---------- Vdd +0.250v (High), Vss – 0.25v (Low)
Operating free-air temperature range, T A ---------- 0°C to 50°C
Storage temperature range ---------- –20°C to 85°C
Humidity range, Rh ---------- 0-85%, non-condensing
Lead temperature 1.5 mm (0.06 inch) from case for 10 seconds----- 225°C

† Exceeding the ranges specified under "absolute maximum ratings" can damage the device. The values given are for stress ratings only. Operation of the device at conditions other than those indicated under "recommended operating conditions" is not implied. Exposing the device to absolute maximum rated conditions for extended periods may affect device reliability and performance.

NOTES: 1. Voltage values are with respect to the device GND terminal.

LIS-1024 Electrical Characteristics/Operating Conditions

(@T_A = 25°C, VDD= I/OLEVEL = 5.0VDC, CLK_{IN} = 1 MHz, unless otherwise specified)

Parameter	Conditions	Min	Typ	Max	Units
Digital Signals					
Input High Logic Level (V_{iH})		Vdd–0.6V			V
Input Low Logic Level (V_{iL})				0.6	V
Digital Out load current (I_{out})				1.0	mA
Input Clock Freq. (CLK_{IN})	Pixel Read Rate (ERC) = CLK_{IN}	1.0	1,000	20,000	MHz
Input Clock Duty Cycle		40		60	%
t pcdly - Clk to 1st pixel	Rising edge of clock		2		ns
t rsh - RST Set Up & Hold	Spec in # of Clock Cycles See Note 2	3			CLK_{IN}
t sdly - Sync Out to Clk Dly.	Rising & falling edge of Sync out to rising edge of clock	1		120	ns
t spix - Sync out to 1st pixel	Falling edge of SYN. Spec in # of Clock Cycles		2		CLK_{IN}
DC					
Supply Voltage (Vdd)	@ Supply voltages less than Sat Voltage, VO is clipped by supply, no load applied.	2.80		5.0	V
Supply Current	Including Load Resistor	8	18	50	ma
Video Output	**See Note 1**				
Video Out (VO) – Ext. Load	@ Supply voltages less than Saturation Voltage, VO is clipped by supply, no load applied.	330		10k	Ohms
Output Voltage @ Saturation		2.8	3.3	4.0	V
Output Voltage @ Dark		0.64	0.74	0.84	V
Electro-optical	**See Note 1**				
Pixel FPN - PRNU	Non-Uniformity 50% Sat		±0.3		% Total
Pixel FPN - DSNU	Non-Uniformity Dark		±0.3		% Total
Linearity	Pixel avg. from 5% - 75% Saturation		1.0		% SAT
Well Capacity (Full Well)			8.0		Me-

Sensitivity	From 5% - 75% Saturation. Unloaded video, values typical and may vary.		0.32		µv/e-
Quantum Efficiency	675nm		60		%
Output Due To Dark Current	At 24 °C	2	19	38	mV/s
Signal/Noise (RMS)	Temporal RMS noise @ 1 MHz erc and 500 KHz video bandwidth filter applied.		>84		db
Spectral Response Range		350		1100	nm
Environmental					
Relative Humidity Range		0		85	%
Operating Temperature Range		0	25	50	°C

Note 1: Specs. given at pixel read rates of 1 MHz. At higher read rates, MTF and S/N begin to degrade. End pixels response may vary from nominal array characteristics. S/N values are typical and may vary. Higher S/N ratios obtainable with lower clock speed and bandwidths.

Note 2: RST is specified to be initiated for 3 CLK_{IN} cycles to insure proper reset of pixels. Shorter pulse widths will reset the internal timing, but may not fully reset pixels.

SIGNAL DESCRIPTION & PACKAGE PINOUT

Signal	I/O type	Definition	8 Pin DIP	16 Pad LCC
GND	-----	Ground Reference.	1	1
CLK	Input	Clock	2	3
PRE	Input	Pixel Reset Enable	3	5
RMS	Input	Reset Mode Select	4	7
RST	Input	External Reset/Start pixel read	5	10
VO	Output	Video Output	6	12
SYN	Output	Sync Output	7	14
VDD	Input	Supply Voltage	8	16

OPERATION AND TIMING

The device offers multiple modes of operation including:

- Dynamic Pixel Reset™ (DPR) Mode: Each pixel is reset after reading,
- Dynamic Pixel Reset™ (DPR) Non-Destructive Mode: Each pixel is allowed to integrate even after reading,
- Frame Mode Destructive Read: All pixels are reset all at once
- Frame Mode Non-Destructive Read: All pixels originally reset at once and allowed to integrate after reading.

Example timing diagrams are given below. The user determines mode of operation by selecting logic levels for the PRE (Pixel Reset Enable) pin and the RMS (Reset Mode Select) pin. The device requires a clock frequency equal to the desired pixel read rate. In frame mode, a read cycle is initiated by the internal reset node or by pulsing the RST pin. See the Reset Mode Truth Table for all modes of operation.

In all modes, the end of each frame is identified with a pulse being output on the SYN pin. This SYN pulse will go high on the rising edge of the 1026 clock cycle count for that frame. The SYN pulse goes low on the rising edge of the 1028 clock count. The Sync Output (SYN) pin goes high for 2 clock counts. The internal counter is reset on the rising edge of the 1029 clock count.

Mode inputs RMS & PRE may be initiated asynchronously. It is recommended that changes to mode inputs be made between counts 1025 (after last pixel) and 1028 (falling edge of sync out). One full frame of video may be required to achieve valid data, dependant on when PRE, and RMS are initiated.

RST pin is used for external reset. RST may be initiated asynchronously One full frame of video may be required to achieve valid data, dependant on when RST is initiated in DPR modes. Active high, RST resets the internal counter, and resets pixels when PRE is held low. Initiating RST pin interrupts SYN output.

NOTES TO TIMING DIAGRAMS

1. Clock duty cycle should be 40% to 60%.
2. 1024 Clock cycles for the number of pixels to read, starting at the first pixel.
3. t int represents integration time.
4. t cnt represents clock cycle count
5. t rpix represents time between falling edge of RST and 1st rising edge of CLK_{IN}
6. RST pulse always resets internal counter, thus next pixel output is the first pixel.

Figure 1: LIS-1024 Free Running Timing Setup

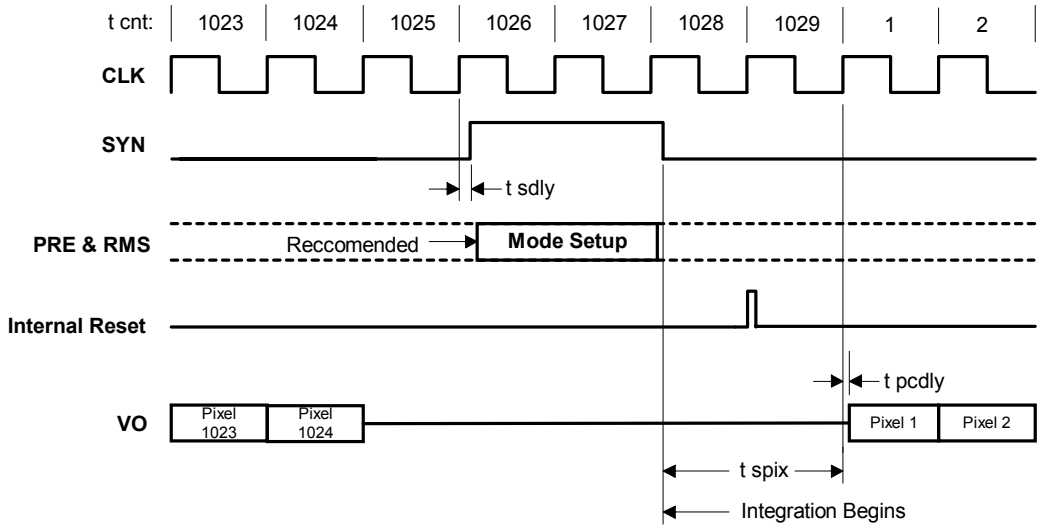


Figure 2: LIS-1024 External Reset Timing Setup (PRE Held High)

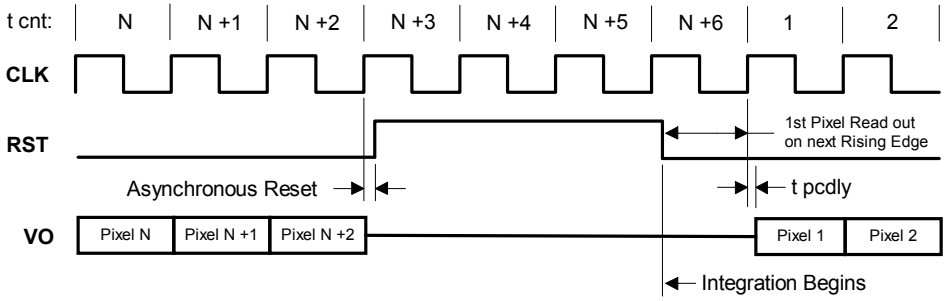
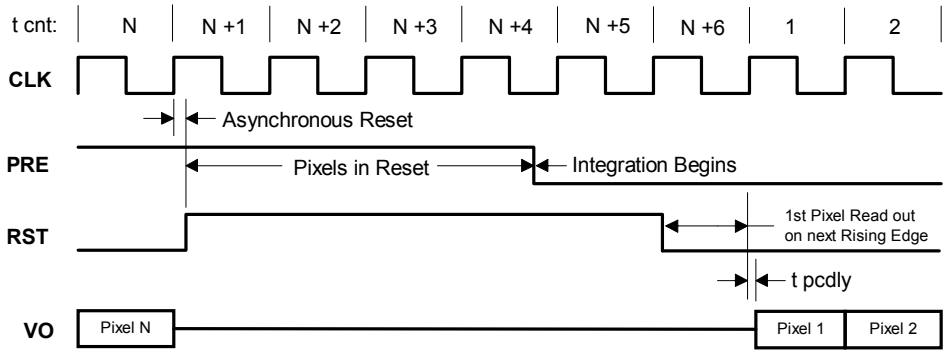


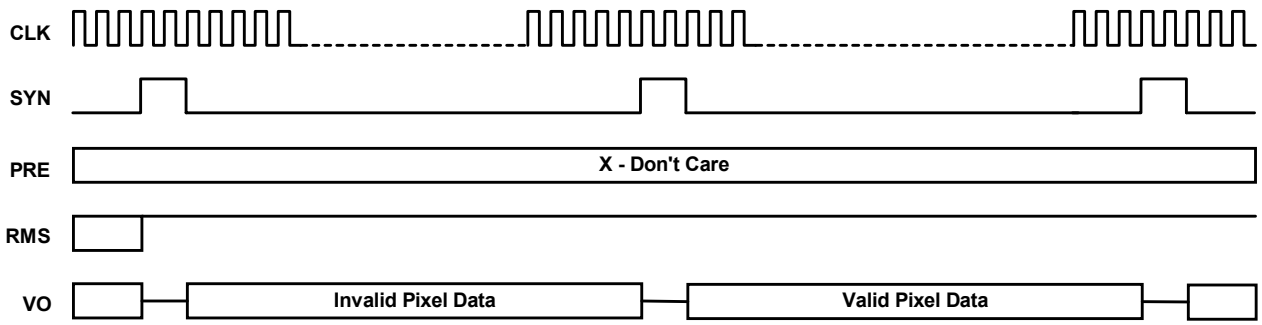
Figure 3: LIS-1024 External Reset Timing Setup Using PRE To Control Pixel Reset & Integration



DYNAMIC PIXEL RESET™ (DPR) MODE.

In this mode, pixels are reset as they are sequentially read. This assures identical integration time for each pixel. Clock must run for 1028 (1024+4) clock cycles for internal counter to reset if relying on the internal logic, or the user can reset externally. If reset externally, it will require one full frame to establish equal integration time for each pixel. In all cases it takes the first full frame of video to establish equal integration time for each pixel. See Reset Mode Truth Table below for more details. The pixel integration time in this mode is equal to the clock period times 1028 (4 + number of 1024 pixels) in the device. The device will operate well at speeds to 12 MHz, at speeds faster than this, DPR™ mode of operation is not recommended, but instead choose one of the frame modes.

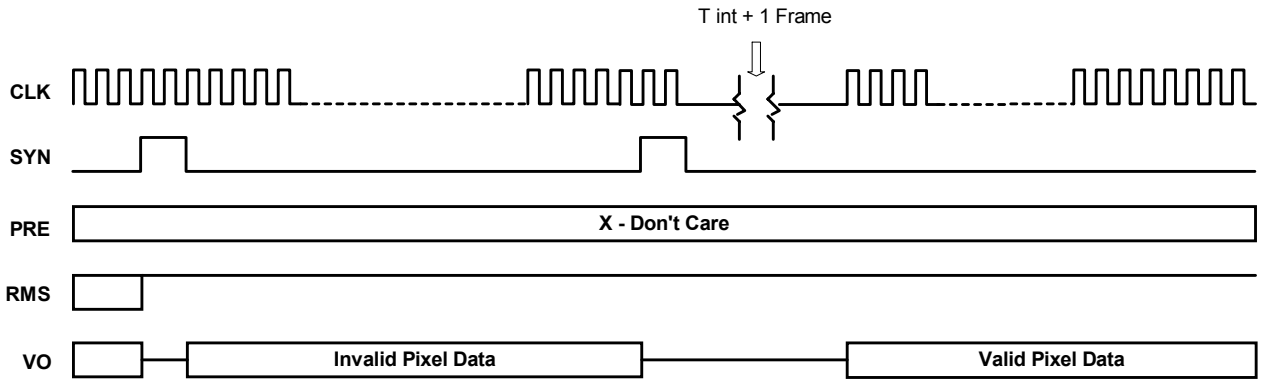
Figure 4: Dynamic Pixel Reset (DPR) Timing



DYNAMIC PIXEL RESET™ (DPR) NON-DESTRUCTIVE MODE.

In this mode, as in the DPR mode the pixels are reset as they are sequentially read. This assures identical integration time for each pixel. Initially clock must run for 1028 (1024+4) clock cycles for internal counter to reset if relying on the internal logic, or the user can reset externally. If reset externally, it will require one full frame to establish equal integration time for each pixel. In all cases it takes the first full frame of video to establish equal integration time for each pixel. See Reset Mode Truth Table below for more details. In order to extend integration time, clock is to be held low after the 1028 cycle. The pixel integration time in this mode is equal to the clock period times 4 + number of pixels (1024) + time clock is held low. The device will operate well at speeds to 12 MHz, at speeds faster than this, Dynamic Pixel Reset (DPR) Non-Destructive Mode of operation is not recommended, but instead choose one of the frame modes.

Figure 5: Dynamic Pixel Reset (DPR) Non-Destructive Read Timing



FRAME MODE - DESTRUCTIVE READ

In Frame Mode - Destructive Read, all pixels & internal counter are reset by internal resets generated at the end of frame see "Operation & Timing", or by initiating a reset pulse at pin RST. It is important to note that integration time for the each pixel is dependent on its position in the array. In strobed or pulsed light source applications it is desirable to initiate the event before the first pixel is read to provide even pixel-to-pixel integration of the event. Flat field illumination will result in a video ramp. The timing for Frame Mode - Non Destructive read applies, except that taking the PRE line high will cause the pixels to be reset when the RST pin goes high. This mode is ideal for Strobe applications.

Figure 6: Frame Mode Destructive Read Timing

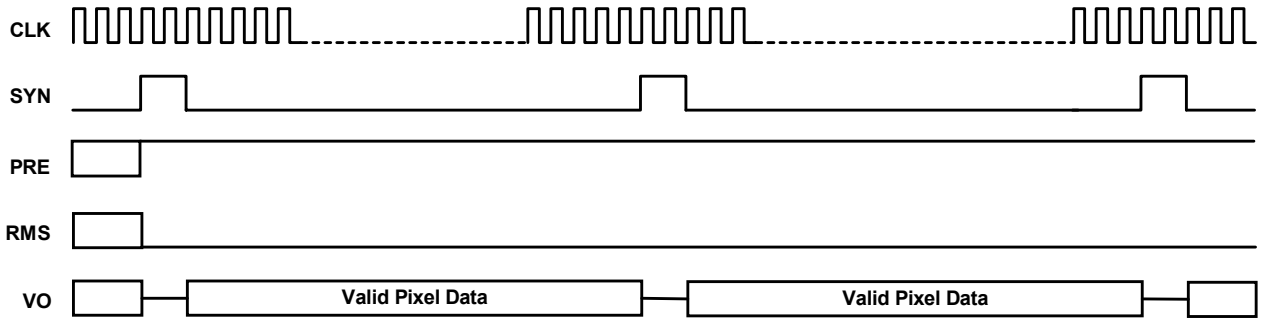
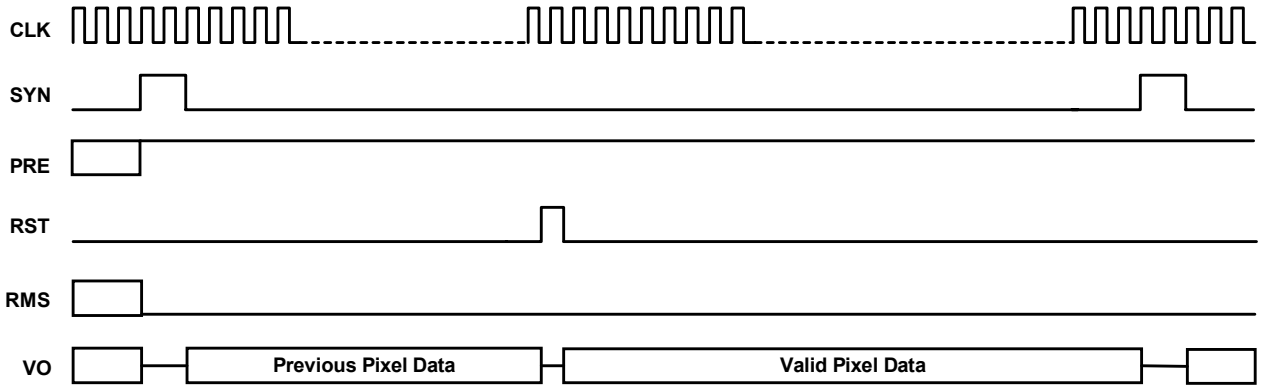
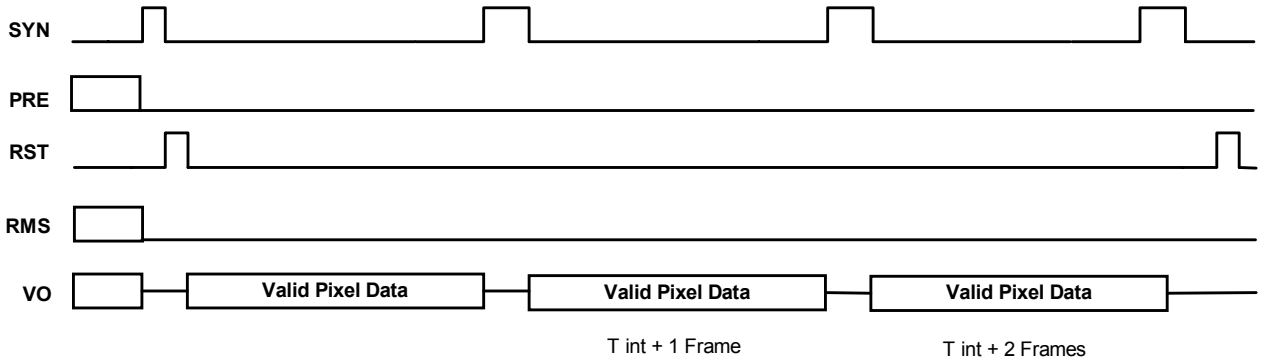


Figure 7: Frame Mode Destructive Read with External Reset Timing



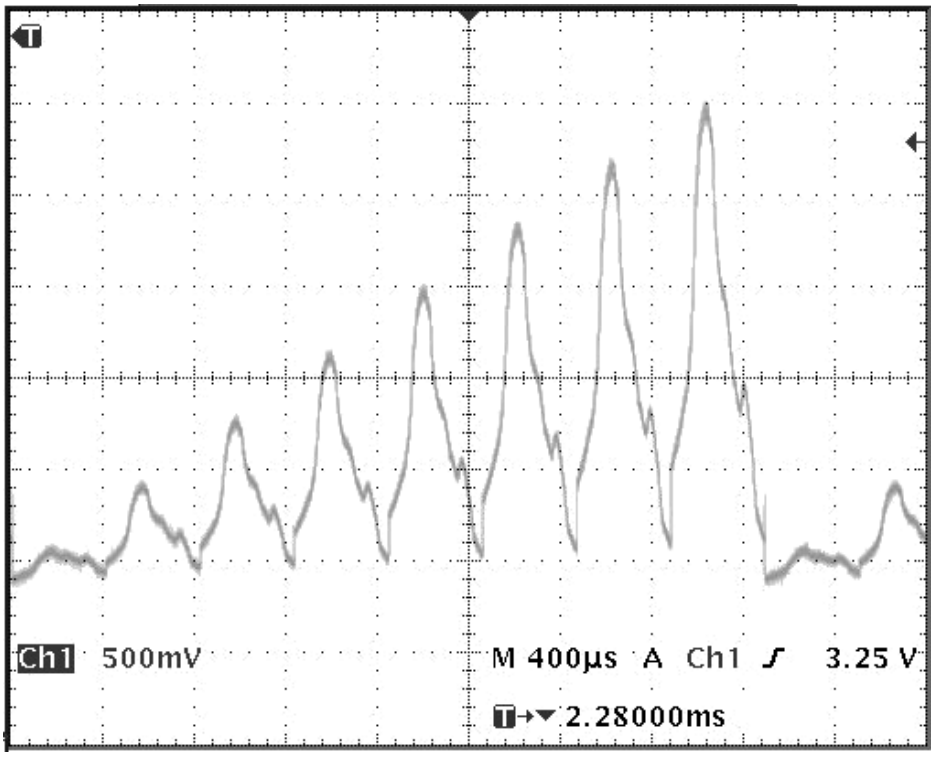
FRAME MODE - NON-DESTRUCTIVE READ

Figure 8: Frame Mode Non-Destructive Read Timing



In this mode, the RST pulse resets the internal counter, and the video out is set to read the first pixel. Because the Pixel Reset Inhibit (PRE) line is held low, the pixels are not reset, and the image is preserved and read out in subsequent frame(s). The sensor will continue to integrate and read out until RST is pulsed or mode pins RMS & PRE are toggled. Long integration times result in integrating pixel dark current, and can be reduced by cooling the device.

Figure 9: Frame Mode Non-Destructive Read Output Trace



LIS-1024 in Non-Destructive Frame Mode running at 2.5 mHz pixel read rate for eight frames

RESET MODE TRUTH TABLE:

The following truth table summarizes the various reset modes, and readout modes.

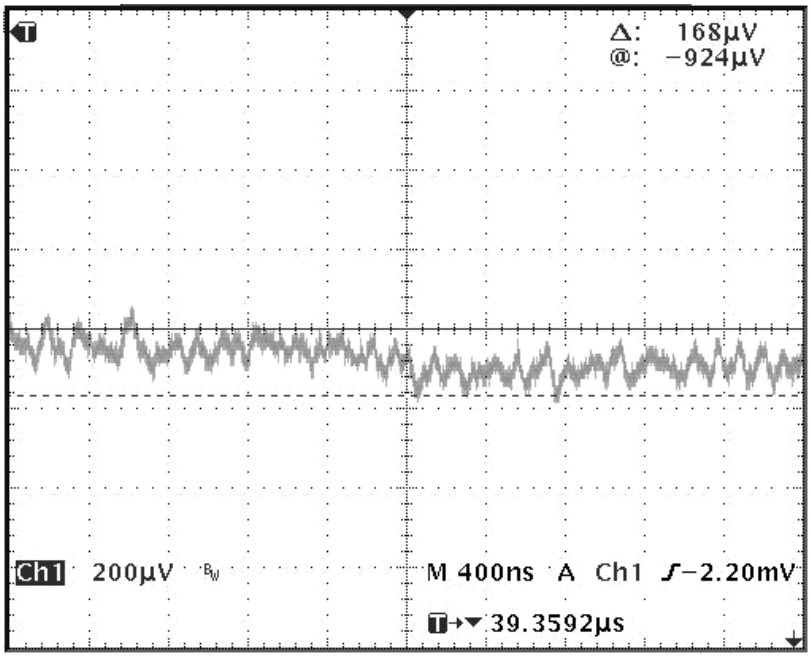
MODE	RST	RMS	PRE	PIXEL RESET OR INTEGRATING	COUNTER RESET OR NORMAL	NOTES
0	0	0	0	INTEGRATING	NORMAL	Frame mode, continuous integration.
1	0	0	1	ALL PIX. RESET	NORMAL	Frame mode, all pixels reset.
2	0	1	X	DPR RESET	NORMAL	DPR mode, previous pixel reset
3	1	0	0	INTEGRATING	RESET	External reset, frame mode, continuous integration
4	1	0	1	ALL PIX. RESET	RESET	External reset, frame mode, all pixels reset
5	1	1	X	DPR RESET	RESET	External reset, DPR mode, previous pixel reset

0 = Logic 0, 1 = Logic 1, X = Don't Care

VIDEO OUTPUT

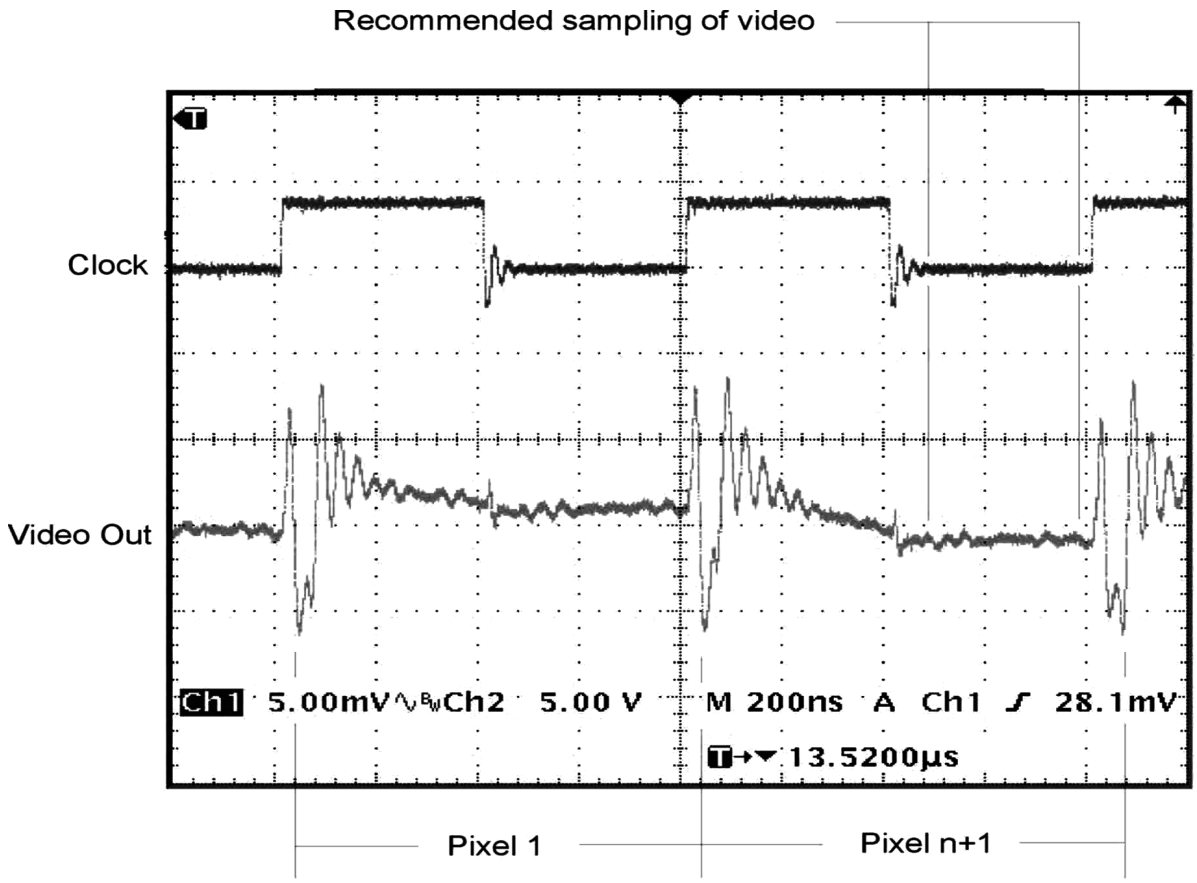
The LIS1024 is capable of a 2.5v output swing into 330 to 10k ohm load. It is advised that applications utilizing an A/D converter to sample on the second half (55% to 95% is optimum) of readout time of each pixel. This allows the column & output amplifiers to settle from each transition from pixel to pixel, and from system clock edges. Second half occurs during logic low (0) of CLK signal. See figure 11.

Figure 10: Black Level Output Trace.

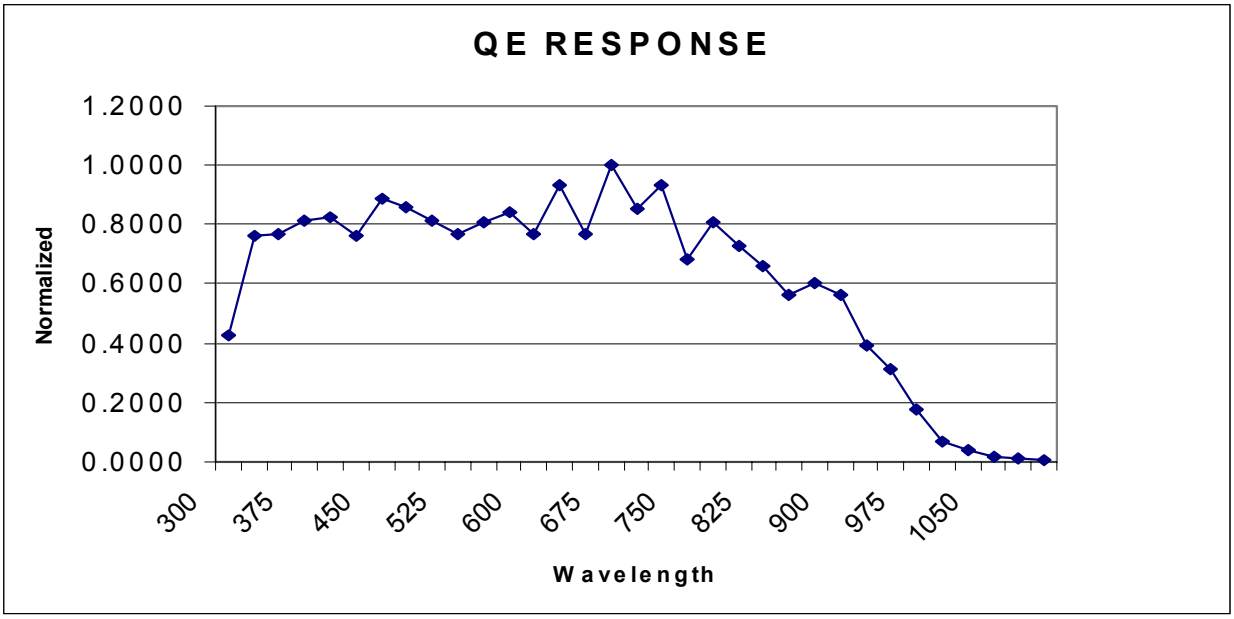


LIS-1024 scope trace with scope probe AC coupled. Output showing peak to peak noise levels of 300 µV at full dark. 156.25 KHz Clk/Read Rate @ 100Khz Filter. Peak signal to RMS noise (S/N) well in excess of 90db.

Figure 11: Video Output Trace.



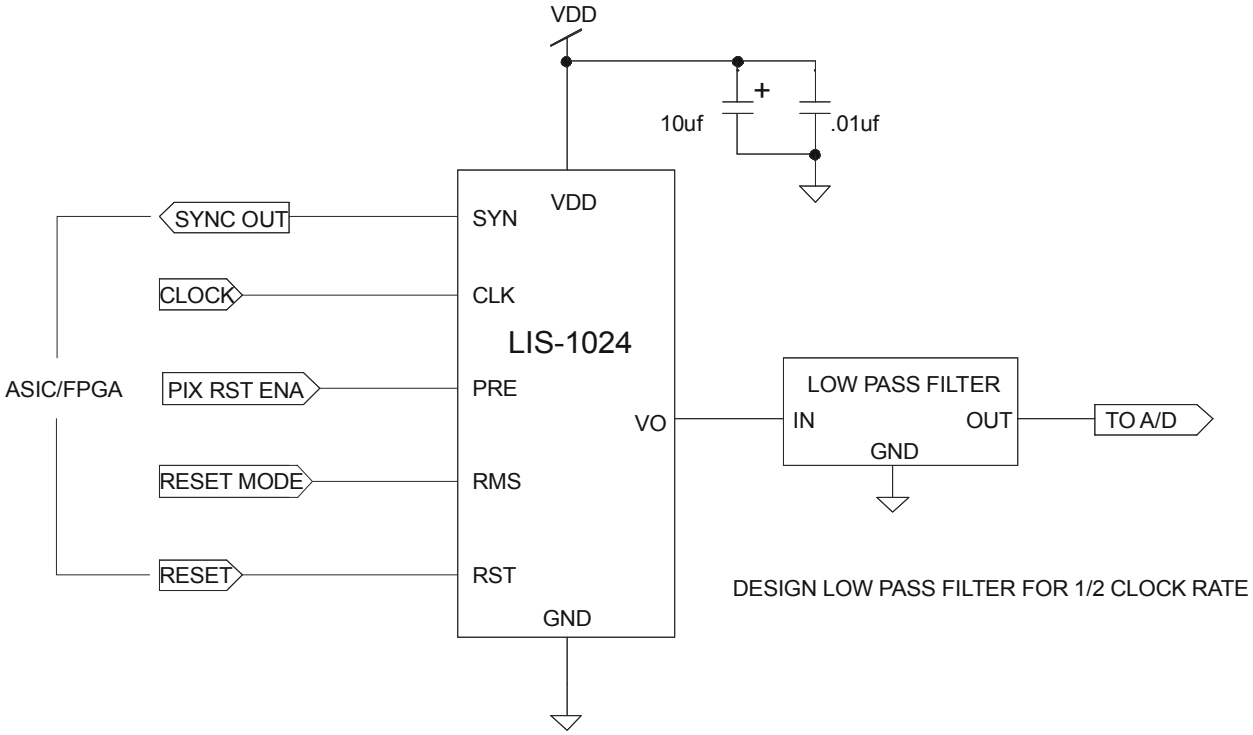
LIS1024 raw video output (no filter), 1.25 mHz clock rate.



Note: Data below 350nm not measured, but device is sensitive to 200 nm. Shown for un-

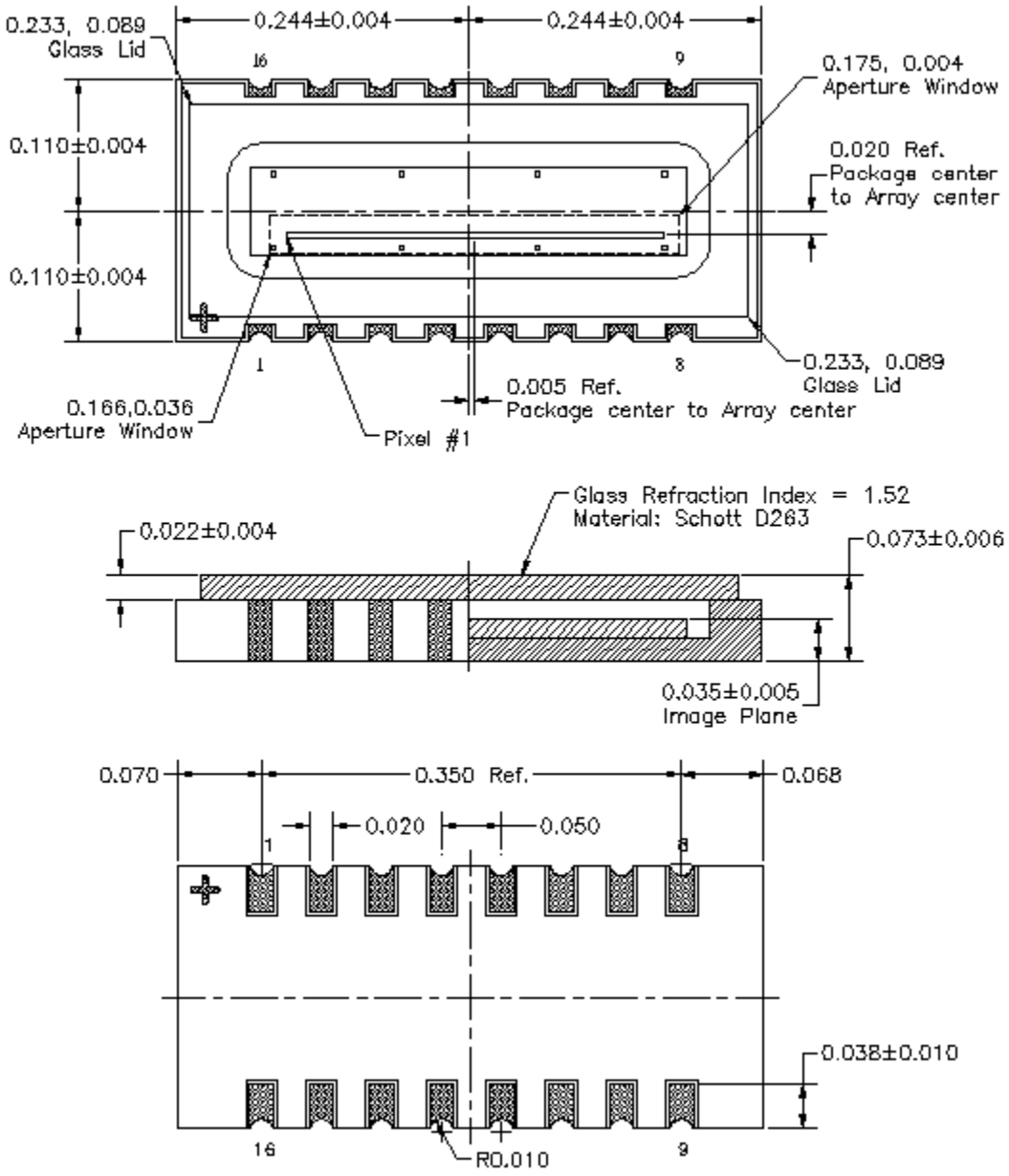
TYPICAL APPICATION CIRCUIT:

The following shows the LIS-1024 in a common application, interfacing to a A/D converter.



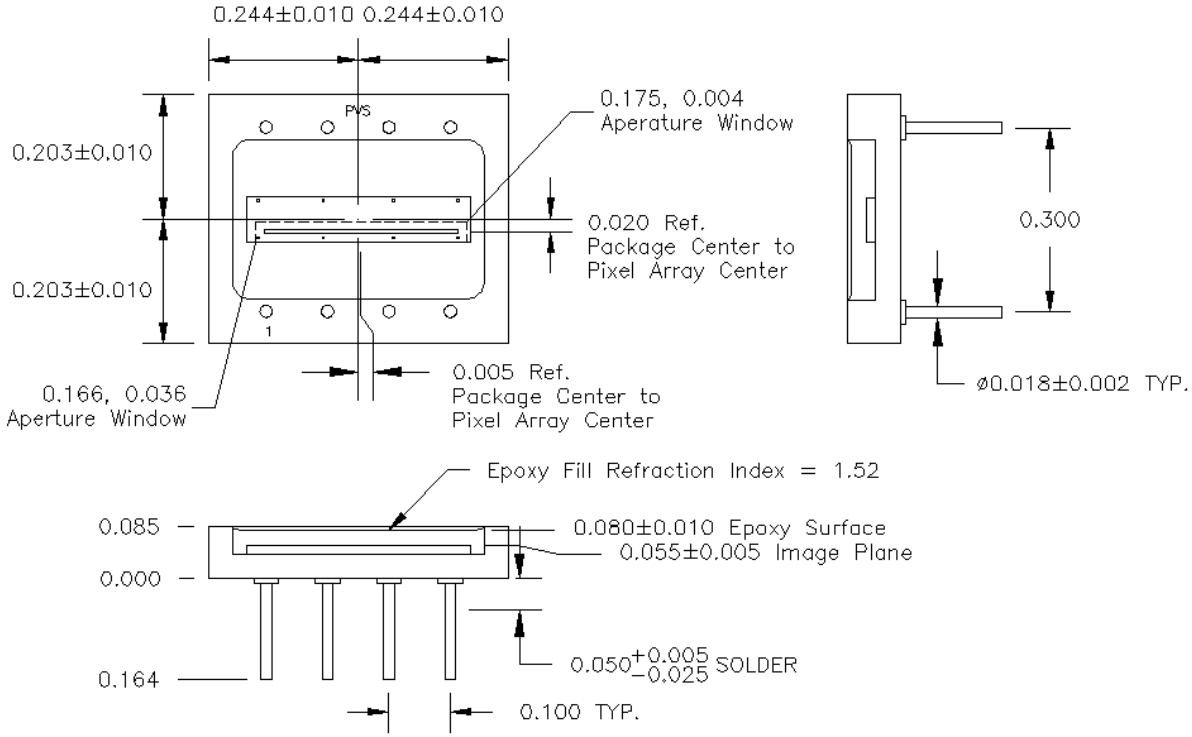
Package & Optical Information:

LIS1024 in 16 Pad LCC
P/N: LIS-1024D-LG



For additional 16 Pad LCC package info see drawing: 40085

LIS1024 in 8 Pin DIP (NOT FOR NEW DESIGNS)
P/N: LIS-1024D-DE



For additional 8 pin dip package info see drawing: 40072

ORDERING INFORMATION

P/N: LIS-1024A-LG Leadless Chip Carrier (LCC)

P/N: LIS-1024D-DE 8 pin DIP package (DO NOT USE FOR NEW DESIGNS)

Contact PVS or your local authorized representative for availability.

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This imager may be covered under the following patent: 6,084,229