IM29F002T and IM29F002B
2 M Bit (256K x 8) 5V-Only Flash Memory

Features:

- **0.40 µm, triple-poly double-metal CMOS process**
- **Single power supply operation**
  5V ± 10% for both read and write
- **High endurance**
  > 10,000 program/erase cycles
- **Fast read access time**
  45, 55, 70, and 90 ns
- **Single page erasability for optimal data alterability**
  Page size: 512 bytes
- **Hardwired data protection**
  Inhibits program and erase operations of the top (IM29F002T) or bottom (IM29F002B) 32 pages of the array for false write and virus prevention.
- **Flexible boot block configurability**
- **Fast program and erase operations:**
  Byte program : < 20 µsec typical
  Page erase : < 6 msec typical
  Chip erase : < 2 sec typical
- **Self-timed program/erase operations with end-of-cycle detection**
  Data# Polling and Toggle Bit
- **Inadvertent write protection**
  Glitch filtering for WE# and CE#
  Low Vcc (< 3.5 V) write inhibit
  Hardwired data protection
- **Low Icc for power conservation**
  Read: 20 ma typical
  Write: 30 ma typical
  Stand-by: 25 µA typical
- **Compatible with JEDEC byte wide pin-out and single-supply flash command standards**
- **Package types:**
  32-pin PLCC, TSOP and PDIP
  Others available upon request

General Descriptions

The IM29F002T/B is a 2 Mega-bit, 5V-only page erasable flash memory organized as 256K X 8 bits. It is manufactured with IMT's proprietary double metal, 0.40 µm CMOS flash technology. High performance cell design and advanced process technology attain better reliability, manufacturability, circuit performance and future scaleability than other alternative approaches. Fast, self-timed program/erase operations are made possible with an innovative cell and array architecture which is free from the over-erase problem of the traditional stacked-gate structures.

Single page (512 bytes) data alterability ensures optimum flexibility and efficiency in program codes, parameters and data storage. It also allows backward compatibility to other large-erase-block based flash products for direct replacement.

The IM29F002T/B is designed with interface features for direct in-system programming and erase operations. Vendor re-programmable, hardwired data protection is provided for absolute prevention in inadvertent data alteration and virus infection.

The IM29F002 conforms to the JEDEC byte wide memory pin-out and single supply flash command standards.

Designed, manufactured and tested for extended endurance applications, the IM29F002 is specified for more than 10^4 cycling endurance and greater than 10 years of data retention.

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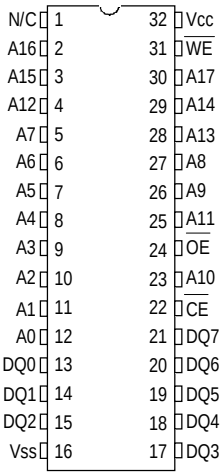
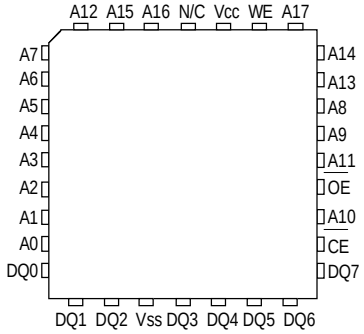
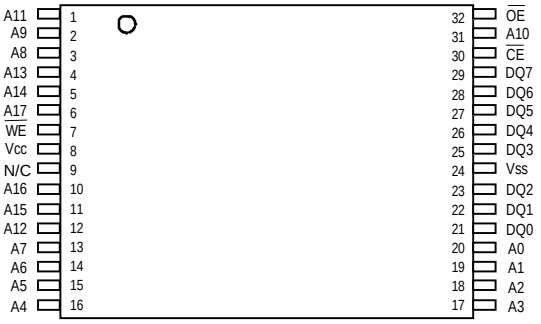
Pin-out Assignments



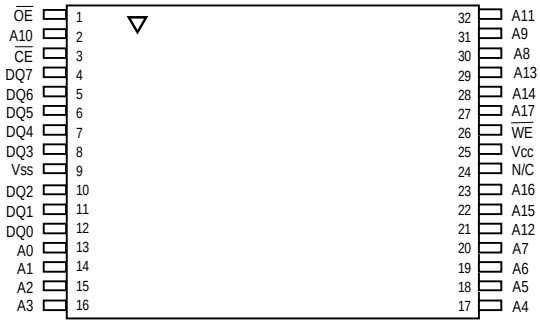
32-pin PDIP



32-pin PLCC

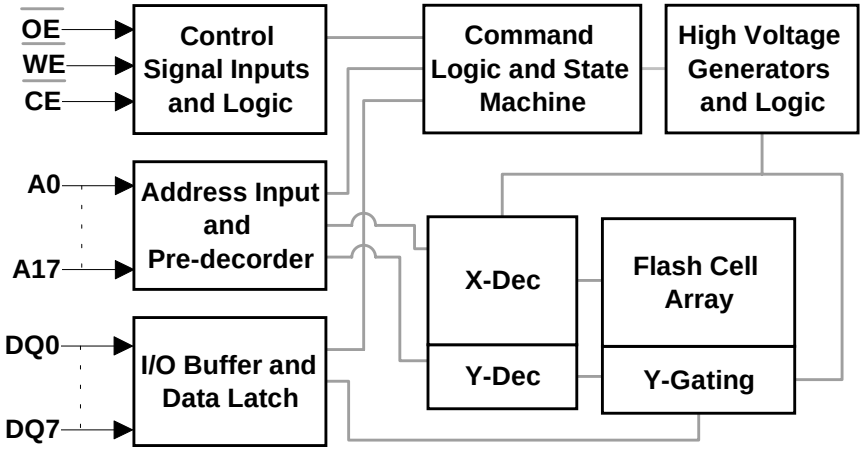


Standard 32-pin TSOP



Reverse 32-pin TSOP

Block Diagram



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Flexible Boot Block Architecture

The page erase function of IM29F002T/B erases only the bytes located inside the 512-byte boundary (as defined by A9 - A17) of the selected page. It does not affect any other memory location outside of the page boundary. Any page of the array can be used as an independent data storage unit which is not affected by the erase and programming operations of the rest of the array. A boot block of any size can be constructed by selecting a contiguous, or non-contiguous if so desired, group of pages from the top or bottom address. This provides the most convenient boot block configuration than those utilizing the fixed-size boot block approach.

Hard Wired Data Protection

A hard wired data protection option is provided for the first 32 pages either from the top address (IM29F002T) or from the bottom address (IM29F002B). This option can be utilized to protect the BIOS boot codes which usually reside in the top or bottom 16K-byte address range.

Device Operation

Read

The read operation of the IM29F002T/B is activated by setting CE# and OE# to low (V_{IL}) and WE# to high (V_{IH}). Data is obtained from the output pins. CE# controls the device selection function. When CE# is high, the device is deselected and only standby power is consumed. When CE# is low, the device is selected. OE# controls the output buffer. It is used to gate data from the output pins. The data bus is in high impedance state when either CE# or OE# is high. See Fig. 1 for the read cycle timing diagram.

Write

The write operation is used to issue commands and data for the program and erase functions of the device. It is initiated by forcing CE# low, OE# high and WE# low. The addresses are latched by the falling edge of either CE# or WE#, whichever occurs last. The data is latched by the rising edge of either CE# or WE#, whichever occurs first. See Fig. 2 for the timing diagram of writing a command with WE# as the controlling signal, and Fig. 3 for that with CE# as the controlling signal.

Erase: Page and Chip Erase

The IM29F002T/B provides two erase functions: page erase and chip erase. The page erase function erases a single page (512 bytes in size) at a time. It is activated by writing the page erase command to the part. The page erase command is consisted of 6 write cycles as shown in Table 2. The first 5 cycles contain the command codes, while the 6th cycle asserts the page address (A9 to A17) by forcing the correct address signals to the address pins. See Fig. 9 for the flow chart and Fig. 5 for the page erase timing diagram. The chip erase function erases the complete 2 mega-bit array simultaneously. It is activated by a 6-byte command cycle shown in Table 2. See Fig. 6 for the timing diagram and Fig. 10 for the flow chart.

The page and chip erase operations, once initiated, will trigger an internal timer to start the erase operation until completion, which takes typically 6 ms for the page and 2 sec for the chip erase. During this period, the data and address buses of the part are in high impedance states. The system buses are free for other operations.

OPERATION	CE#	OE#	WE#	A0	A1	A9	I/O
Read	V_{IL}	V_{IL}	V_{IH}	A_{in} Note 1	A_{in} Note 1	A_{in} Note 1	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HIGHZ
Output Disable	V_{IL}	V_{IH}	V_{IH}	X	X	X	HIGHZ
Write	V_{IL}	V_{IH}	V_{IL}	A_{in} Note 1	A_{in} Note 1	A_{in} Note 1	D_{IN}
Enable Hardwired Data Protect	V_{IL}	V_H Note 1	V_{IL}	X	X	V_H Note 1	X
Disable Hardwired Data Protect	V_H	V_H Note 1	V_{IL}	X	X	V_H Note 1	X
Verify Hardwired Data Protect	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IH}	V_H Note 1	CODE
Product Identification							
Manufacturer ID Byte 1	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	V_H Note 1	7FH
Byte 2	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IH}	V_H Note 1	1FH
Device ID	V_{IL}	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_H Note 1	A1H/A2H Note 2

Note 1: V_H=12 V, A_{in} = address input, X = don't care.
Note 2: A1H for IM29F002T and A2H for IM29F002B

Table 1 Operation Modes

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Program

Byte program operation is initiated by issuing a program command which is consisted of 4 write cycles as shown in Table 2. The first 3 cycles contain the command codes and the 4th cycle asserts the byte address and data. See Fig. 11 for the flow chart and Fig. 4 for the timing diagram. The program operation, once initiated, will continue internally until completion, typically within 20 µs. During the byte programming period, the data and address buses of the part are in high impedance state. The system buses are free for other operations. For example, during the byte programming period, the host is free to perform other tasks, such as to fetch data from other locations in the system for the next byte-program operation.

Program/Erase Status Detection: Data# Polling and Toggle Bit

The IM29F002T/B provides two status bits for detecting the completion of a program or erase period. They are the Data# Polling (DQ_7) and Toggle (DQ_6) bits. During the program or erase operation, the only valid read operations of the part are to read Data# Polling and Toggle Bits. Both bits are enabled and can be detected after the program or erase cycle is initiated by the first rising edge of WE# or CE# signal. See Fig. 7 and 8 for the timing diagrams and Fig. 9, 10 and 11 for the flow charts representation of the usage of Data# Polling and Toggle Bit in page erase, chip erase and byte program operations.

Data# Polling (DQ_7)

When the IM29F002T/B is in the program or erase period, any attempt to read DQ_7 will receive the complement of the intended data of the program or erase operation. Once the program or erase cycle is completed, DQ_7 will show true data. The device is then ready for the next operation. See Fig. 7 for Data# Polling timing diagram.

Toggle Bit (DQ_6)

During the program or erase cycle, any consecutive attempts to read DQ_6 will produce alternating 0's and 1's. It will start with "0" and then toggle between "0" and "1". When the program or erase cycle is completed, the toggling action will stop. The device is then ready for the next operation. See Fig. 8 for Toggle Bit timing diagram.

Data Protection

The IM29F002T/B provides both hardware and software features to protect nonvolatile data from inadvertent writes.

Optional Hardwired data protection for selected sectors: The program and erase operations of the first (IM29F002T) or last (IM29F002B) 32 pages can be disabled permanently to prevent false write and/or virus infection. As shown in Table 1, the hardwired protection mode can be enabled by applying V_H, or 12 Volt, to A9 and OE#, and V_{IL} to CE# and WE#. The mode can be disabled by applying the same voltages to the above pins except CE#, where V_H is applied. To verify the status of the hardwired data protection mode, A9 is set to V_H (or 12 Volt), CE#, OE# and A0 to V_{IL}, and WE# and A1 to V_{IH}. If D0 = "1" then the hardwired data protection mode is enabled. Or vice versa, if

Command	First Cycle		Second Cycle		Third Cycle		Fourth Cycle		Fifth Cycle		Sixth Cycle	
	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read	xxxxH	F0H										
Reset/ Read	5555H	AAH	2AAAH	55H	5555H	F0H	Byte Add	Byte Data				
Program	5555H	AAH	2AAAH	55H	5555H	A0H	Byte Add	Byte Data				
Page Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	Page Add	30H
Chip Erase	5555H	AAH	2AAAH	55H	5555H	80H	5555H	AAH	2AAAH	55H	5555H	10H
Product Identification												
Manufacturer ID												
Byte 1	5555H	AAH	2AAAH	55H	5555H	90H	xx00H	7FH				
Byte 2	5555H	AAH	2AAAH	55H	5555H	90H	xx11H	1FH				
Device ID	5555H	AAH	2AAAH	55H	5555H	90H	xx01H	A1H/A2H[Note]				

Note: A1H for IM29F002T and A2H for IM29F002B

Table 2 Command Definitions

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Command	First Cycle		Second Cycle		Third Cycle		Fourth Cycle			
							Add			
	Add	Data	Add	Data	Add	Data	A17 - A2	A1	A0	Data/Status
Read Hardwired Protection Status Bit	5555H	AAH	2AAAH	55H	5555H	90H	Don't Care	1	0	Protected: D0 = 1, D7-1=Don't Care Unprotected: D0 = 0, D7-1=Don't Care

Table 3 Hardwired Protection Status Bit Read Command

D0 = "0". The status of the hardwired data protection mode can also be verified by software means. See Table 3 for the command code to access the status bit of the top and bottom sector. The hardwired data protection mode can not be disabled by software means, however.

Noise/Glitch Protection: A WE# or CE# noise glitch of less than 5 ns will not initiate a program or erase cycle.

V_{CC} Power Up/Down Detection: The program or erase operation is inhibited when V_{CC} is less than 3.5V.

Write Inhibit Mode: The program or erase operation is inhibited if any one of the following conditions is enforced: OE# low, CE# high, or WE# high. This prevents inadvertent data alterations during power-up or power-down period.

Product Identification

The product identification mode identifies the device as the IM29F002T/B and the manufacturer as IMT. This mode may be accessed by hardware or software operations. They are typically used by a Flash Memory programmer to identify the IMT IM29F002T/B device and apply the correct algorithm to program the data. See Table 1 for hardware operation or Table 2 for software operation codes. The manufacturer ID for IMT is consisted of two bytes. The first byte is 7F which is located at A0=0 and A1=0. The second byte is 1F, located at A0=1 and A1=1. The device ID is A1, located at A1=0 and A0=1. See Table 4 for manufacturer and device ID designations.

	Byte 1				Byte 2			
	Address			Data	Address			Data
ID Type	A17-2	A1	A0		A17-2	A1	A0	
Manufacturer ID	X	0	0	7FH	X	1	1	1FH
Device ID	X	0	1	A1H/A2H[Note]	Not Applicable			

Note: A1H for IM29F002T and A2H for IM29F002B

Table 4 Product Identification Table

Termination of Product Identification Mode

To return to the standard read mode, the Software Product Identification mode must be terminated. It is accomplished by issuing the Reset/Read operation, which returns the device to the read operation. See Table 2 for the Reset/Read command codes.

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Absolute Maximum Ratings

Storage temperature…….-65°C to +150 °C
Ambient temperature with power applied…….-65°C to +125°C
Voltage with respect to ground
Vcc…….. -0.5 V to 5.5 V
A9 …….. -0.5 V to +12.5 V
All the other pins… -0.5 V to Vcc + 0.5 V

Operating Ranges

Ambient Temperature :
Commercial (C) Devices…0 °C to 70 °C
Industrial (I) Devices……-40 °C to +85 °C
Extended (E) Devices… -55 °C to 125 °C

Vcc Supply Voltages : 4.5 V to 5.5 V

DC Parameters:

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{CC}	Power Supply Current				CE#=OE#=$V_{IL,}$WE#=V_{IH} , all I/Os open,
	Read		40	mA	Address input = V_{IL}/V_{IH}, at f=1/$T_{RC,\ Min.}$, V_{CC}=$V_{CC,\ Max}$
	Write		50	mA	CE#=WE#=$V_{IL,}$ OE#=$V_{IH,}$ V_{CC} = $V_{CC,\ Max}$.
	Standby Power Supply Current				
I_{SB1}	TTL input		2	mA	CE# = $V_{IH,}$ V_{CC} = $V_{CC,\ Max}$.
I_{SB2}	CMOS input		100	µA	CE# = V_{CC} -0.3V, V_{CC} = $V_{CC,\ Max}$.
I_{LI}	Input Leakage Current		1	µA	V_{IN} =GND to V_{CC}, V_{CC} = $V_{CC,\ Max}$.
I_{LO}	Output Leakage Current		10	µA	V_{OUT} =GND to V_{CC} , V_{CC} = $V_{CC,\ Max}$.
V_{IL}	Input Low Voltage		0.8	V	V_{CC} = $V_{CC,\ Max}$.
V_{IH}	Input High Voltage	2.0		V	V_{CC} = $V_{CC,\ Max}$.
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.1 mA, V_{CC} = $V_{CC,\ Min}$.
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -400µA, V_{CC} = $V_{CC,\ Min}$.
V_H	High voltage input for Product ID and Hardwired Data Protection modes	11.5	12.5	V	CE# = OE# =V_{IL}, WE# = V_{IH}
I_H	High voltage input for Product ID and Hardwired Data Protection modes		50	µA	CE# = OE# = V_{IL}, WE# = V_{IH}, A_9 = $V_{H,\ Max}$.

AC Parameters:

a) Read Characteristics:

Parameter	Description	IM29F002-45		IM29F002-70		IM29F002-90		IM29F002-120		
		Min	Max	Min	Max	Min	Max	Min	Max	Unit
t_{RC}	Read cycle time	45		70		90		120		ns
t_{AA}	Address to output delay		45		70		90		120	ns
t_{CE}	CE# to output delay		45		70		90		120	ns
t_{OE}	OE# to output delay		25		35		45		60	ns
t_{CLZ}	CE# low to output active	0		0		0		0		ns
t_{OLZ}	OE# low to output active	0		0		0		0		ns
t_{CHZ}	CE# high to output at high-Z		20		30		40		50	ns
t_{OHZ}	OE# high to output at high-Z		20		30		40		50	ns
t_{OH}	Output hold from address change	0		0		0		0		ns

b) Write Characteristics:

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Parameter	Description	IM29F002-45		IM29F002-70		IM29F002-90		IM29F002-120		
		Min	Max	Min	Max	Min	Max	Min	Max	**Unit**
t_{WC}	Write command cycle time	45		70		90		120		ns
t_{AS}	Address setup time	0		0		0		0		ns
t_{AH}	Address hold time	35		45		55		60		ns
t_{DS}	Data setup time	20		30		40		45		ns
t_{DH}	Data hold time	0		0		0		0		ns
t_{OES}	OE# setup time	0		0		0		0		ns
t_{OEH}	OE# hold time	0		0		0		0		ns
t_{CS}	CE# setup time	0		0		0		0		ns
t_{CH}	CE# hold time	0		0		0		0		ns
t_{CP}	CE# write pulse width	25		35		45		50		ns
t_{CPH}	CE# write pulse width high	20		30		30		35		ns
t_{WS}	WE# setup time	0		0		0		0		ns
t_{WH}	WE# hold time	0		0		0		0		ns
t_{WP}	WE# write pulse width	25		35		45		50		ns
t_{WPH}	WE# write pulse width high	20		30		30		35		ns
t_{WHWH1}	Byte programming time		30		30		30		30	µs
t_{WHWH2}	Page erase time		9		9		9		9	ms
t_{WHWH3}	Chip erase time		3		3		3		3	s
t_{CEP}	CE# access time for Data# Polling and Toggle bit read		45		70		90		120	ns
t_{OEP}	OE# access time for Data# Polling and Toggle bit read		25		35		45		60	ns

Test Conditions

Input rise and fall time …….. 5 ns
Input pulse levels…….. 0.0 V to 5.0 V
Timing measurement reference level
Input…….. 1.5 V
Output…….. 1.5 V
Output loading
45ns and 70 ns parts…….. 1 TTL load + 30 pF
90 ns and 120 ns parts…….. 1 TTL load + 100 pF

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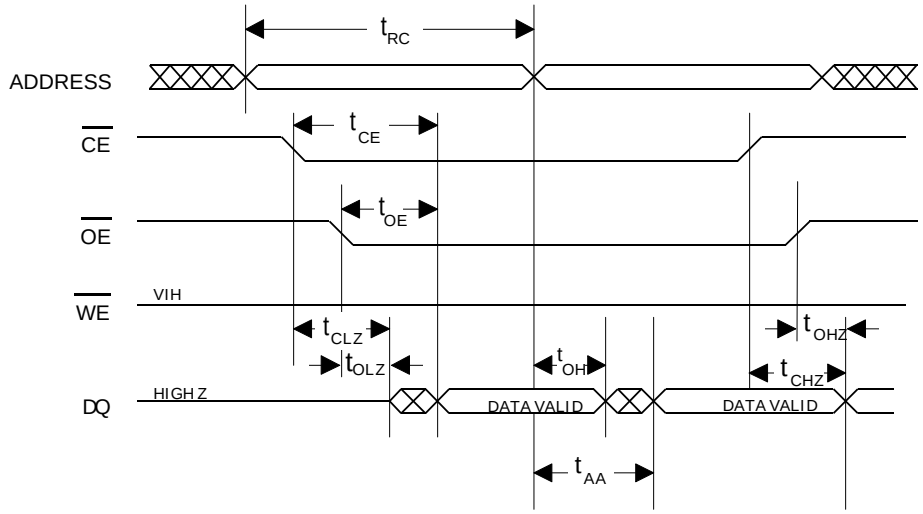

Fig. 1 Read Cycle Timing Diagram

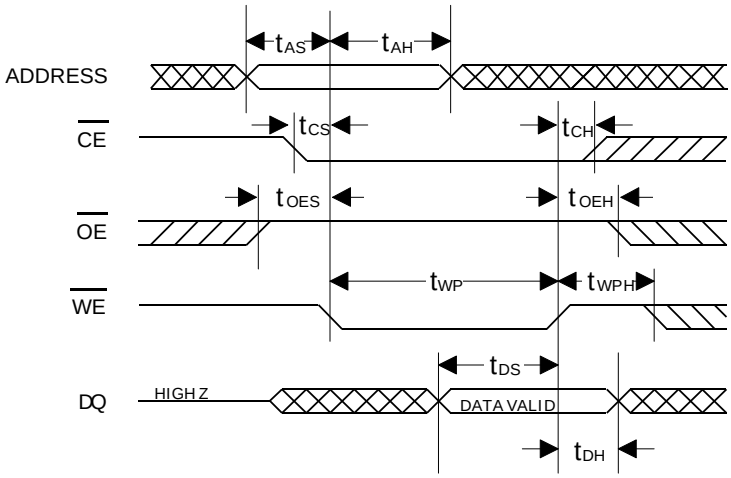

Fig. 2 $\overline{WE}$ Controlled Command Write Timing Diagram

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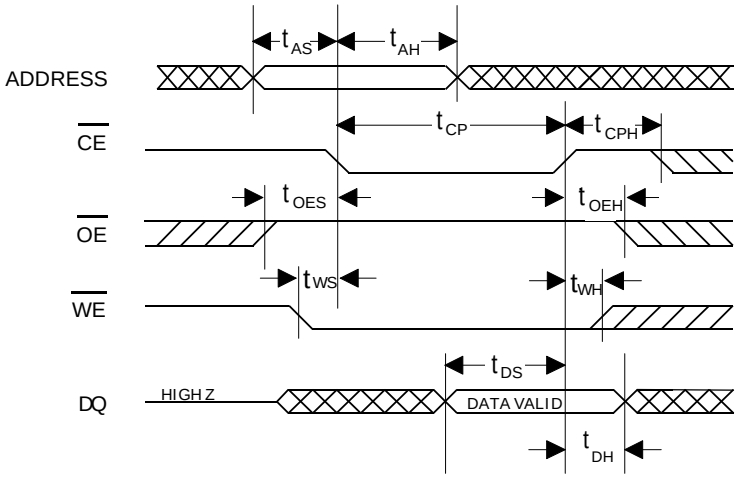

Fig. 3 $\overline{CE}$ Controlled Command Write Timing Diagram

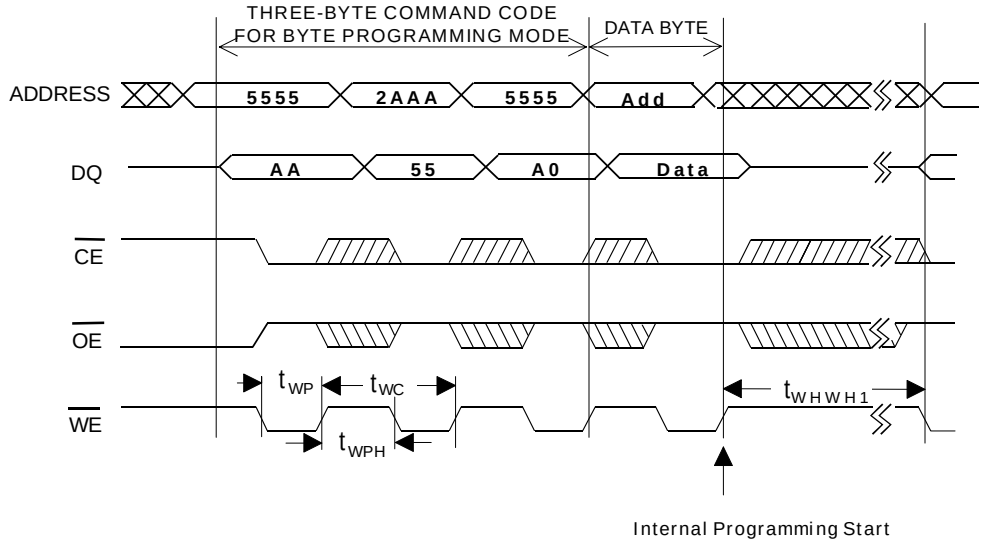

Fig. 4 Byte Programming Mode Timing Diagram

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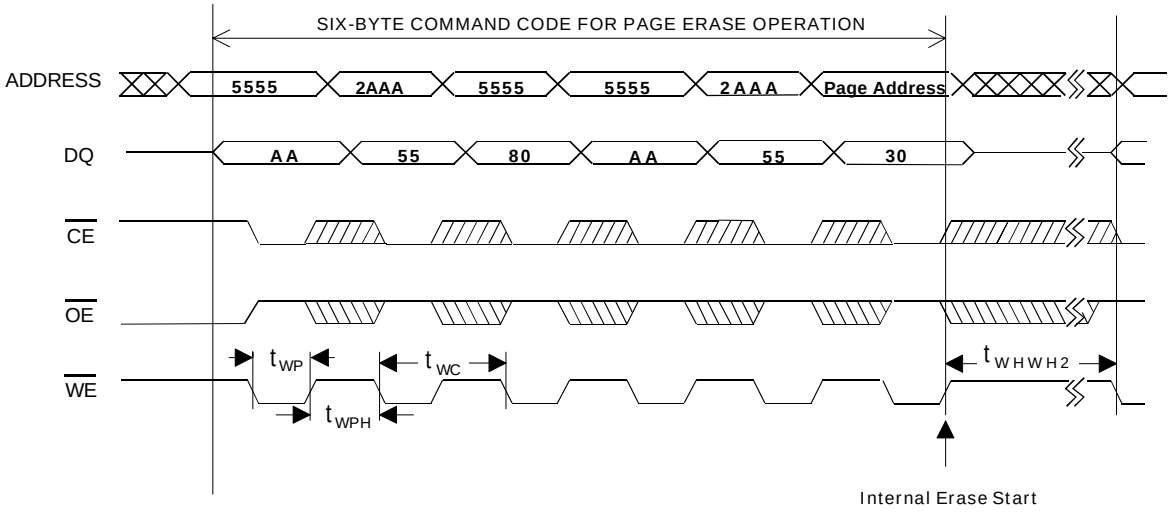

Fig. 5 Page Erase Timing Diagram

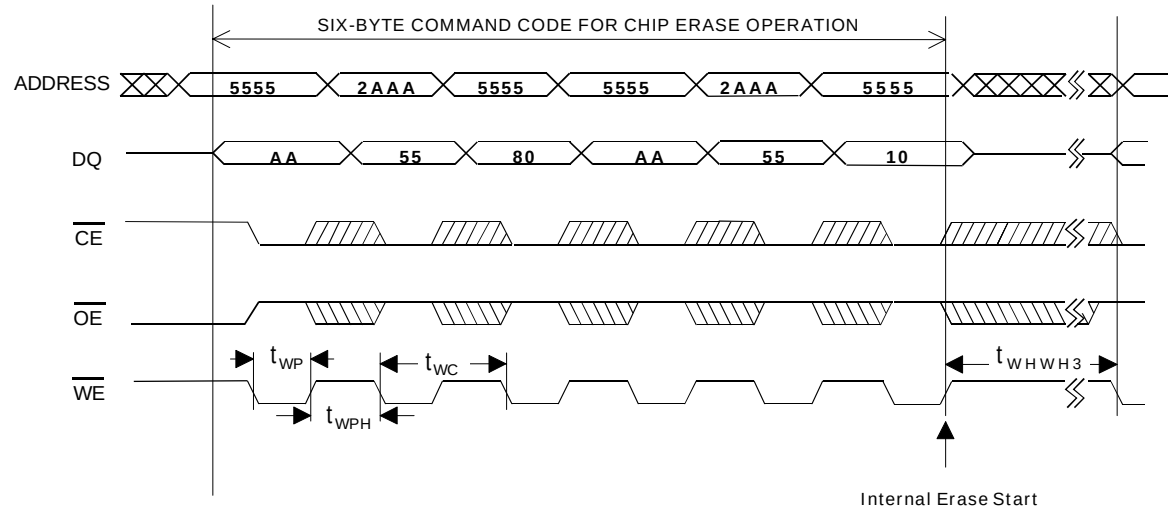

Fig. 6 Chip Erase Timing Diagram

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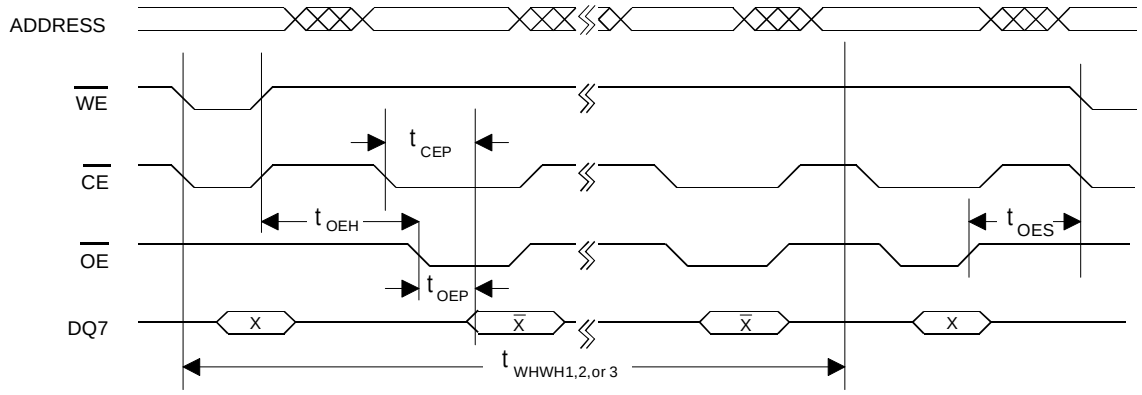

Fig. 7 $\overline{\text{Data}}$ Polling Timing Diagram

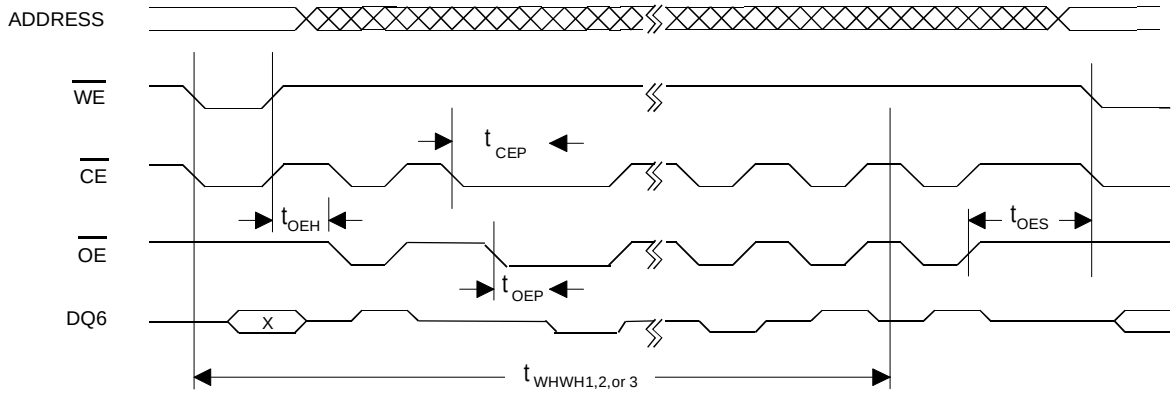

Fig. 8 Toggle Bit Timing Diagram

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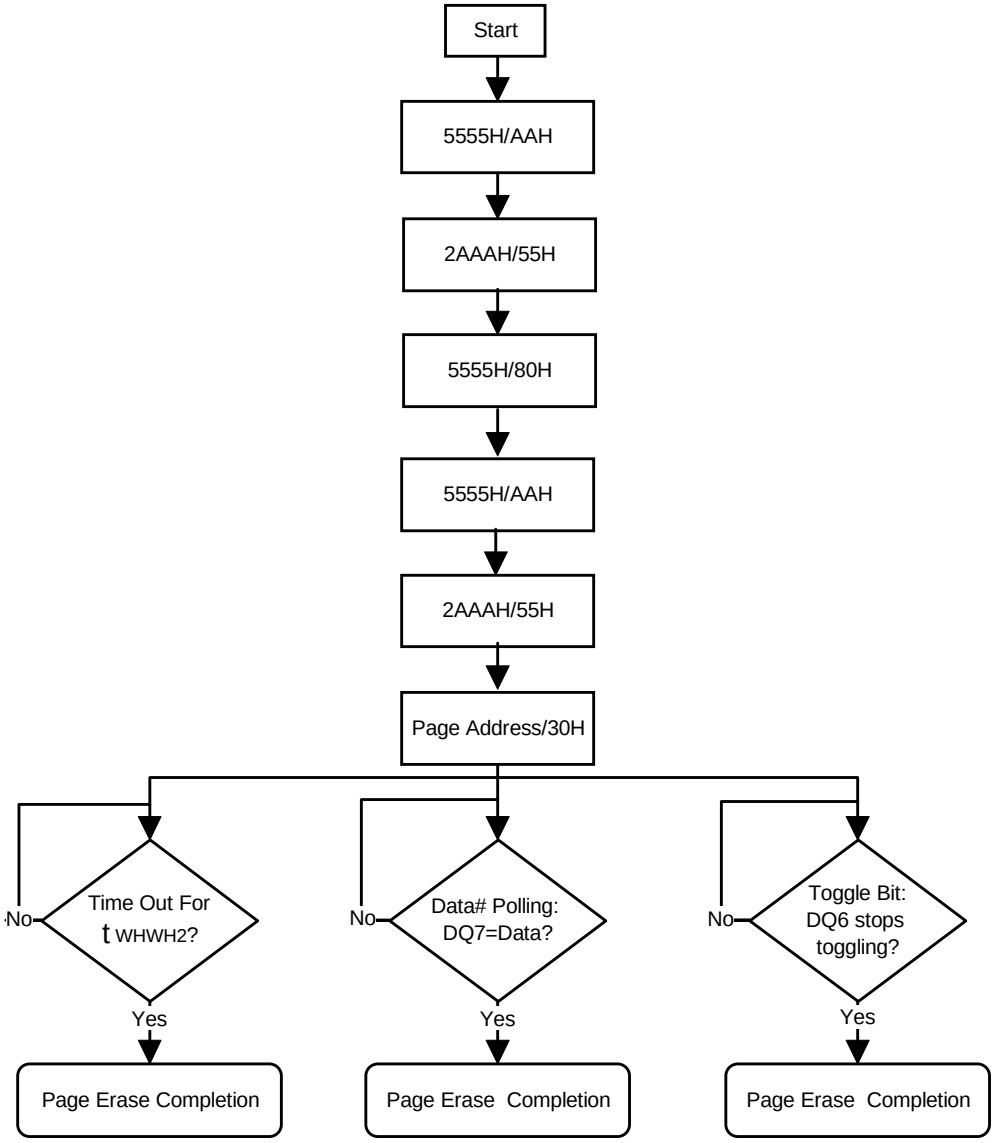

Fig. 9 Page Erase Flow Chart

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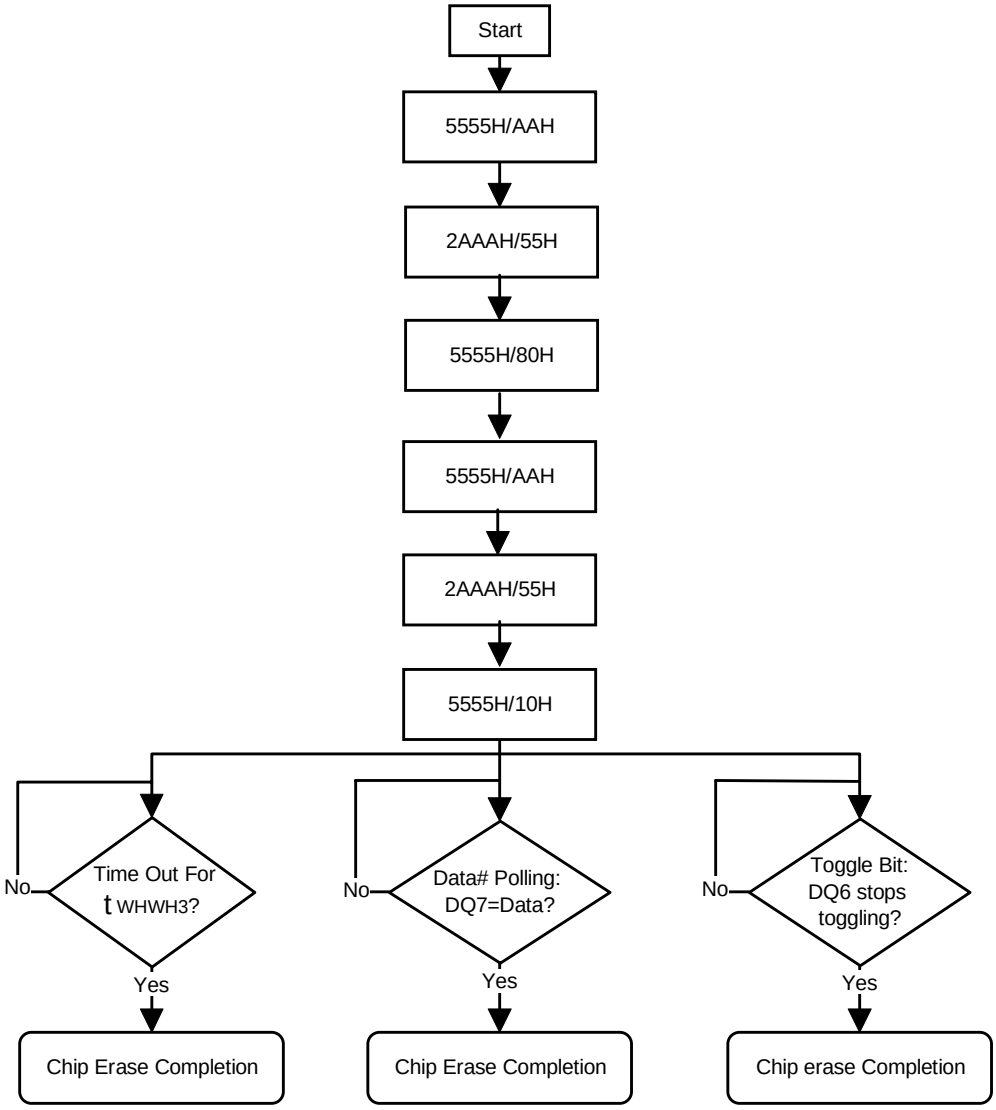

Fig. 10 Chip Erase Flow Chart

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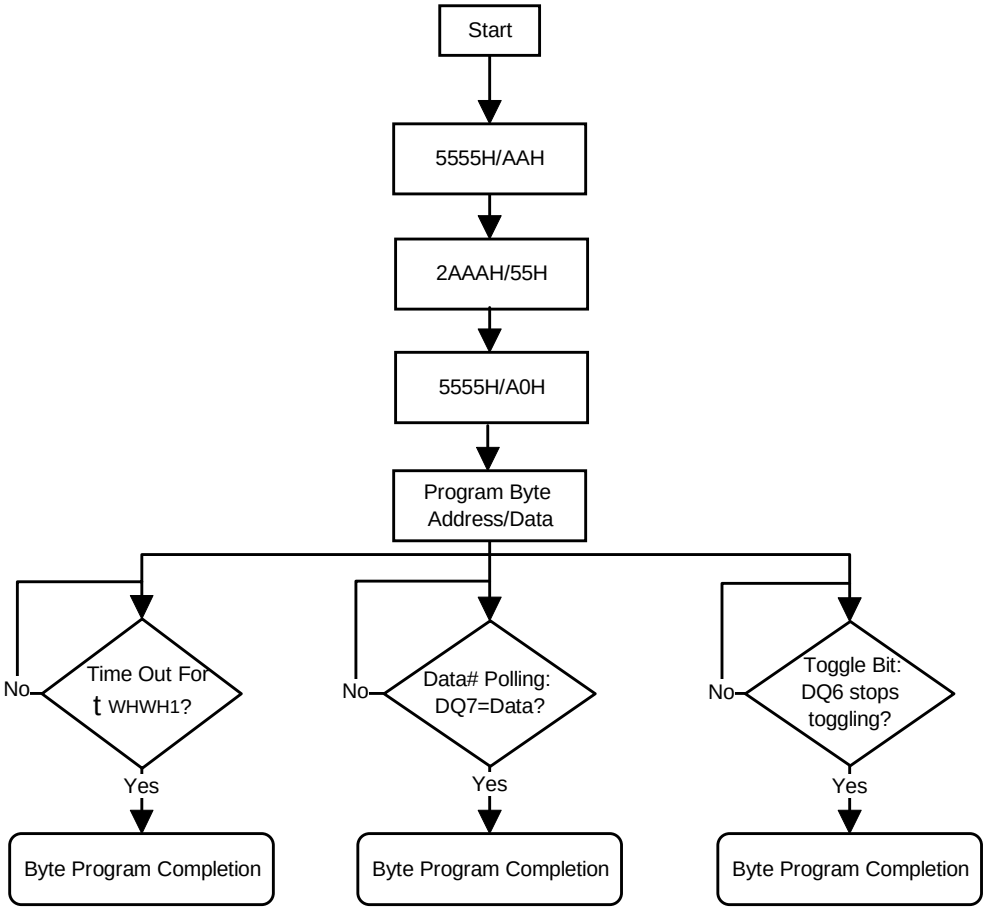

Fig. 11 Byte Program Flow Chart

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