



### GENERAL DESCRIPTION

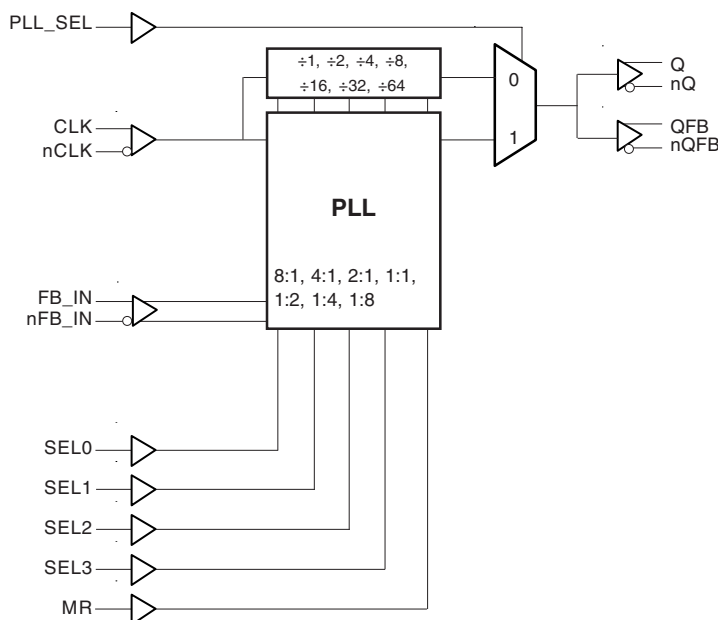


The ICS8735-21 is a highly versatile 1:1 Differential-to-3.3V LVPECL clock generator and a member of the HiPerClock<sup>STM</sup> family of High Performance Clock Solutions from ICS. The CLK, nCLK pair can accept most standard differential input levels. The ICS8735-21 has a fully integrated PLL and can be configured as zero delay buffer, multiplier or divider, and has an output frequency range of 31.25MHz to 700MHz. The reference divider, feedback divider and output divider are each programmable, thereby allowing for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL\_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output dividers.

### FEATURES

- 1 differential 3.3V LVPECL output pair, 1 differential feedback output pair
- Differential CLK, nCLK input pair
- CLK, nCLK pair can accept the following differential input levels: LVDS, LVPECL, LVHSTL, SSTL, HCSL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- Programmable dividers allow for the following output-to-input frequency ratios: 8:1, 4:1, 2:1, 1:1, 1:2, 1:4, 1:8
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Cycle-to-cycle jitter: 25ps (maximum)
- Static phase offset: 50ps ± 100ps
- 3.3V supply voltage
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request

### BLOCK DIAGRAM



### PIN ASSIGNMENT

CLK	1	20	nc
nCLK	2	19	SEL1
MR	3	18	SEL0
V <sub>CC</sub>	4	17	V <sub>CC</sub>
nFB_IN	5	16	PLL_SEL
FB_IN	6	15	V <sub>CCA</sub>
SEL2	7	14	SEL3
V <sub>EE</sub>	8	13	V <sub>CCO</sub>
nQFB	9	12	Q
QFB	10	11	nQ

### ICS8735-21

**20-Lead, 300-MIL SOIC**  
7.5mm x 12.8mm x 2.3mm body package  
**M Package**  
Top View



**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	CLK	Input	Pulldown	Non-inverting differential clock input.
2	nCLK	Input	Pullup	Inverting differential clock input.
3	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted outputs nQ to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
4, 17	V <sub>CC</sub>	Power		Core supply pins.
5	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay". Connect to pin 9.
6	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay". Connect to pin 10.
7	SEL2	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
8	V <sub>EE</sub>	Power		Negative supply pin.
9, 10	nQFB, QFB	Output		Differential feedback outputs. LVPECL interface levels.
11, 12	nQ, Q	Output		Differential clock outputs. LVPECL interface levels.
13	V <sub>CCO</sub>	Power		Output supply pin.
14	SEL3	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
15	V <sub>CCA</sub>	Power		Analog supply pin.
16	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as the input to the dividers. When LOW, selects reference clock. When HIGH, selects PLL. LVCMOS / LVTTTL interface levels.
18	SEL0	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
19	SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
20	nc	Unused		No connect.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		KΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		KΩ



**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs					Outputs PLL_SEL = 1 PLL Enable Mode
SEL3	SEL2	SEL1	SEL0	Reference Frequency Range (MHz)*	Q, nQ; QFB, nQFB
0	0	0	0	250 - 700	÷ 1
0	0	0	1	125 - 350	÷ 1
0	0	1	0	62.5 - 175	÷ 1
0	0	1	1	31.25 - 87.5	÷ 1
0	1	0	0	250 - 700	÷ 2
0	1	0	1	125 - 350	÷ 2
0	1	1	0	62.5 - 175	÷ 2
0	1	1	1	250 - 700	÷ 4
1	0	0	0	125 - 350	÷ 4
1	0	0	1	250 - 700	÷ 8
1	0	1	0	125 - 350	x 2
1	0	1	1	62.5 - 175	x 2
1	1	0	0	31.25 - 87.5	x 2
1	1	0	1	62.5 - 175	x 4
1	1	1	0	31.25 - 87.5	x 4
1	1	1	1	31.25 - 87.5	x 8

\*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.

**TABLE 3B. PLL BYPASS FUNCTION TABLE**

Inputs				Outputs PLL_SEL = 0 PLL Bypass Mode
SEL3	SEL2	SEL1	SEL0	Q, nQ; QFB, nQFB
0	0	0	0	÷ 4
0	0	0	1	÷ 4
0	0	1	0	÷ 4
0	0	1	1	÷ 8
0	1	0	0	÷ 8
0	1	0	1	÷ 8
0	1	1	0	÷ 16
0	1	1	1	÷ 16
1	0	0	0	÷ 32
1	0	0	1	÷ 64
1	0	1	0	÷ 2
1	0	1	1	÷ 2
1	1	0	0	÷ 4
1	1	0	1	÷ 1
1	1	1	0	÷ 2
1	1	1	1	÷ 1



### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_i$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	46.2°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				150	mA
$I_{CCA}$	Analog Supply Current				15	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	SEL0, SEL1, SEL2, SEL3, MR	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	SEL0, SEL1, SEL2, SEL3, MR	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK, FB_IN	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK, nFB_IN	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK, FB_IN	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nCLK, nFB_IN	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: Common mode voltage is defined as  $V_{IH}$ .

NOTE 2: For single ended applications, the maximum input voltage for CLK, nCLK is  $V_{CC} + 0.3V$ .



**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 1.0$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		0.9	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 5. INPUT FREQUENCY CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	CLK, nCLK	PLL_SEL = 1	31.25		700	MHz
			PLL_SEL = 0			700	MHz

**TABLE 6. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f \leq 700MHz$	3.0		4.2	ns
tsk(o)	Output Skew; NOTE 4, 5	PLL_SEL = 0V			20	ps
$t(\emptyset)$	Static Phase Offset; NOTE 2, 5	PLL_SEL = 3.3V	-50	50	150	ps
$f_{jit}(cc)$	Cycle-to-Cycle Jitter; NOTE 5, 6				25	ps
$f_{jit}(\theta)$	Phase Jitter; NOTE 3, 5, 6				$\pm 50$	ps
$t_L$	PLL Lock Time				1	ms
$t_R$	Output Rise Time	20% to 80% @ 50MHz	300		700	ps
$t_F$	Output Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal, when the PLL is locked and the input reference frequency is stable.

NOTE 3: Phase jitter is dependent on the input source used.

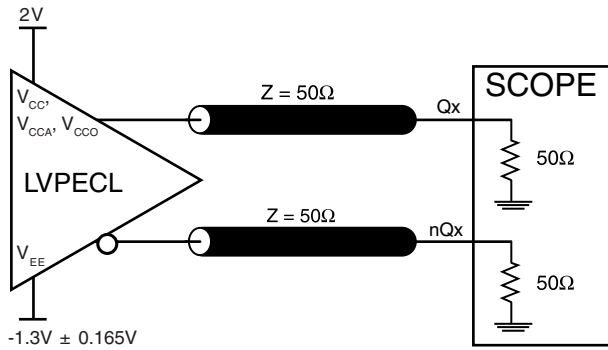
NOTE 4: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential crosspoints.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

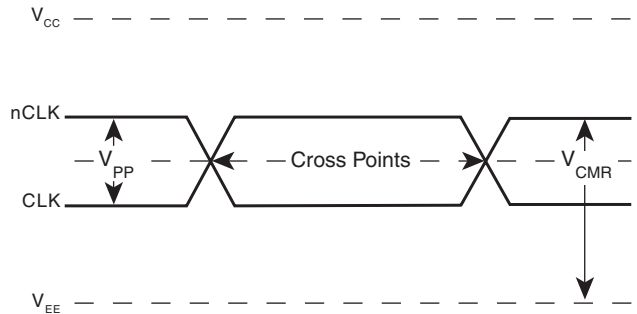
NOTE 6: Characterized at VCO frequency of 622MHz.



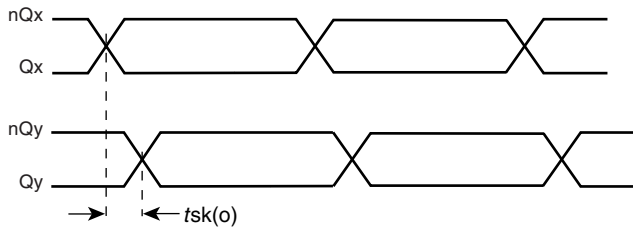
## PARAMETER MEASUREMENT INFORMATION



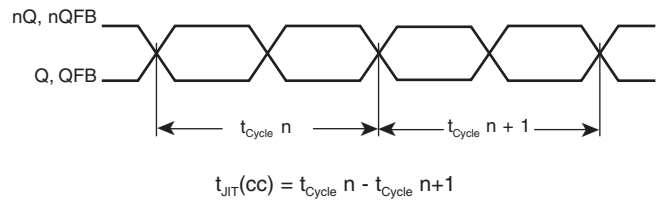
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



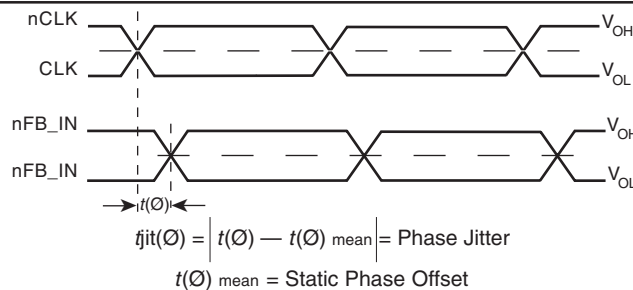
**DIFFERENTIAL INPUT LEVEL**



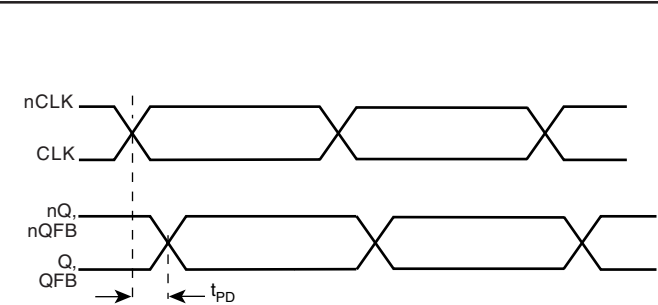
**OUTPUT SKEW**



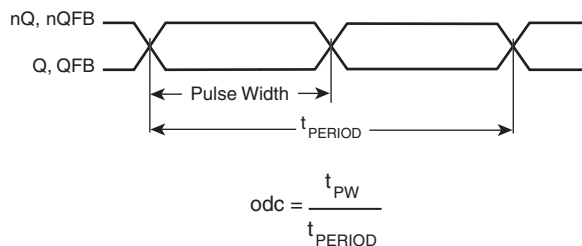
**CYCLE-TO-CYCLE JITTER**



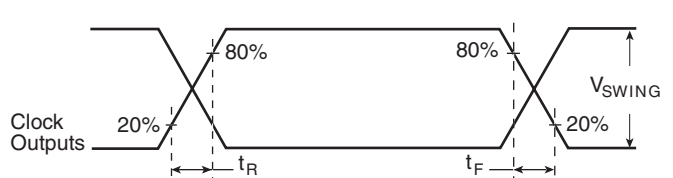
**PHASE JITTER AND STATIC PHASE OFFSET**



**PROPAGATION DELAY**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**OUTPUT RISE/FALL TIME**



## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8735-21 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ , and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu\text{F}$  and a  $.01\mu\text{F}$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

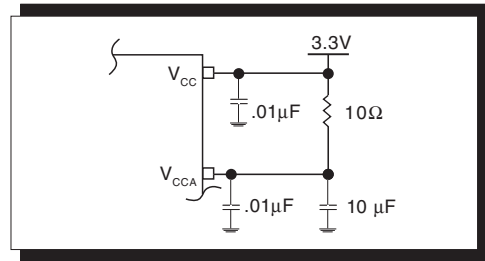


FIGURE 1. POWER SUPPLY FILTERING

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} \approx V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3\text{V}$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .

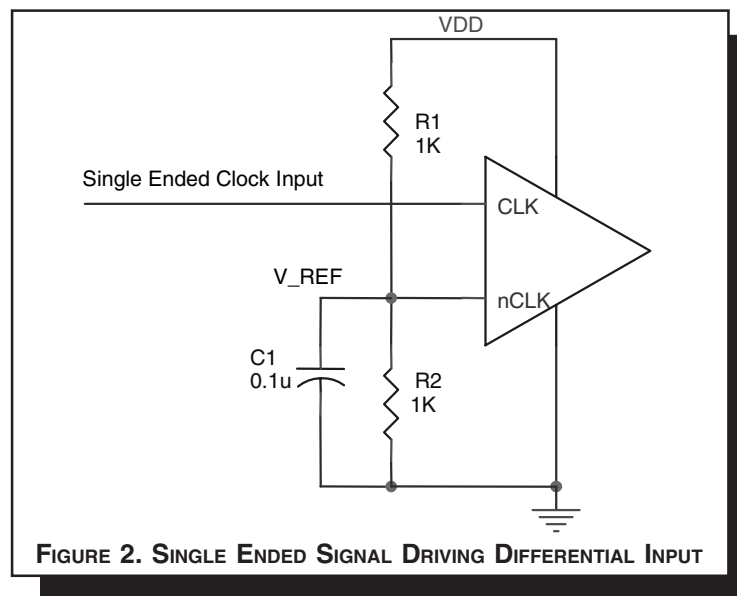


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT



### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

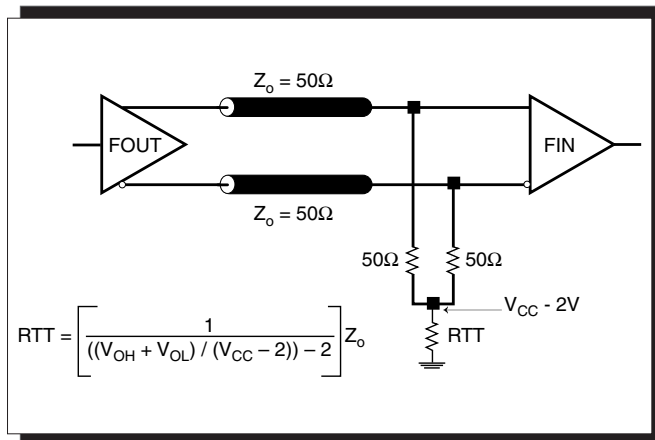


FIGURE 3A. LVPECL OUTPUT TERMINATION

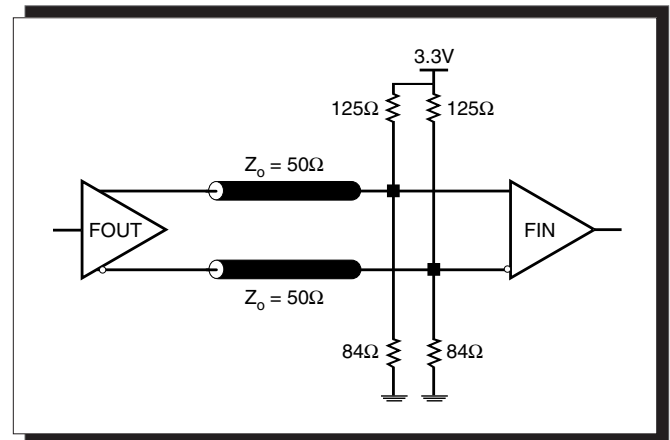


FIGURE 3B. LVPECL OUTPUT TERMINATION

### SCHEMATIC EXAMPLE

Figure 4 shows a schematic example of the ICS8735-21. In this example, the input is driven by an HCSL driver. The zero delay buffer is configured to operate at 155.52MHz input and 77.75MHz output. The logic control pins are configured as follows:

SEL [3:0] = 0101; PLL\_SEL = 1

The decoupling capacitors should be physically located near the power pin. For ICS8735-21.

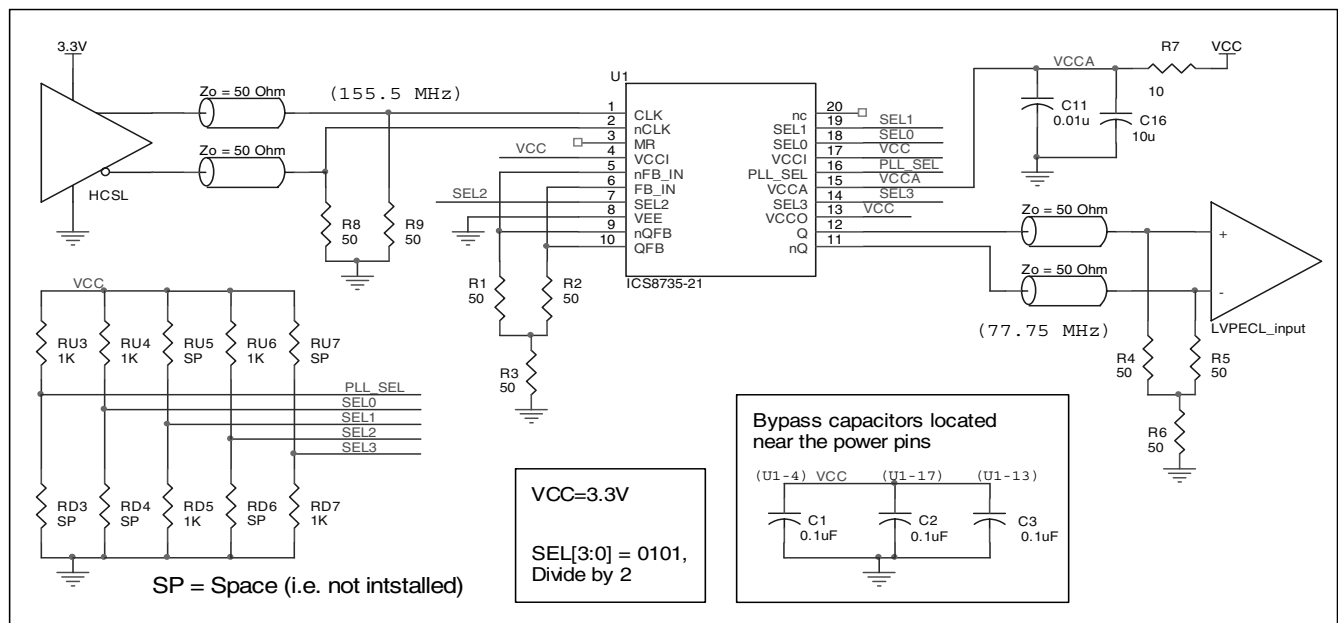


FIGURE 4. ICS8735-21 LVPECL BUFFER SCHEMATIC EXAMPLE

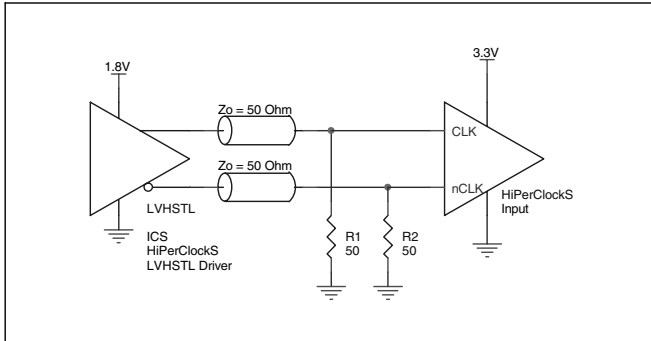




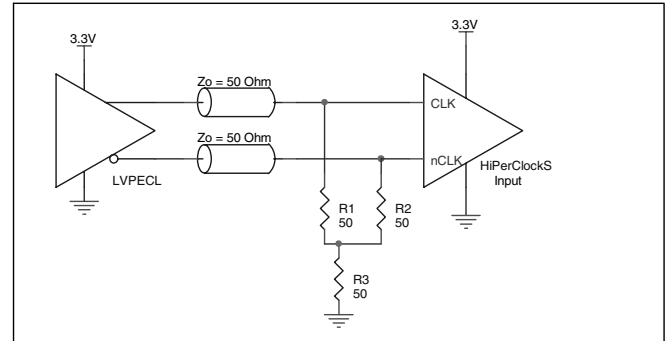
### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 5A to 5D show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested

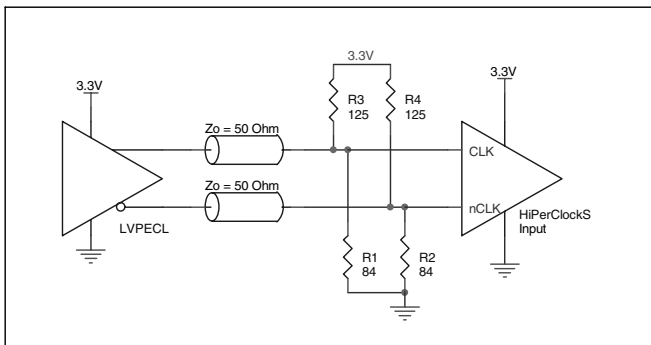
here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 4A*, the input termination applies for ICS HiPerClockS LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



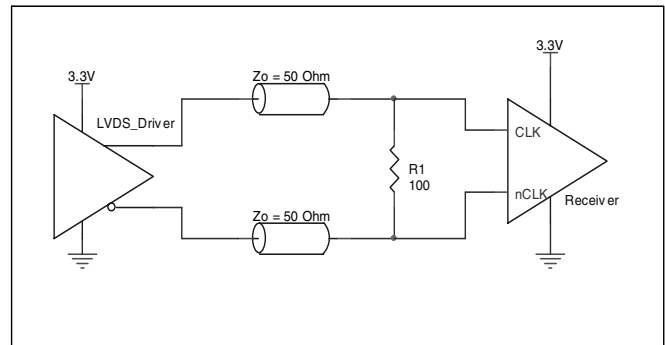
**FIGURE 5A. HiPerClockS CLK/nCLK INPUT DRIVEN BY ICS HiPerClockS LVHSTL DRIVER**



**FIGURE 5B. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 5C. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 5D. HiPerClockS CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8735-21. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8735-21 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 150mA = 519.8mW$
- Power (outputs)<sub>MAX</sub> = **30.2mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $2 * 30.2mW = 60.4mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 519.8mW + 60.4mW = 580.2mW$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd\_total$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ C + 0.580W * 39.7^\circ C/W = 93^\circ C. \text{ This is well below the limit of } 125^\circ C.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 20-PIN SOIC, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

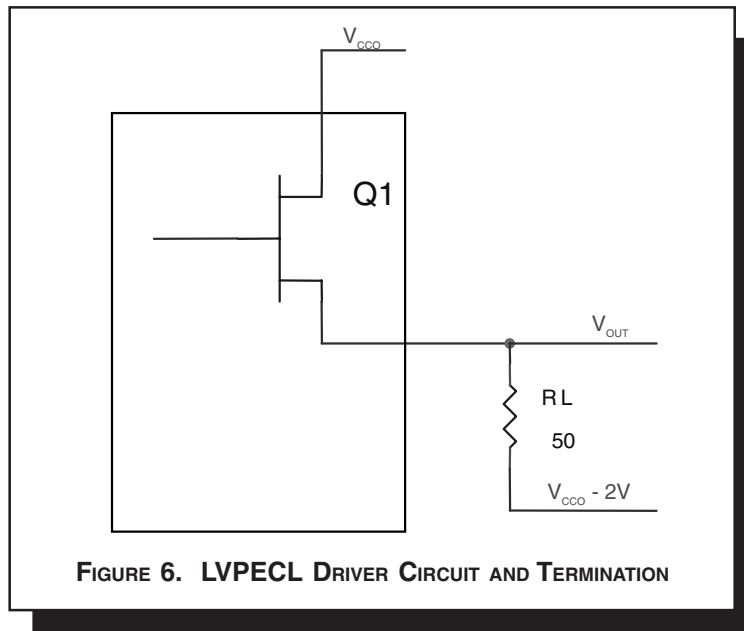
**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.



### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6*.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 1.0V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 1.0V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.

$Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 1V)/50\Omega] * 1V = \mathbf{20.0mW}$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = \mathbf{10.2mW}$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = \mathbf{30.2mW}$



## RELIABILITY INFORMATION

**TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 20 LEAD SOIC**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	<b>0</b>	<b>200</b>	<b>500</b>
Single-Layer PCB, JEDEC Standard Test Boards	83.2°C/W	65.7°C/W	57.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

**NOTE:** Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

### TRANSISTOR COUNT

The transistor count for ICS8735-21 is: 2969



PACKAGE OUTLINE - M SUFFIX FOR 20 LEAD SOIC

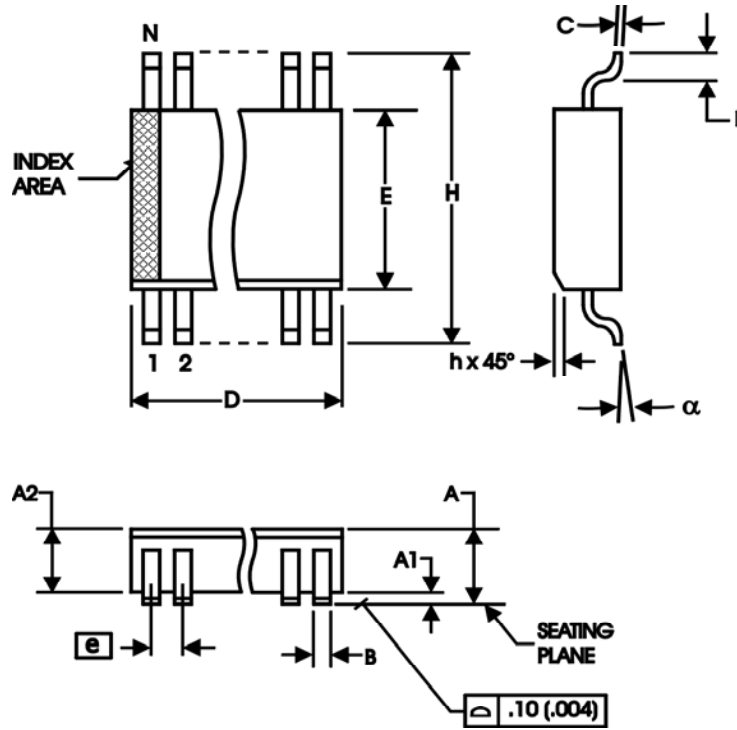


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	20	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	12.60	13.00
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119



Integrated  
Circuit  
Systems, Inc.

# ICS8735-21

700MHz, DIFFERENTIAL-TO-3.3V LVPECL  
ZERO DELAY CLOCK GENERATOR

**TABLE 10. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Count	Temperature
ICS8735AM-21	ICS8735AM-21	20 Lead SOIC	38 per tube	0°C to 70°C
ICS8735AM-21T	ICS8735AM-21	20 Lead SOIC on Tape and Reel	1000	0°C to 70°C

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T6	1	Revised Block Diagram.	10/31/01
		5	Added Output Skew row at 20ps Max.	
		5	Relabeled PLL Reference Zero Delay to Static Phase Offset.	
B	T3A T6	7	Added Output Skew Diagram.	11/20/01
		3	Added note at bottom of the table.	
B		5	Added Note 6.	
B		10	Added Termination for LVPECL Outputs section	6/3/02
B	T2	2	Pin Description Table - revised MR description.	8/19/02
		6	3.3V Output Load Test Circuit Diagram, revised VEE equation from "-1.3V ± 0.135V" to "-1.3V ± 0.165V".	
		8	Revised Output Rise/Fall Time Diagram.	
B		8 - 9	Added Schematic Example section	10/17/02
B	T1 T4A	2	Pin Description table - revised MR and V <sub>CC</sub> descriptions.	2/03/03
		4	Power Supply table - revised V <sub>CC</sub> Parameter to correspond with pin description.	
		9	Deleted Figure 8, "Clock Input Driven by LVPECL Driver w/AC Couple". AC Couple is not recommended for Zero Delay Buffers.	
C	T2	2	Pin Characteristics Table - changed CIN from 4pF max. to 4pF typical.	10/13/03
		4	Absolute Maximum Ratings - revised Output rating.	
		7	Updated Single Ended Signal Driving Differential Input Diagram.	
		8	Updated LVPECL Output Termination Diagrams.	
		8	Updated Schematic Example.	
D	T6	9	Updated Differential Clock Input Interface drawings.	10/27/03
		5	AC Characteristics Table - modified tPD min. limit from 3.6ns to 3.0ns and deleted the typical value.	