I90188-PCI/Utopia Interface Chip

Features

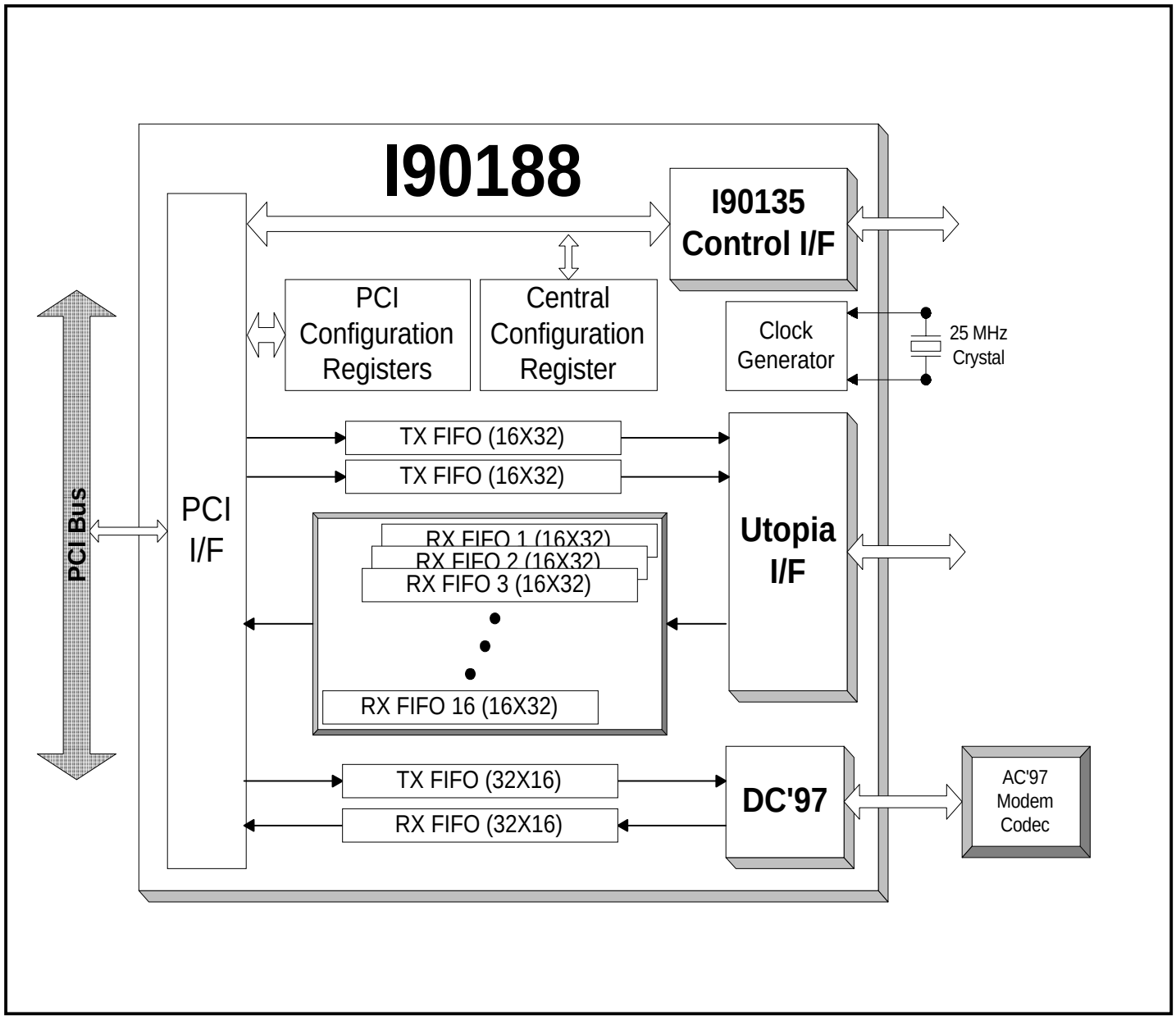
- PCI Interface
  - Compliant with PCI Specification v2.2
  - 32-bit address/data bus
  - Bus frequency up to 33 MHz
  - Supports PCI master/slave device
  - Supports +3.3V or +5V PCI interface
- Utopia Interface
  - Utopia level 1 and 2 support for D0 and D3 hot
  - 8-bit data path
  - Full duplex
  - Cell-based-only
- Supports T1.413 issue 2, ITU-T G.992.1 (G.dmt), and G.992.2 (G.lite) full rate speed
- ITeX I90135 interface
- AC'97 Digital Controller
  - Compliant with AC'97 Component Specification R2.1
  - Provides standard AC97-link interface for AC'97 modem codec
  - Supports multiple sample rates
  - Eight general purpose I/O pins
  - Can be individually enabled or disabled via software configuration registers
  - Can be individually set as input or output via software configuration registers
- +3.3V & +5V Power Supply
- Package: 160-pin PQFP

General Description

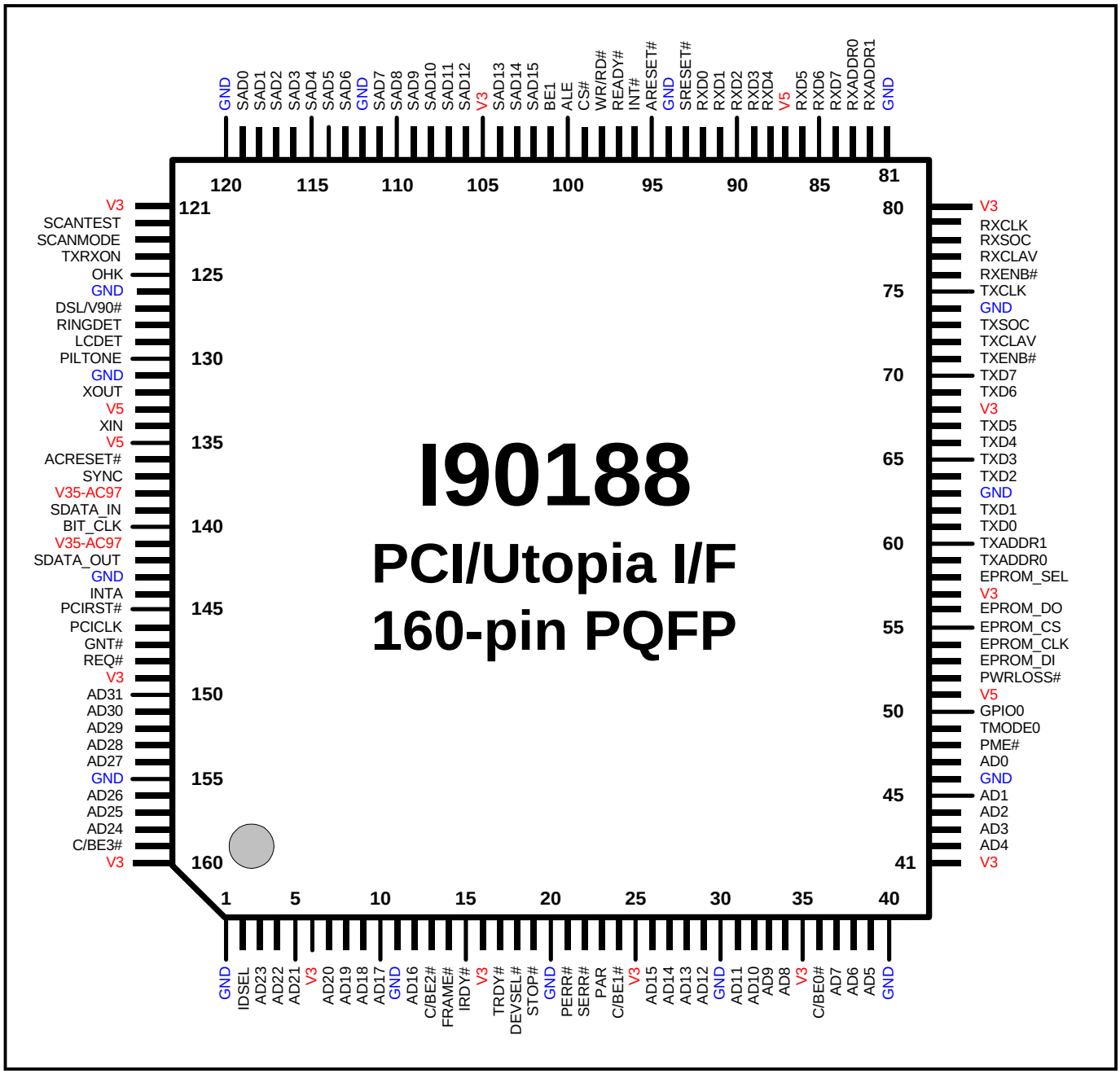
The I90188 is a PCI to the Utopia interface and an AC97-link digital bridge device. The I90188 has an 8-bit full duplex cell-based-only Utopia interface that connects to an ADSL controller. The AC'97 digital controller provides an Intel AC'97 v2.1 standard AC-link interface. The device's 32-bit PCI interface supports PCI slave/master devices, and is PCI specification v.2.2 compliant.

The I90188 requires a single 25 MHz clock frequency input and supports a 3.3V power supply. The I90188 is available in a 160-pin PQFP.

Block Diagram



Pin Diagram


I90188
PCI/Utopia I/F
160-pin PQFP
GND SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 GND SAD7 SAD8 SAD9 SAD10 SAD11 SAD12 V3 SAD13 SAD14 SAD15 BE1 ALE CS# WR/RD# READY# INT# ARESET# GND SRESET# RXD0 RXD1 RXD2 RXD3 RXD4 V5 RXD5 RXD6 RXD7 RXADDR0 RXADDR1 GND
120 115 110 105 100 95 90 85 81
121 125 130 135 140 145 150 155 160
80 75 70 65 60 55 50 45 41
V3 SCANTEST SCANMODE TXRXON OHK GND DSL/V90# RINGDET LCDET PILTONE GND XOUT V5 XIN V5 ACRESET# SYNC V35-AC97 SDATA_IN BIT_CLK V35-AC97 SDATA_OUT GND INTA PCIRST# PCICLK GNT# REQ# V3 AD31 AD30 AD29 AD28 AD27 GND AD26 AD25 AD24 C/BE3# V3
V3 RXCLK RXSOC RXCLAV RXENB# TXCLK GND TXSOC TXCLAV TXENB# TXD7 TXD6 V3 TXD5 TXD4 TXD3 TXD2 GND TXD1 TXD0 TXADDR1 TXADDR0 EPROM_SEL V3 EPROM_DO EPROM_CS EPROM_CLK EPROM_DI PWRLOSS# V5 GPIO0 TMODE0 PME# AD0 GND AD1 AD2 AD3 AD4 V3
1 5 10 15 20 25 30 35 40
GND IDSEL AD23 AD22 AD21 V3 AD20 AD19 AD18 AD17 GND AD16 C/BE2# FRAME# IRDY# V3 TRDY# DEVSEL# STOP# GND PERR# SERR# PAR C/BE1# V3 AD15 AD14 AD13 AD12 GND AD11 AD10 AD9 AD8 V3 C/BE0# AD7 AD6 AD5 GND

Pinout Table

Pin	Signal
1	GND
2	IDSEL
3	AD23
4	AD22
5	AD21
6	V3
7	AD20
8	AD19
9	AD18
10	AD17
11	GND
12	AD16
13	C/BE2#
14	FRAME#
15	IRDY#
16	V3
17	TRDY#
18	DEVSEL#
19	STOP#
20	GND
21	PERR#
22	SERR#
23	PAR
24	C/BE1#
25	V3
26	AD15
27	AD14
28	AD13
29	AD12
30	GND
31	AD11
32	AD10
33	AD9
34	AD8
35	V3
36	C/BE0#
37	AD7
38	AD6
39	AD5
40	GND

Pin	Signal
41	V3
42	AD4
43	AD3
44	AD2
45	AD1
46	GND
47	AD0
48	PME#
49	TMODE0
50	GPIO0
51	V5
52	PWRLOSS#
53	EPROM_DI
54	EPROM_CLK
55	EPROM_CS
56	EPROM_DO
57	V3
58	EPROM_SEL
59	TXADDR0
60	TXADDR1
61	TXD0
62	TXD1
63	GND
64	TXD2
65	TXD3
66	TXD4
67	TXD5
68	V3
69	TXD6
70	TXD7
71	TXENB#
72	TXCLAV
73	TXSOC
74	GND
75	TXCLK
76	RXENB#
77	RXCLAV
78	RXSOC
79	RXCLK
80	V3

Pin	Signal
81	GND
82	RXADDR1
83	RXADDR0
84	RXD7
85	RXD6
86	RXD5
87	V5
88	RXD4
89	RXD3
90	RXD2
91	RXD1
92	RXD0
93	SRESET#
94	GND
95	ARESET#
96	INT#
97	READY#
98	WR/RD#
99	CS#
100	ALE
101	BE1
102	SAD15
103	SAD14
104	SAD13
105	V3
106	SAD12
107	SAD11
108	SAD10
109	SAD9
110	SAD8
111	SAD7
112	GND
113	SAD6
114	SAD5
115	SAD4
116	SAD3
117	SAD2
118	SAD1
119	SAD0
120	GND

Pin	Signal
121	V3
122	SCANTEST
123	SCANMODE
124	TXRXON
125	OHK
126	GND
127	DSL/V90#
128	RINGDET
129	LCDET
130	PILTONE
131	GND
132	XOUT
133	V5
134	XIN
135	V5
136	ACRESET#
137	SYNC
138	V35-AC97
139	SDATA_IN
140	BIT_CLK
141	V35-AC97
142	SDATA_OUT
143	GND
144	INTA
145	PCIRST#
146	PCICLK
147	GNT#
148	REQ#
149	V3
150	AD31
151	AD30
152	AD29
153	AD28
154	AD27
155	GND
156	AD26
157	AD25
158	AD24
159	C/BE3#
160	V3

Pin Description

Symbol	Pin #	Type	Description
POWER SUPPLIES			
V3	6, 16, 25, 35, 41, 57, 68, 80, 105, 121, 149, 160	PWR	***+3.3V OR +5V Power Supply for PCI bus, I90135 and Utopia Interface.***
V35-AC97	138, 141	PWR	***+3.3V OR +5V Power Supply for AC'97 (AC-LINK) Interface***
V5	51, 87, 133, 135	PWR	***+5V Power Supply for PUB core.***
GND	1, 11, 20, 30, 40, 46, 63, 74, 81, 94, 112, 120, 126, 131, 143, 155	GND	***Ground.***
PCI BUS INTERFACE SIGNALS			
AD[31:0]	150 - 154, 156 - 158, 3 - 5, 7 - 10, 12, 26 - 29, 31 - 34, 37 - 39, 42 - 45, 47.	DI/O	***PCI Multiplexed Address / Data 31 - 0.*** 32-bit bi-directional address/data multiplexed lines AD31 is the MSB and AD0 is the LSB. The direction of these pins are defined below: ***PHASE*** / ***Bus Master*** / ***Target*** Address Phase / Output / Input Read Data Phase / Input / Output Write Data Phase / Output / Input
C/BE[3:0]#	159, 13, 24, 36	DI/O	***Command/Byte Enable 3 - 0 #.*** Multiplexed bus command and byte enables.
DEVSEL#	18	DI/O	***Device Select*** #. When driven active low, the signal indicates the driving device has decoded its address as the target of the current access. This pin acts as an output pin when the I90188 (including ISA slave) is the slave of PCI bus cycle transaction. Otherwise, it is an input pin.
TRDY#	17	DI/O	***Target Ready #.*** This signal indicates that the target of the current data phase of the transaction is ready to be completed. This pin acts as an output pin when the I90188 (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.
IRDY#	15	DI/O	***Initiator Ready #.*** This signal indicates that the initiator is ready to complete the current data phase of the transaction. This pin acts as an output pin when the I90188 is the bus master of the PCI bus. Otherwise, it is an input pin.
FRAME#	14	DI/O	***FRAME #.*** This signal is driven by the initiator to indicate the beginning and duration of a PCI access.
IDSEL	2	DI	***Initialization Device Select.*** This signal is used as a chip select during configuration read and write transactions.
PAR	23	DI/O	***Parity*** This signal is used for the even parity check on both AD[31:0] & C/BE[3:0]# lines. The PAR input/output direction follows the

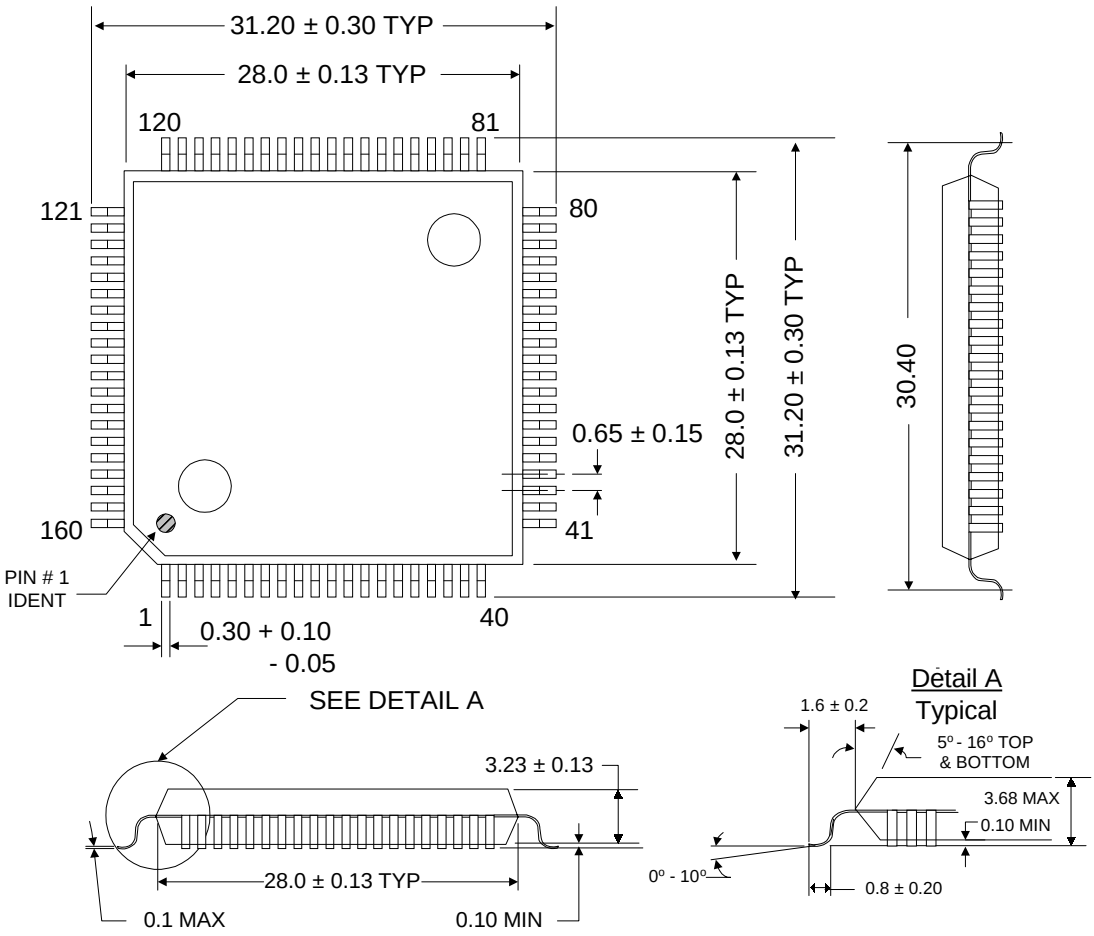
Symbol	Pin #	Type	Description
			AD[31:0] input/output direction.
PERR#	21	DI/O	***Parity Error #.*** This signal is used for reporting data parity errors during all PCI transactions except a Special Cycle. PERR# is an output when AD[31:0] & PAR
SERR#	22	DO	***System Error.*** This signal is used for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. When reporting address parity errors, SERR# is an output.
STOP#	19	DI/O	***Stop.*** This signal indicates that the current target is requesting the initiator to stop the current transaction. This pin acts as an output pin when the I90188 (including ISA slave) is the slave of the PCI bus cycle transaction. Otherwise, it is an input pin.
REQ#	148	DO	***PCI Bus Request.*** This signal is asserted to request the host bridge to allow the I90188 to become the PCI bus master.
GNT#	147	DI	***PCI Bus Grant.*** This signal is asserted from the host bridge allowing the device to become the PCI bus master.
PCICLK	146	DI	***33 MHz PCI Clock.***
PCIRST#	145	DI	***PCI Bus Reset***. PCIRST# is used to reset PCI bus devices.
INTA	144	DO	***PCI Interrupt A.***
PME#	48	DO	***Power Management Event*** This signal is used to report a power management event to the bus.
I90135 CONFIGURATION INTERFACE SIGNALS (Note: The PCLK [Processor Clock] equals to PCICLK = 33MHz)			
SRESET#	93	D0	***I90135 Configuration Interface Reset #.*** This pin is used to reset the I90135 configuration interface.
SAD[15:0]	102 - 104, 106 - 111, 113 - 119	DI/O	***I90135 Configuration Interface multiplexed Address / Data 15 - 0.***
BE1	101	DI	***I90135 Address [1] Input.***
ALE	100	DI/O	***I90135 Address Latch Enable.*** This signal is used to latch the address of the internal register to be accessed.
WR/RD#	98	DI/O	***I90135 Configuration Write / Read #.*** This signal specifies the direction of the I90135 configuration register access cycle.
CS#	99	DO	***I90135 Chip Select.*** This signal indicates I90135 chip selected.
READY#	97	DI/O	***I90135 Ready #.*** This signal controls the OBC (On-Board Controller) bus cycle termination.
INT#	96	DO	***I90135 Configuration Interrupt #.*** This signal request the OBC for interrupt service.
UTOPIA (ATM Cell) INTERFACE SIGNALS			

Symbol	Pin #	Type	Description
TXADDR[1:0]	60 - 59	DO	***Utopia Transmit Multiple PHY Address 1 - 0.*** Two bits wide true data driven from the ATM to MPHY layer to poll and select the appropriate MPHY device. TXADDR[1] is the MSB. Each MPHY device needs to maintain its address.
TXD[7:0]	70 - 69, 67 – 64 62 - 61	DO	***Utopia Transmit Data 7 - 0.*** High octet of data. Most significant octet of transmit data, driven from ATM to PHY.TXD[7] is the MSB, TXD[0] is the LSB of the 8-bit data path.
TXSOC	73	DO	***Utopia Transmit Start of Cell Indication.***
TXENB#	71	DO	***Utopia Transmit Enable #.*** In multiple PHY configurations, TXDENB# is used to tri-state TXDATA and TXSOC PHY layer outputs.
TXCLAV	72	DO	***Utopia Transmit Cell Available.*** In multiple PHY configurations
TXCLK	75	DO	***Utopia Transmit Clock.*** The Utopia Transmit clock frequency is the same as the PUB 25 MHz clock.
RXADDR[1:0]	83 - 82	DI	***Utopia Receive Multiple PHY Address 1 - 0.*** Two bits wide true data driven from the ATM to MPHY layer to poll and select the appropriate MPHY device. RXADDR[1] is the MSB. Each MPHY device needs to maintain its address.
RXD[7:0]	84 - 86, 88 - 92	DI	***Utopia Receive Data 7 - 0.*** High octet of data. Most significant octet of Receive data, driven from PHY to ATM.RXD[7] is the MSB, RXD[0] is the LSB of the 8-bit data path.
RXSOC	78	DI	***Utopia Receive Start of Cell Indication.***
RXENB#	76	DO	***Utopia Receive Enable #.*** In multiple PHY configurations, RXDENB# is used to tri-state RXDATA and RXSOC PHY layer outputs.
RXCLAV	77	DI	***Utopia Receive Cell Available.*** In multiple PHY configurations
RXCLK	79	DO	***Utopia Receive Clock.*** The Utopia Receive clock frequency is the same as the PUB 25 MHz clock.
AC-LINK AC'97 INTERFACE SIGNALS			
ACRESET#	136	DO	***AC'97 Master Reset #.***
SYNC	137	DO	***48 KHz Fixed Rate Sample SYNC.***
SDATA_IN	139	DI	***Serial, time division multiplexed, AC ' 97 input stream.***
BIT_CLK	140	DI	***12.288 MHz Serial Data Bit Clock.***
SDATA_OUT	142	DO	***Serial, time division multiplexed, AC ' 97 Output stream.***
MISCELLANEOUS SIGNALS			
ARESET#	95	DO	***ADSL Controller Reset #.***
TXRXON	124	DI	***Transmit / Receive ON.*** This is an output signal for LED to indicate the ADSL is transmitting (LED on) or receiving (LED off).
OHK	125	DO	***Off Hook.*** This signal indicates the handset is off hook.

Symbol	Pin #	Type	Description
SCANTEST	122	DI	***SCAN Test Input***
SCANMODE	123	DI	***SCAN Mode Input***
DSL/V90#	127	DO	***DSL or V.90 # select.***
RINGDET	128	DI	***Ring Detect.***
LCGDET	129	DI	***Loop Current Sense.***
PILTONE	130	DI	***Pilot Tone.***
XOUT	132	DO	***25 MHz Crystal Output.***
XIN	134	DI	***25 MHz Crystal Input.***
TMODE0	49	DI	***Test Mode Control 0.***
PWRLOSS#	52	DI	***Power Loss Input Signal***
EPROM_DI	53	DO	***Data Input to the serial EPROM***
EPROM_CLK	54	DO	***Clock signal to the serial EPROM***
EPROM_CS	55	DO	***Chip Select signal to the serial EPROM***
EPROM_DO	56	DI	***Data Output from the serial EPROM***
EPROM_SEL	58	DI	***Select Signal from serial EPROM***
GPIO0	50	DI/O	***General Purpose Input / Output 0.***

Package

The I90188 is available in a 160-Pin Plastic Quad Flat Pack.



(DIMENSIONS ARE IN MILLIMETERS)
[160 LEAD PQFP JEDEC METRIC 28 X 28 X 3.4 mm]

ORDERING INFORMATION

Part #	Package
I90188	160 PQFP

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