Technical Specifications

HCC (Hybrid Control Circuit)

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1 INTRODUCTION

1.1 Purpose

The aim of this document is to describe the functions of the HCC (Hybrid Control Circuit) Component. After the ASIC Layout generation and final Simulation

1.2 Reference Documents

[1] ASIC Design and Manufacturing Requirements, WDN/PS/700, ESA, October 1994

[2] Protocol for the TDR (Tracker Data Reduction) to TFE (Tracker Front-End or Hybrid) connection HCC (Hybrid Control Circuit) specification G.Ambrosi & D.Rapin University of Geneva, 22 November 1999.

[3] HCC (Hybrid Control Circuit) Requisiti di Base TC/RBA /99-004.2 rev. 2 10/03/00

1.3 Glossary

Logical operators used in expressions:

Operator	Result
!	NOT: ones complement
*	AND

TFE: Tracker Front-end or Hybrid

TDR: Tracker Data Reduction

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2 GENERAL DESCRIPTION

The HCC component generates the digital signals that controls the VA chips housed on the two front end TFE hybrids K and S.

It reshapes the digital signal for the VAs.

It is controlled by 5 signals generated by the TDR (Tracker Data Reduction) cable connected to the TFE hybrids.

The HCC controls the following operations:

- readout sequence;
- calibration sequence;
- Init, Reset or Abort sequence;

The HCC is fully described in VHDL, including testbenches.

It consumes approximately 1K ASIC gates.

The following figure shows the HCC block diagram.

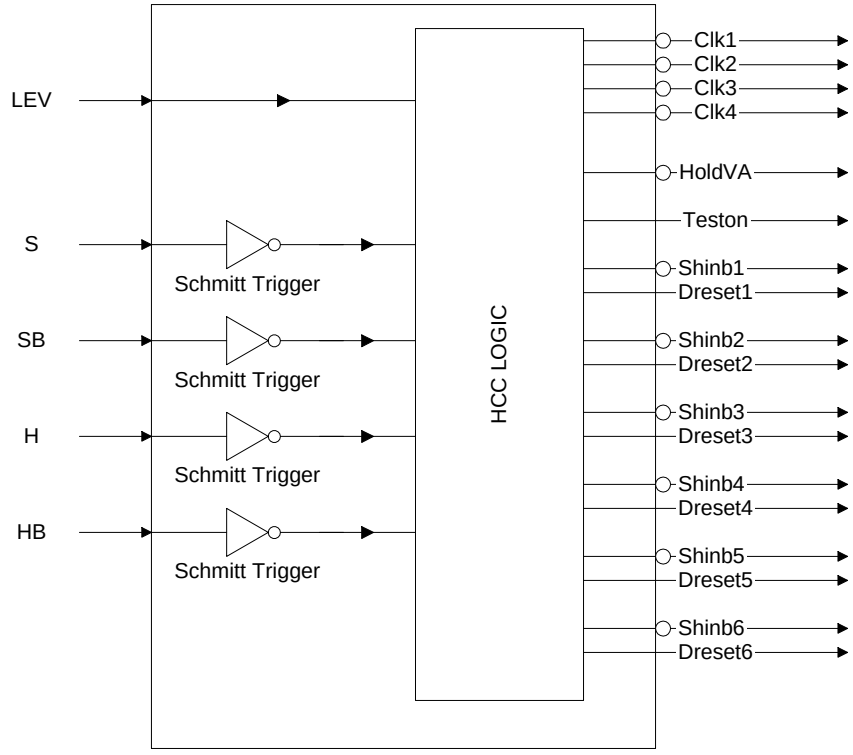


Fig. 1

2.1 Pinouts

Signal Name	Type
S	CMOS Input (with schmitt trigger)
SB	CMOS Input (with schmitt trigger)
H	CMOS Input (with schmitt trigger)
HB	CMOS Input (with schmitt trigger)
LEV	CMOS Input
Clk<4:1>	CMOS Output
HoldVa	CMOS Output
Shinb<6:1>	CMOS Output
Dreset<6:1>	CMOS Output
Teston	CMOS Output
TESTMODE	CMOS Input

2.2 Operating Temperature

Ta 0° C to 70° C

2.3 Absolute Maximum Ratings

Process: 0.6 µm Double Metal CMOS (CUB)

Symbol	Parameter	MIN.	MAX.	UNIT	NOTE
VDD	DC Supply Voltage	-0.3	7.0	V	
Vin	Input Pin Voltage	-0.3	VDD + 0.3	V	
Iin	Input Current on any Pin	-100	+100	mA	25 deg.C
Tstrg	Storage Temperature	-65	+150	deg.C	
H	Humidity Noncondensing	5	85	%	Noncond.
	Electrostatic Discharge		1000	V	R=1,5kOhm C=100pF
	Lead Temperature		(1)	deg.C	T=10s

(1) 300 deg. C: all ceramic packages and DIL plastic packages
260 deg. C: for surface mounting plastic packages

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent

damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (eq. hot carrier degradation).

2.4 DC Characteristics

Input PADs Schmitt Trigger characteristics.

		Ta=0 to +70			
PARAMETER	**Vdd**	**MIN**	**MAX**	**UNIT**	**Conditions**
Hysteresis (V_{T+}- $V_{T\grave{o}}$)	3,6 V	1,15	2,05	**V**	Ta=worst case
	4,5 V	1,20	2,10		

Symbol	Parameter	Operating cond.	Min.	Typ.	Max.	Units
	negative-going threshold	CMOS Input (with schmitt trigger)	0.90		1.45	V
	positive-going threshold	CMOS Input (with schmitt trigger)	2.50		3.00	V
VIL	Low Input Voltage	CMOS Input		1.2		V
VIH	High Input Voltage	CMOS Input		2.8		**V**
IIL		All Inputs			-1.0	uA
IIH		All Inputs			1.0	uA

NOTE: All the above values have been calculated for Vdd = 4 Volts.

- **Clk <4:1>, HoldVa, Teston**

  Vol(max) = 0.4 V

  Vih(min) = 3.5 V (Vdd - 0.5)

  Iol (vdd=4V) = 6.5 mA

  Ioh (vdd=4V) = -6.5 mA

- **Dreset<6:1>, Shinb<6:1>**

  Vol(max) = 0.4 V

  Vih(min) = 3.5 V (Vdd = 4V)

  Iol (vdd=4V) = 3.25 mA

  Ioh (vdd=4V) = -3.25 mA

2.5 AC Characteristics

Rise time vs.output load / supply voltage for OB35 and OB33 pads (typical case)

OB35	Clk <4:1>, HoldVa, Teston Output Slope (ns)					
	Output load (pF)					
Vdd	10 pF	20 pF	30 pF	40 pF	50 pF	70 pF
3,3 V	*3,20* (1)	5,55	7,89	10,24	12,59	*17,28*(1)
4 V	**2,61**	**4,53**	**6,45**	**8,37**	**10,29**	**14,13**
5 V	*2,20*(1)	3,82	5,44	7,06	8,68	*11,92*(1)

OB33	Dreset<6:1>, Shinb<6:1> Output Slope (ns)					
	Output load (pF)					
Vdd	10 pF	20 pF	30 pF	40 pF	50 pF	70 pF
3,3 V	*4,02* (1)	7,98	11,93	15,89	19,84	*27,75*(1)
4 V	**3,29**	**6,49**	**9,69**	**12,89**	**16,09**	**22,50**
5 V	*2,78*(1)	5,45	8,13	10,80	13,47	*18,82*(1)

(1) Values in italic = library data

I/O Delay Table		Delay (ns) (Output rising transition)			Delay (ns) (Output falling transition)		
From	To	Min. (1)	Typ. (1)	Max. (1)	Min. (1)	Typ. (1)	Max. (1)
S,SB	Clk<4:1>	6.9	12.4	19.8	5.3 (6.7) (2)	9.7 (12.3) (2)	16.1 (21.0) (2)
S,SB	Shinb<6:1>	5.9	10.8	18.0	6.9	12.6	22.0
S,SB	Dreset<6:1>	7.0	12.7	21.5	5.0	9.2	15.2
S,SB	Teston	8.2	14.6	23.7	6.5	11.6	19.3
H,HB	HoldVa	6.0	10.5	15.8	4.0	7.0	12.5

(1) Min.= Process best case, Tj = -50°C, Vdd = 4.4 Volts
Typ = Process typical, Tj = 25°C, Vdd = 4.0 Volts
Max. = Process worst case, Tj = 125°C, Vdd = 3.6 Volts

(2) First readout cycle

All the above values have been calculated for: Input slope = 10 ns, Output Load = 20 pF.

2.6 HCC Power Rails and physical levels

Signal Name	Nominal Value	Description	Note
Vdd	+ 2 Volts	Power	Digital Vdd of the VAs
Vss	- 2 Volts	Power	Digital Vss of the VAs

Logica level	Physical Value	Description	Note
1	+ 2 Volts	Vdd	
0	- 2 Volts	Vss	

2.7 Power dissipation

Parameter	Max	Min	Note
AC power dissipation	15 mW	-	STR/STB frequency :5 MHz

2.8 HCC Technology

AMS 0.6µm CMOS 2M CUQ with epitaxial layer

A certain level of latch up immunity will be guaranteed by the epitaxial layer, but currently we have not any "number" from experimental results.

In addition AMS 0.6 µm CMOS technology is not intended for space application, as a consequence we cannot guarantee any total dose immunity.

For SEU immunity ad hoc techniques will be adapted by design in order to increase it; anyway also in this case no precise "number" will be guaranteed.

2.9 Application

This chip architecture is implemented taking into account the constraints of a typical space application (error coding and correction, low-power, etc.).

The HCC ASIC contains structures for SEU protection and structures for testability: a 100% scan chain to obtain fault coverage higher than 97%.

The HCC ASIC is implemented following a full Triple Modular Redundancy (TMR) approach. All flip-flops are triplicated and a majority voting circuit is implemented along with each set of three flip-flops, in order to determine the effective present state. Each set of three flip-flops receives the same input signal.

The implementation of the TMR architecture eliminates SEU effects on all the memory-sensitive elements of the circuit in such a way that:

- an upset in one of the three flip-flops does not affect the present state (upset masked)
- the upset flip-flop recovers its correct state at the next system clock event.

3 FUNCTIONAL DESCRIPTION

3.1 Signal description

Signal Name	Type	Explanation	Note
S	Input	STR: Strobe line differential. STR= S * !SB	TDR/TFE cable signals
SB	Input		
H	Input	Two independent levels that controls the HCC operations	
HB	Input		
LEV	Input	Controls the output polarity	
Clk<4:1>	Output	Clock signal for Hybrid Vas	Va ckb
HoldVa	Output	Hold analog data	Va holdb
Shinb<6:1>	Output	Shinb<i>: start pulse for Va<i> readout	Va shift_in_b
Dreset<6:1>	Output	Dreset<i>: digital Va<i> reset	Va dreset
Teston	Output	Turn Hybrid Vas in test-mode	Va test_on
TESTMODE	Input	Set the HCC in test mode	1=Test mode 0= Operating Mode

3.2 Operating Modes

TESTMODE signal = 0.

The following table shows the TDR signals for the 3 HCC sequences :

- readout ;
- calibration;
- Init, Reset or Abort;

Signal Name	Init state	Readout	Calibration			Init Reset Abort
S	0	STR =386 pulses	STR = 1 pulse	0	STR =386 pulses	STR = 1 pulse
SB	1			1		
H	0	1	1	0	0	0
HB	1	0	1	1	0	1

3.2.1 Output signal polarity

Signal Name	Logical Level	Output Signals level after Init, Reset, or Abort sequence				
		Clk<4:1>	HoldVa	Teston	Shinb<6:1>	Dreset<6:1>
LEV	1	1	1	0	1	0
LEV	0	0	0	1	0	1

3.2.2 Init state (LEV=1)

Signal Name	Logical Level	Explanation
S	0	STR=0.
SB	1	
H	0	
HB	1	
Clk<4:1>	1	
HoldVa	1	
Teston	0	
Shinb<6:1>	1	
Dreset<6:1>	0	

3.2.3 Readout sequence (LEV=1)

Signal Name	Init state	Readout		Init state
S	0	0	STR =386 pulses	0
SB	1	1		1
H	0	1	1	0
HB	1	0	0	1
Clk<4:1>	1	0	= !STR	1
HoldVa	1	0	1	1
Teston	0	0	0	0
Shinb<6:1>	1	1	See next table	1
Dreset<6:1>	0	0		0

	Shinb<6:1>						Dreset<6:1>					
Nr. Clk pulse	1	2	3	4	5	6	1	2	3	4	5	6
1	0	1	1	1	1	1	0	0	0	0	0	0
2	1	1	1	1	1	1	0	0	0	0	0	0
64	1	1	1	1	1	1	0	0	0	0	0	0
65	1	0	1	1	1	1	0	0	0	0	0	0
66	1	1	1	1	1	1	1	0	0	0	0	0
128	1	1	1	1	1	1	0	0	0	0	0	0
129	1	1	0	1	1	1	0	0	0	0	0	0
130	1	1	1	1	1	1	0	1	0	0	0	0
192	1	1	1	1	1	1	0	0	0	0	0	0
193	1	1	1	0	1	1	0	0	0	0	0	0
194	1	1	1	1	1	1	0	0	1	0	0	0
256	1	1	1	1	1	1	0	0	0	0	0	0
257	1	1	1	1	0	1	0	0	0	0	0	0
258	1	1	1	1	1	1	0	0	0	1	0	0
320	1	1	1	1	1	1	0	0	0	0	0	0
321	1	1	1	1	1	0	0	0	0	0	0	0
322	1	1	1	1	1	1	0	0	0	0	1	0
384	1	1	1	1	1	1	0	0	0	0	0	0
385	1	1	1	1	1	1	0	0	0	0	0	0
386	1	1	1	1	1	1	0	0	0	0	0	1
387	1	1	1	1	1	1	0	0	0	0	0	0
388	1	1	1	1	1	1	0	0	0	0	0	0
388+n	1	1	1	1	1	1	0	0	0	0	0	0

Readout sequence STR timing:

- STR pulse #1, #65,#129,#193, #257, #321 > 100 ns
- Other STR pulse > 50 ns

The read-out is started by the overlap (coincidence) of Clk and Shinb<i>.

- Overlap > 40 ns

A sequence of Readout can be aborted (Clk pulse Number <386) by means of one sequence of Init Reset or Abort.

After the 386-STR pulse the HCC enters in a IDLE state.

Successive STR pulses do not modify the HCC IDLE state.

The HCC is Initialized by two different operations :

- Init Reset or Abort sequence;
- Init state (>50 ns.)

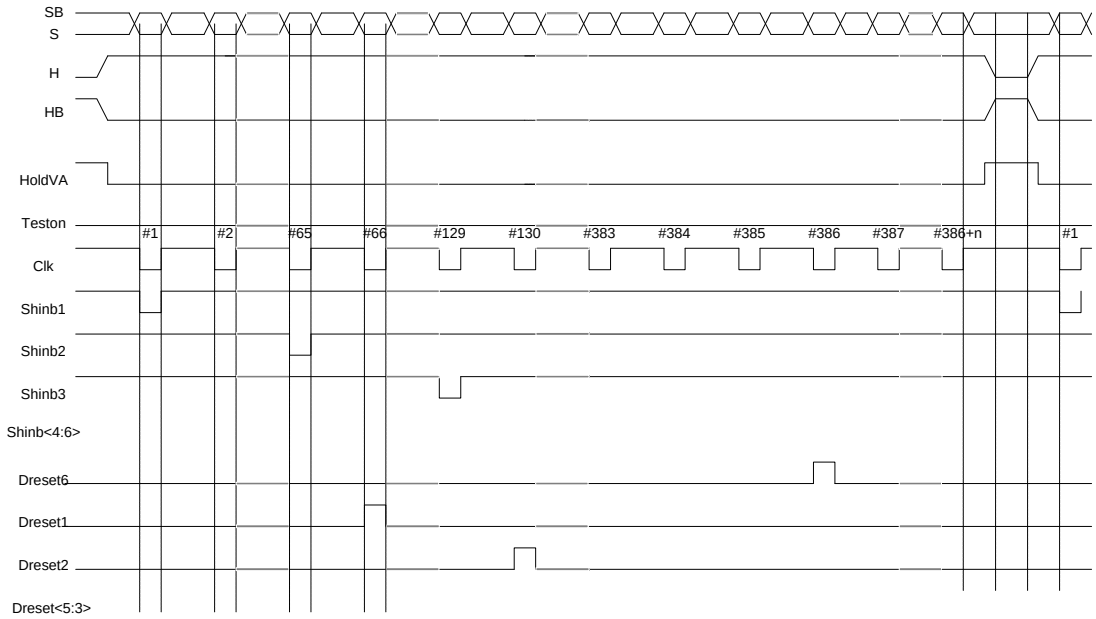


Fig. 2 Readout Sequence

3.2.4 Calibration sequence (LEV=1)

Signal Name	Init state	Calibration			
S	0	0	STR =1 pulses	0	STR =386 pulses
SB	1	1		1	
H	0	1	1	0	0
HB	1	1	1	1	0
Clk<4:1>	1	1	1	1	=!STR
HoldVa	1	1	1	1	1
Teston	0	0	1 on the rising edge of STR	1	1
Shinb<6:1>	1	1	1	1	See previous table
Dreset<6:1>	0	0	0	0	

The HCC is returned into normal mode after a Init Reset or Abort sequence.

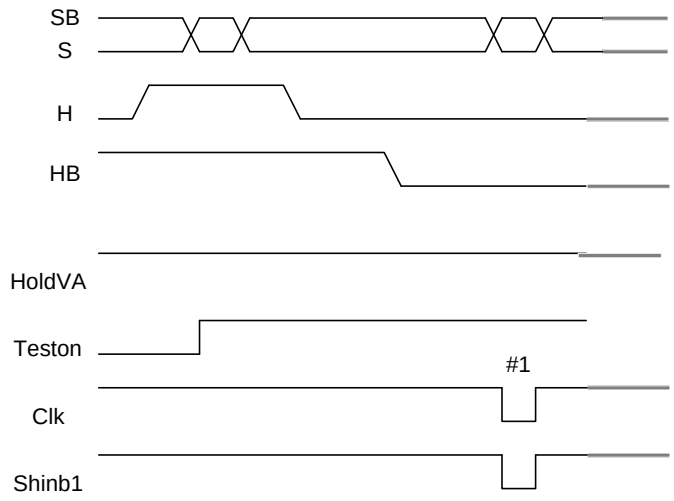


Fig. 3 Calibration sequence (Shinb <6:1> and Dreset<6:1> as for read-out sequence

3.2.5 Init, Reset or Abort sequence(LEV=1)

Signal Name	previous state	Init Reset or Abort		Init state
S	0	0	STR =1 pulses	0
SB	1	1		1
H	X	0	0	0
HB	X	1	1	1
Clk	1	1	1	1
HoldVa	X	1	1	1
Teston	X	X	0 on the rising edge of STR	0
Shinb<6:1>	1	1	1	1
Dreset<6:1>	0	0	=STR	0

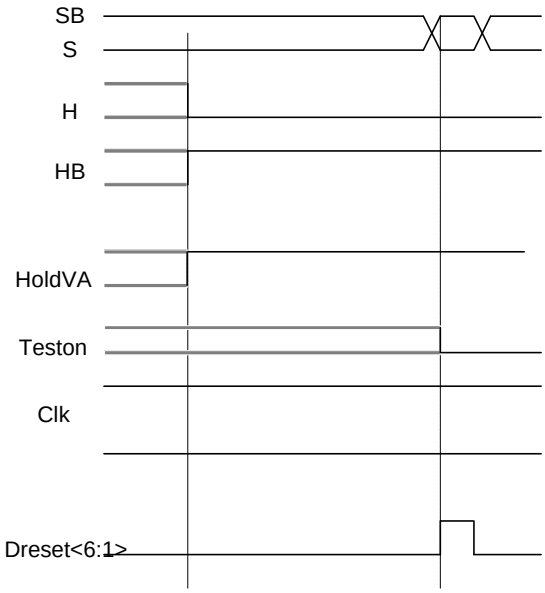


Fig. 4 Init, Reset or Abort sequence

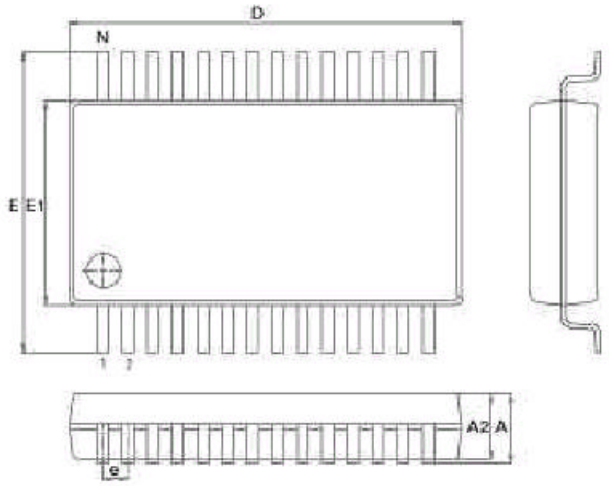
4 HCC PIN-OUTS

4.1 Package

28 pin Shrink Small Outline Package (SSOP – 28L)

Dimensions: 7.80 x 10.20 mm

Pin to Pin spacing: 0.65 mm



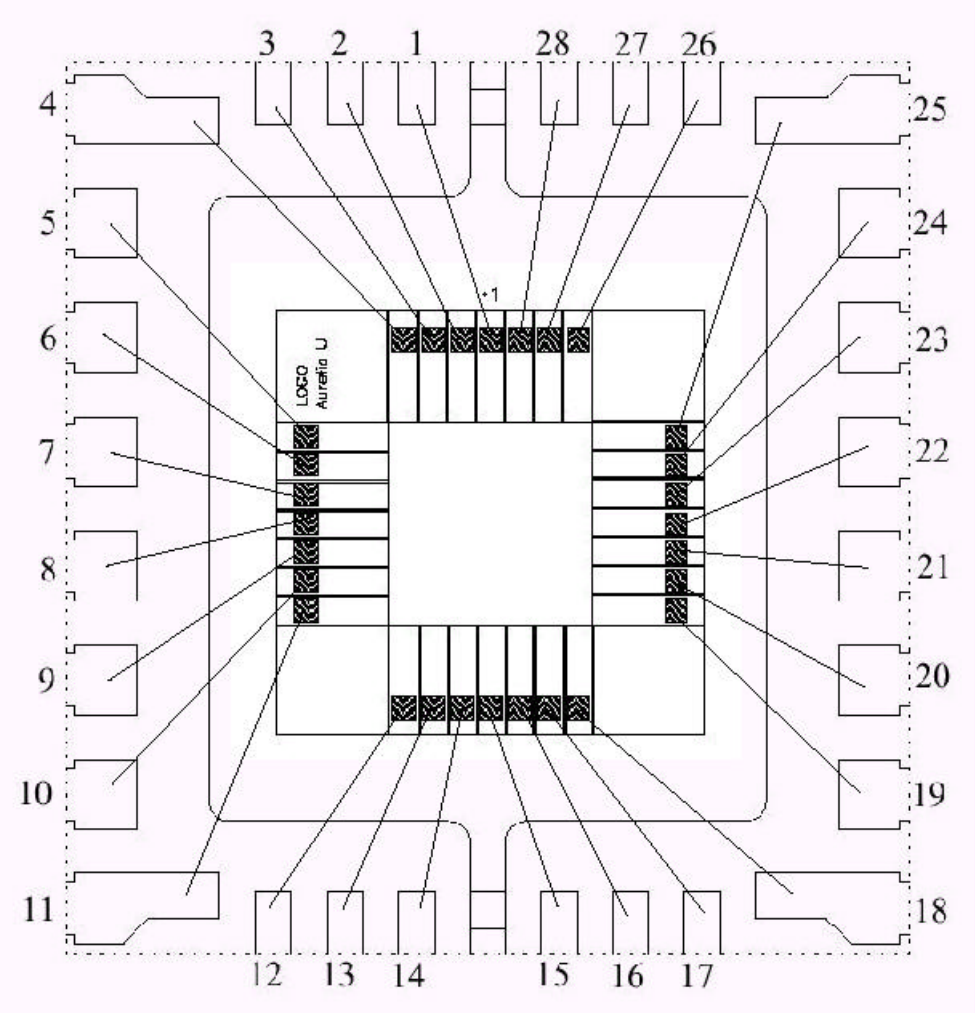
Values:

D = 10.20 mm
E1 = 5.30 mm
E = 7.80 mm
e = 0.65 mm
A = 2.0 mm (MAX)
A2 = 1.75 mm

4.2 Pin assignment

Pin	Signal Name	Function	Pin	Signal Name	Function
1	Shinb<6>	Output	15	Shinb<1>	Output
2	Dreset<6>	Output	16	Dreset<1>	Output
3	Teston	Output	17	Shinb<2>	Output
4	Gnd-core (Vss)	Power supply	18	Vdd-pherip	Power supply
5	Clk<4>	Output	19	Dreset<2>	Output
6	TESTMODE	Input	20	Dreset<3>	Output
7	LEV	Input	21	Shinb<3>	Output
8	S	Input	22	Clk<1>	Output
9	SB	Input	23	Clk<2>	Output
10	H	Input	24	Shinb<4>	Output
11	HB	Input	25	Dreset<4>	Output
12	Vdd-core	Power supply	26	Gnd-periph (Vss)	Power supply
13	Clk<3>	Output	27	Shinb<5>	Output
14	HoldVa	Output	28	Dreset<5>	Output

4.3 Bonding Diagram



5 HCC-TFE CONNECTIONS

The hybrid S houses 10 VA_hdr chip and two differential signals (Outp1,Outm1 and Outp2 Outm2) for the VA analog outputs: 2 VA will come read at the same time.

- Shinb<1> readout VA 1 and 6;
- Shinb<2> readout VA 2 and 7;
- Shinb<3> readout VA 3 and 8;
- Shinb<4> readout VA 4 and 9;
- Shinb<5> readout VA 5 and 10.

The hybrid K houses 6 VA_hdr chip and 1 differential signal (Outp1,Outm1) for the VA analog outputs.

- Shinb<1> readout VA 1 ;
- Shinb<2> readout VA 2 ;
- Shinb<3> readout VA 3 ;
- Shinb<4> readout VA 4 ;
- Shinb<5> readout VA 5 .
- Shinb<6> readout VA 6 .

Signal Name	Explanation	VA pin	Nr. VA Chip connected	
			hybrid S	hybrid K
Clk<1>	Clock signal for Hybrid Vas	Va ckb	3	3
Clk<2>	Clock signal for Hybrid Vas	Va ckb	3	3
Clk<3>	Clock signal for Hybrid Vas	Va ckb	2	-
Clk<4>	Clock signal for Hybrid Vas	Va ckb	2	-
HoldVa	Hold analog data	Va holdb	10	6
Shinb<6:1>	Shinb<i>: start pulse for Va<i> readout	Va shift_in_b	2	1
Dreset<6:1>	Dreset<i>: digital Va<i> reset	Va dreset	2	1
Teston	Turn Hybrid Vas in test-mode	Va test_on	10	6

6 TDR SPECIFICATIONS

6.1 Operating Modes

The following table shows the TDR signals for the 3 HCC sequences :

- readout ;
- calibration;
- Init, Reset or Abort;

Signal Name	Init state	Readout	Calibration			Init Reset Abort
S	0	STR =386 pulses	STR = 1 pulse	0	STR =386 pulses	STR = 1 pulse
SB	1			1		
H	0	1	1	0	0	0
HB	1	0	1	1	0	1

6.2 TDR Readout operation timing

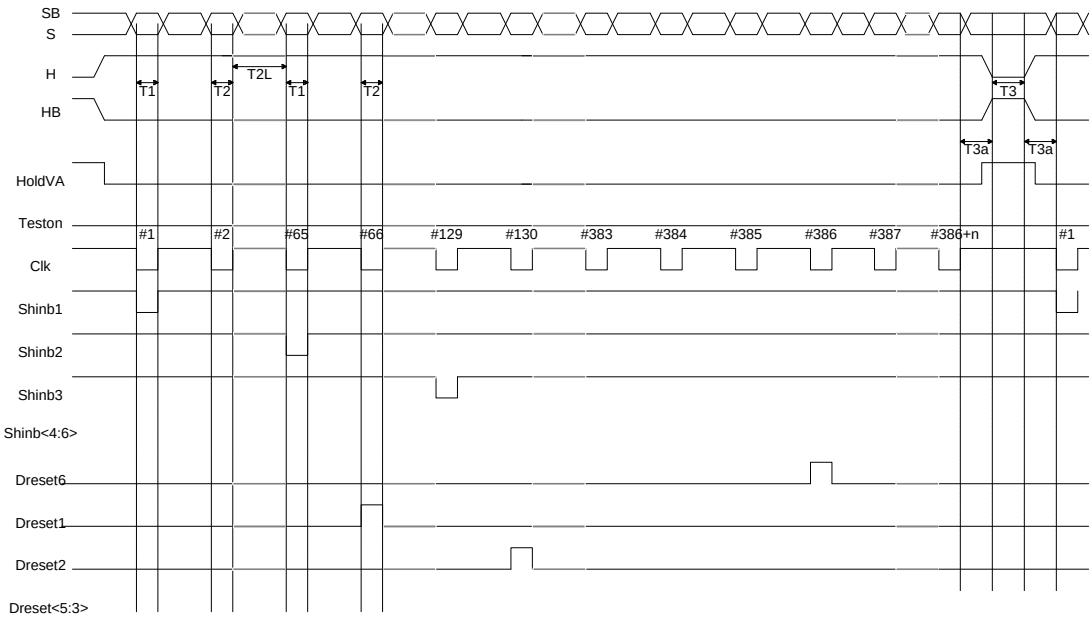


Fig. 5 TDR Readout operation timing

- T1> 100 ns STR pulse #1, #65,#129,#193, #257, #321
- T2> 50 ns Other STR pulses.
- T3 > 50 ns Init state after a Readout sequence
- T2L > 150 ns
- T3a > 30 ns

After a Readout operation, the TDR must perform one of these two operations (to Initialize HCC):

- Init, Reset or Abort operation
- Init state

A Readout operation can be aborted (Clk pulse Number <386) performing an Init Reset or Abort. operation

6.3 TDR Calibration operation timing

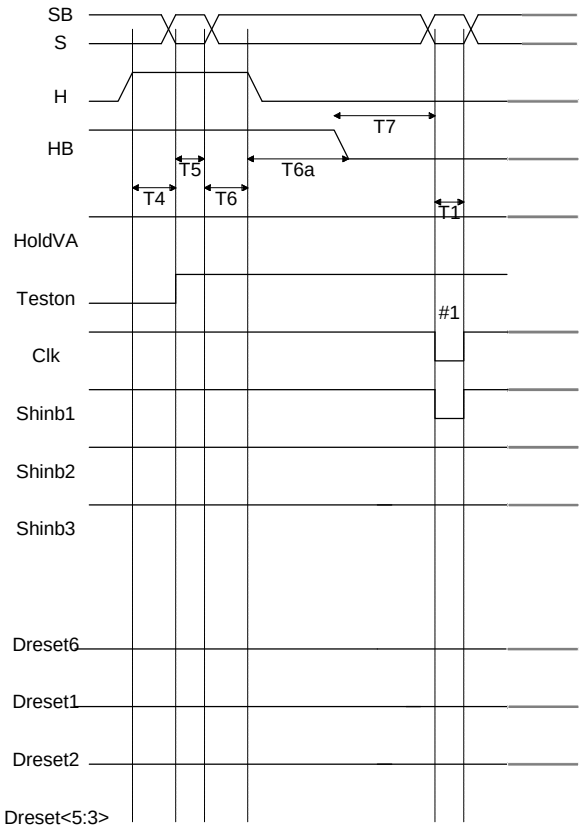


Fig. 6 Calibration operation

- T4 > 100 ns
- T5 > 100 ns
- T6 > 100 ns
- T6a > 20 ns
- T7 > 50 ns

The following STR pulses will have the same characteristics of the Readout operation

- T1 > 100 ns STR pulse #1, #65,#129,#193, #257, #321
- T2 > 50 ns Other STR pulse.

After a Calibration operation, the TDR must perform an Init, Reset or Abort operation

Before a Calibration operation, the TDR must perform an Init, Reset or Abort operation

6.4 TDR Init, Reset or Abort operation timing

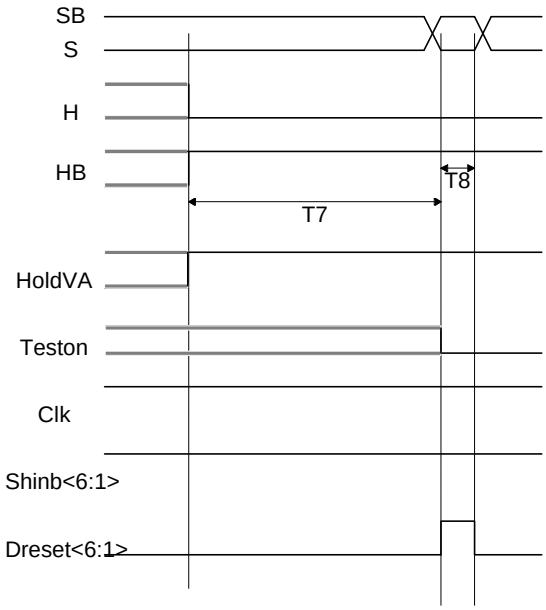


Fig. 7 Init, Reset or Abort operation

- T7 > 50 ns
- T8 > 50 ns

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