Technical Specification

FROST64

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INDEX

1. INTRODUCTION

1.1. Purpose

The technical specifications of Frost64, a fast and low noise photon counting ASIC developed for biomedical application are given in this document.

1.2. Reference Documents

[1] 16_AS_CNTSHF datasheet

[2] Franky: Datasheet e test

1.3. Glossary

AI	Analog Input Pin
AO	Analog Output Pin
A I/O	Analog Input/Output Pin
DI	Digital Input Pin
DO	Digital Output Pin
D I/O	Digital Input/Output Pin
PG	Power/Ground Pin

2. PRODUCT DESCRIPTION

FUNCTION:	64-channel pixel detector
TECHNOLOGY	AMS 0.8um CMOS CXQ
CELL SIZE	4555um x 11430um (52.0 mm^2)
POWER CONS.	100 mA @ 5 V
PACKAGE	CQFP120
N. of PADS	117
INPUT PAD PITCH	130um

2.1. Short Description

64-channel, fast and low noise single photon counting system developed in order to reach an acceptable time duration of the digital mammography exam. It consist in 64 identical channel. Each channel has an analogue input section with a low noise preamplifier and a CR-RC^2 shaper, a discriminator section with a 3 bit DAC in order to reach locally the discriminator threshold and a readout full-custom digital section. To set globally the discriminator threshold of all channels a 6 bit DAC is used.

2.2. Main Characteristics

3.7.1 Analog Section

- Sensitivity: 150 mV/fC with 10pF of input capacitance.
- Peaking time: 311 ns
- Decay time: 0,55μs
- polo/zero cancellation
- Non Linearity < +/- 1,2%
- Maximum noise @ Cin = 10pF: 850e^- rms
- Gain time spread : +/-2,5%
- Peaking time spread: +/- 1%
- Adjustable threshold with 6 bit DAC
- Minimum detectable signal: 1fC
- Counting rate : 1 Mhz

3.7.2 Digital section

- 16 bit asynchronous counter with external reset and enable and serial output for each channel
- 20MHz output speed

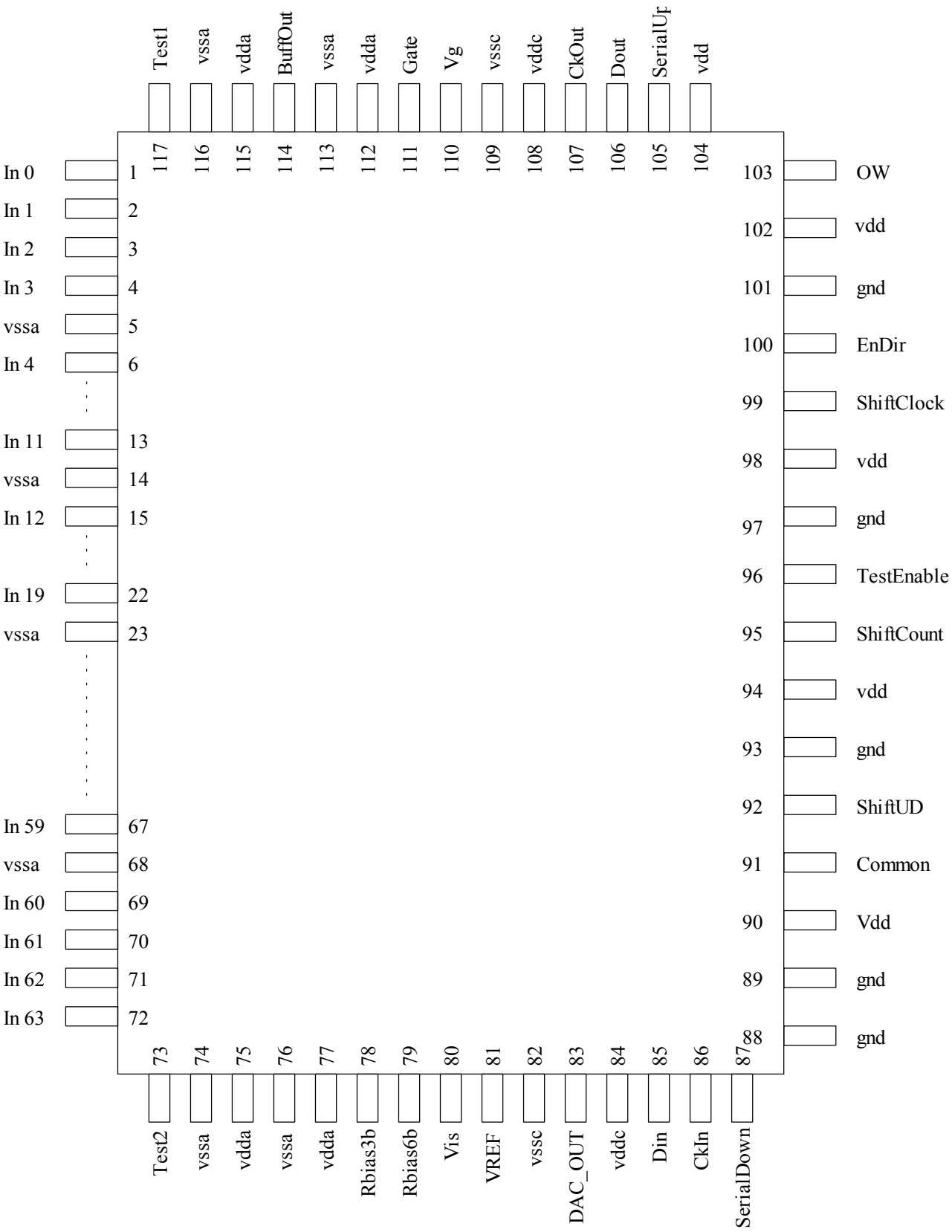

Test1
vssa
vdda
BuffOut
vssa
vdda
Gate
Vg
vssc
vddc
CkOut
Dout
SerialUp
vdd
117
116
115
114
113
112
111
110
109
108
107
106
105
104
In 0
1
In 1
2
In 2
3
In 3
4
vssa
5
In 4
6
In 11
13
vssa
14
In 12
15
In 19
22
vssa
23
In 59
67
vssa
68
In 60
69
In 61
70
In 62
71
In 63
72
103
OW
102
vdd
101
gnd
100
EnDir
99
ShiftClock
98
vdd
97
gnd
96
TestEnable
95
ShiftCount
94
vdd
93
gnd
92
ShiftUD
91
Common
90
Vdd
89
gnd
88
gnd
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
Test2
vssa
vdda
vssa
vdda
Rbias3b
Rbias6b
Vis
VREF
vssc
DAC_OUT
vddc
Din
CkIn
SerialDown

Figure 1

2.3. Pads Description

Name	Pin	Type	Note
in0 – in63	1-4, 6-13,15-22,24-31,33-40,42-49,51-58,60-67,69-72	AI	Channel input (wired – bonding to silicon detector)
test2	73	AI	32-channel calibration input
gnda	5,14,23,32,41,50,59,68, 74,76,113,116	PG	Ground of analogue section
vdda	75,77,112,115	PG	Supply of analogue section
rbias3b	78	A I/O	DAC3 bias resistor
rbias6b	79	A I/O	DAC6 bias resistor
Vis	80	A I/O	Discriminator's hysteresis calibration
VREF	81	A I	DAC voltage reference
vssc	82,109	PG	Ground of discriminator section
vddc	84,108	PG	Supply of discriminator section
DAC_OUT	83	AO	DAC6 output
D_in	85	DI	Stream input to program discriminator section
ck_in	86	DI	Clock input to program discriminator section
serial_down	87	D I/O	Down shift register chain
gnd	88,89,93,97,101	PG	Ground of digital section
vdd	90,94,98,102,104	PG	Supply of digital section
common	91	DI	Counter input during test modality
shift_UD	92	DI	Selector for shift direction
shift_count	95	DI	Shift or count enable
test_enable	96	DI	Test modality enable
shift_clock	99	DI	Clock to serial readout
en_dir	100	DI	Clock phase during test modality
ow	103	DO	Overflow flag (wired-or)
serial_up	105	D I/O	Up shift register chain
D_out	106	DO	Stream output to program discriminator section
ck_out	107	DO	Clock output program discriminator section
Vg	110	A I/O	Discriminator bias forcing
gate	111	A I	Pole-zero cancellation
BuffOut	114	AO	Channel <0> analogue output
Test 1	117	AI	32-channel calibration input

Table 1

2.4. Pads Distribution

Pads are distribute uniformly along each side of the chip with different pitch :

- 72 pads on left side (pads n. 1 – 72), pitch 130 um
- 15 pads on down side (pads n. 73 - 87), pitch 235 um
- 16 pads on right side (pad 88 103), pitch 620 um
- 14 pads on up side (pad 104 - 117), pitch 235um
- **Chip Area:** (X x Y): 4588 um x 11354 um = 52.09 mmq

3. FUNCTIONAL DESCRIPTION

The chip structure is depicted in Figure . It is mainly composed by 8 blocks of 8 channels each and a calibration section (including DACs and polarization circuits). The analog output of channel 0 is buffered and connected to pad to be easily tested.

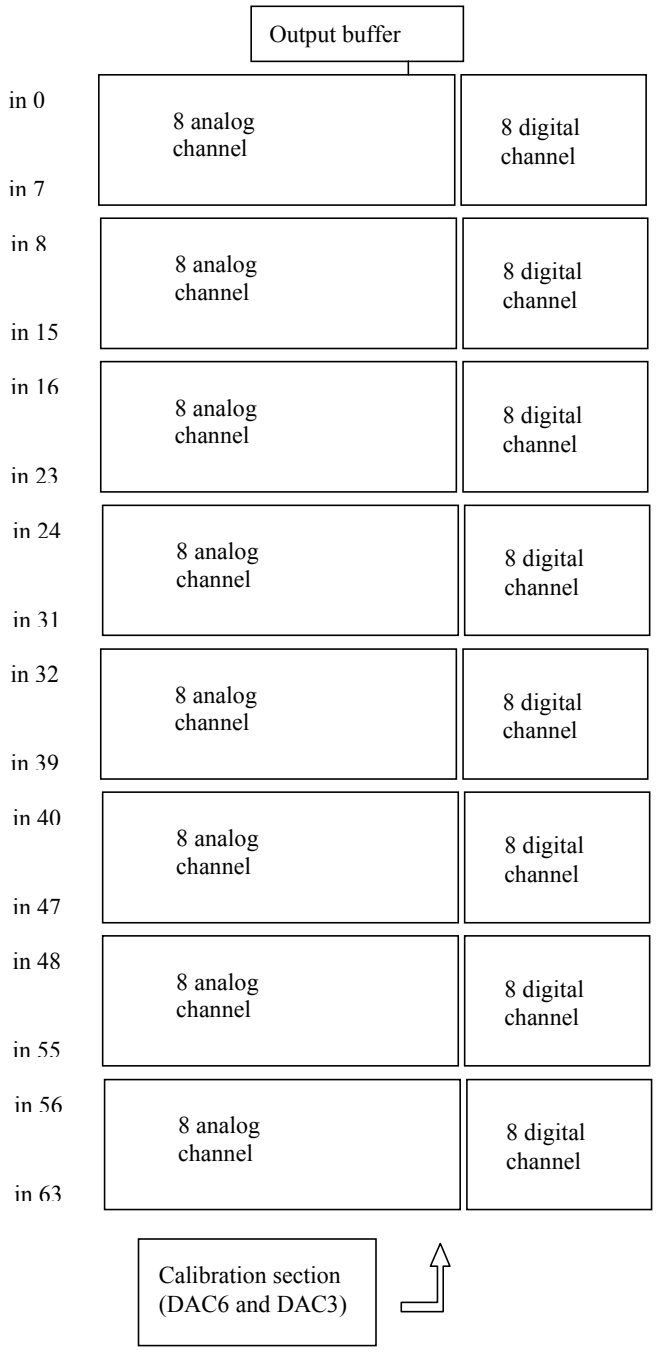


Figure 2

The upper block of 32 channels and the lower block of 32 have separate voltage supply, whereas a ground pin exists for each block of 8 channels.
Each 8 channels block structure is shown in Figure 1.

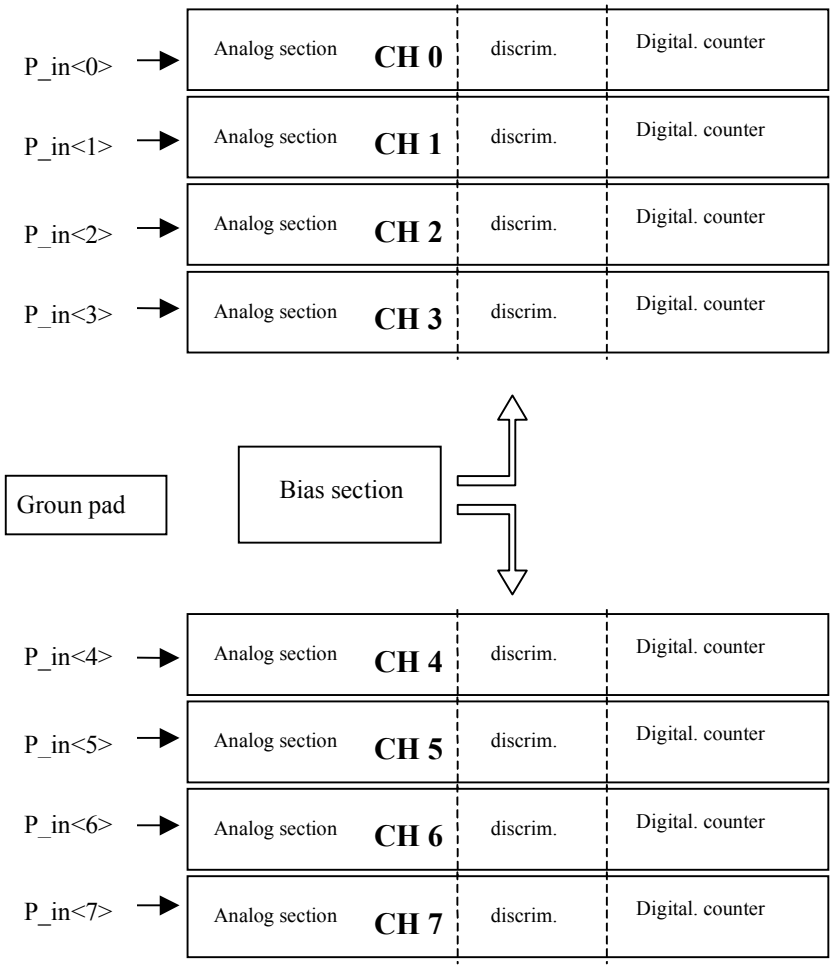


Figure 1

The Bias section provides bias currents and voltage references for each analog section of the channels.

3.1. Analog channel

The analog channel is now described in more detail. Figure 2 shown its basic structure: charge preamplifier , shaper and comparator. The shaper block provides a CR-RC^2 shaping with pole-zero cancellation. Figure 3 shows how the circuit has been implemented. Two MOS resistor are used: one as feedback resistor for the charge preamplifier and one for the pole-zero cancellation network. All of the 64

channels have the gate of those transistor connected together to pad "P_vg ". The normal voltage to apply at this pad is 0 V but it may be decrease up to –0.2V if the feedback resistor became too large.

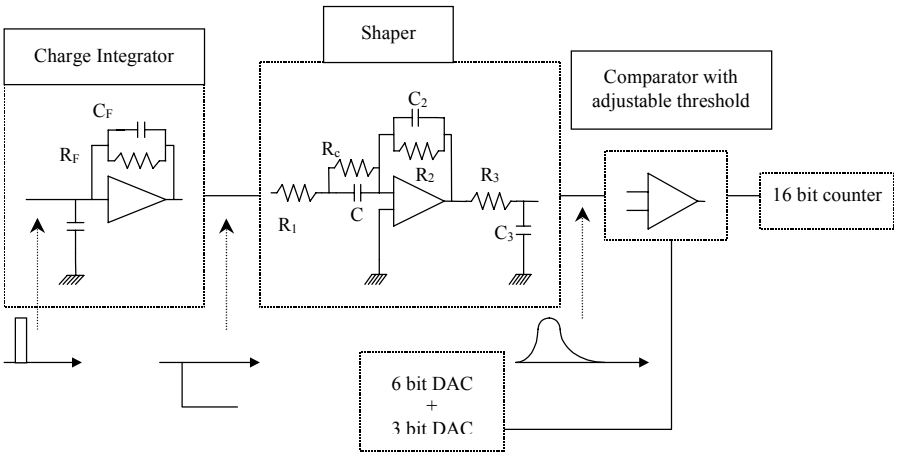


Figure 2

The circuit contains three identical inverting amplifier, in this way the shaper output has the same DC voltage level of the preamplifier input.

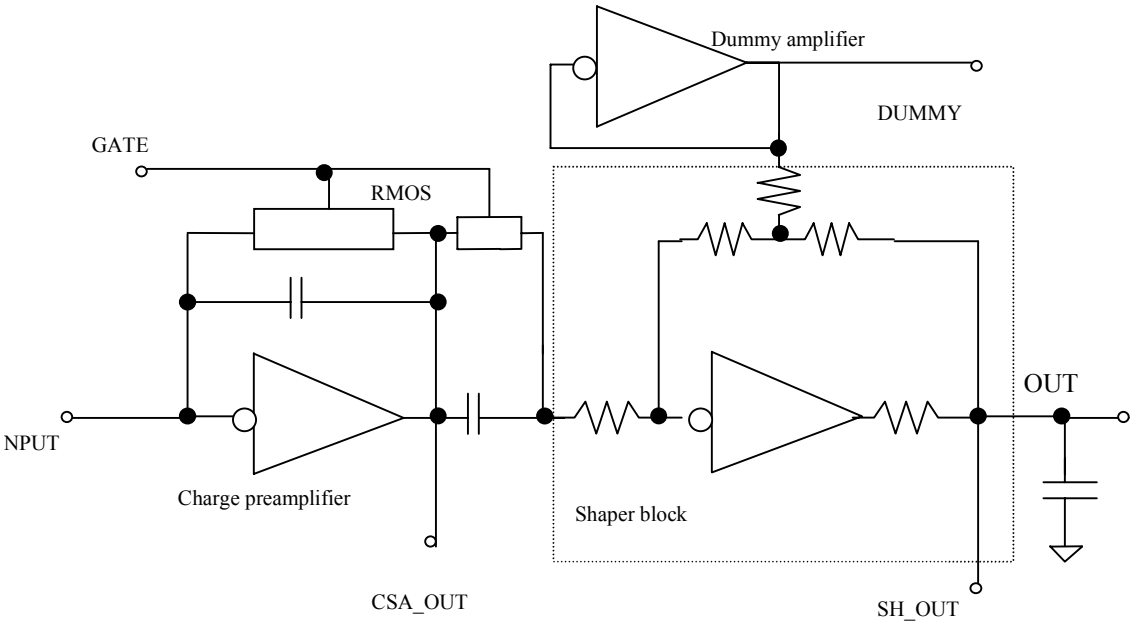


Figure 3

There is only one "dummy amplifier" for 8 channel included in "Bias section" of Figure 1.

3.2. Output Buffer

This buffer let the output of channel 0 to be externally available at pin P_BuffOut. It shift the DC voltage of the shaper output of +1.0V and must be AC coupled at the scope input. All the characteristics of the shaped signal (sensitivity , peaking time, rise time, fall time and linearity) are unaffected by the buffer.

3.3. Discriminator

The discriminator compare the shaped signal with an adjustable threshold voltage that can be varied globally by a 6 bit DAC and locally (for a single discriminator) by a 3 bit DAC. It is provided of an hysteresis, for noise immunity, that can be regulated for all 64 discriminator by a voltage applied to the pin P_Vis. The commutation speed can by also adjusted changing the polarization current; this can be done forcing the pin P_Vg at different voltage level.

3.4. Threshold regulation

The discriminator threshold can be set for all 64 channel by the 6 bit DAC and finely tuned for each discriminator by the 3 bit DAC. DACs connection and reference distributions are shown in Figure 4. A voltage reference must be applied to the pin P_VREF and two resistors must be connected between pads P_Rbias3b and P_Rbias6b to ground; they set the voltage range for DAC3 and DAC6 respectively. DAC6 generates a voltage always greater or equal to VREF. This voltage is passed to the block called "DAC3 references" that generates 8 voltage level distributed to all 64 DAC3. DAC3 is simply composed by 8 switch that let to connect the negative input of the discriminator to the desired voltage. They can be selected by a 3 bit data stored in a 3 bit shift register as shown in Figure 5. To set the voltage threshold for all the 64 channel a stream of 198 bit is needed. The clock must applied at pin "CkIn" and data enter serially at pin "P_Din" and exit at pin P_Dout. The first entering 3 bits set the threshold for channel 0 and the last 6 bit set the DAC6 voltage.

The timing diagram is shown in Figure 6: the entering datum is sampled in the rising edge of the clock CKIn; when a datum enter at input Din one datum come out from pin Dout. Figure 7 shows how data are weighted when stored in the shift registers.

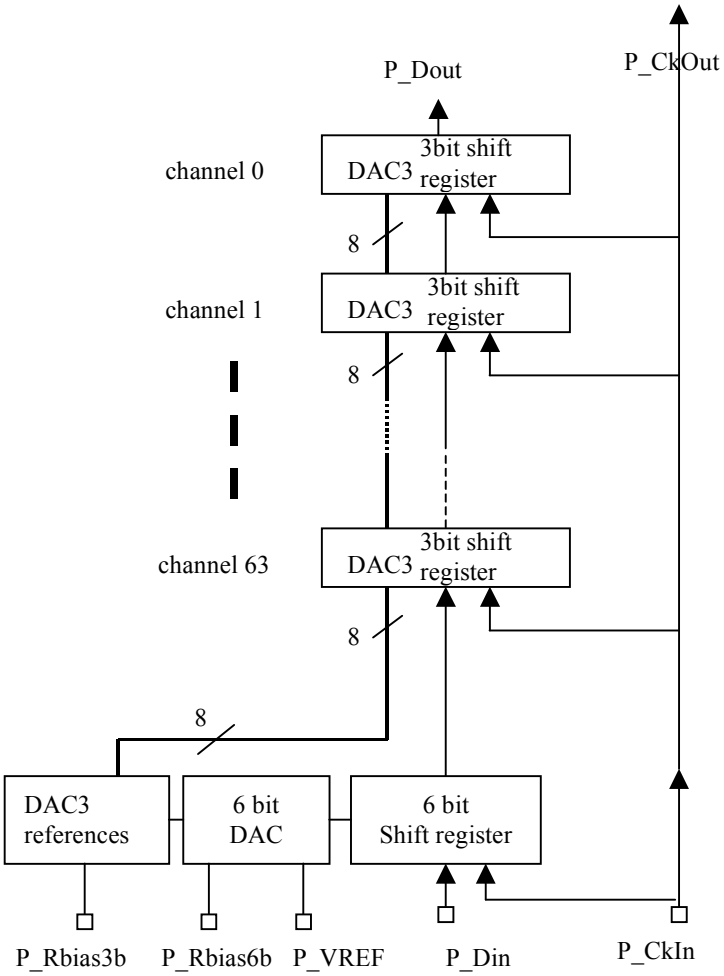

P_Dout
P_CkOut
channel 0
DAC3
3bit shift register
8
channel 1
DAC3
3bit shift register
8
channel 63
DAC3
3bit shift register
8
8
DAC3 references
6 bit DAC
6 bit Shift register
P_Rbias3b
P_Rbias6b
P_VREF
P_Din
P_CkIn

Figure 4

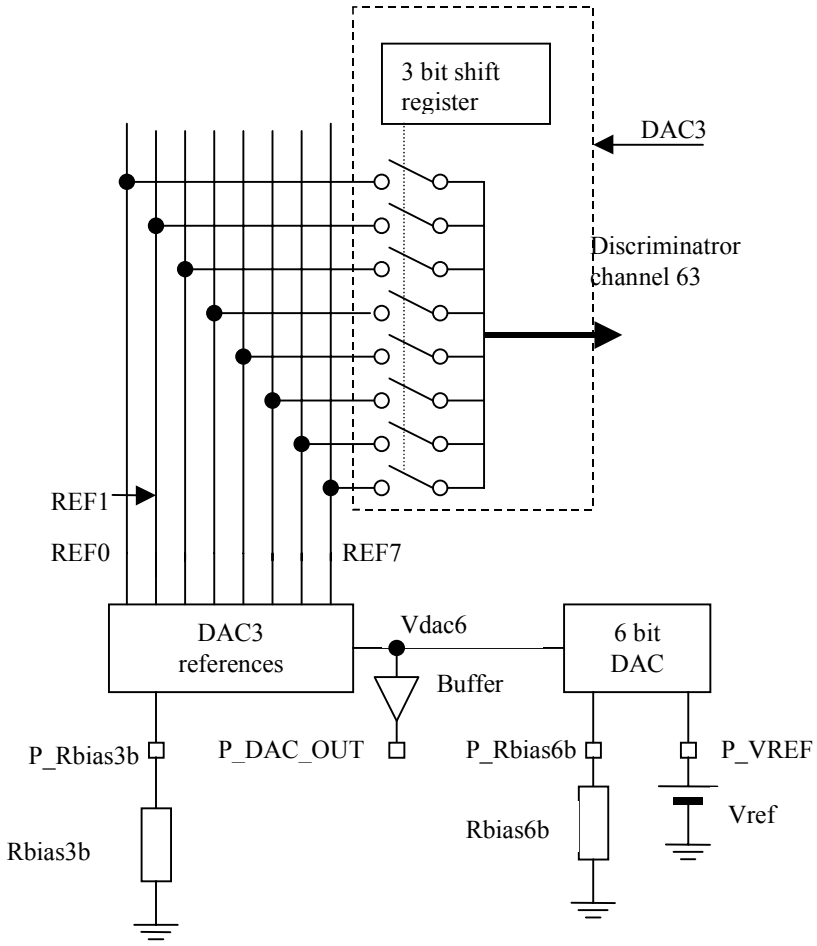

3 bit shift register
DAC3
Discriminatror channel 63
REF1
REF0
REF7
DAC3 references
Vdac6
6 bit DAC
Buffer
P_Rbias3b
P_DAC_OUT
P_Rbias6b
P_VREF
Rbias3b
Rbias6b
Vref

Figure 5

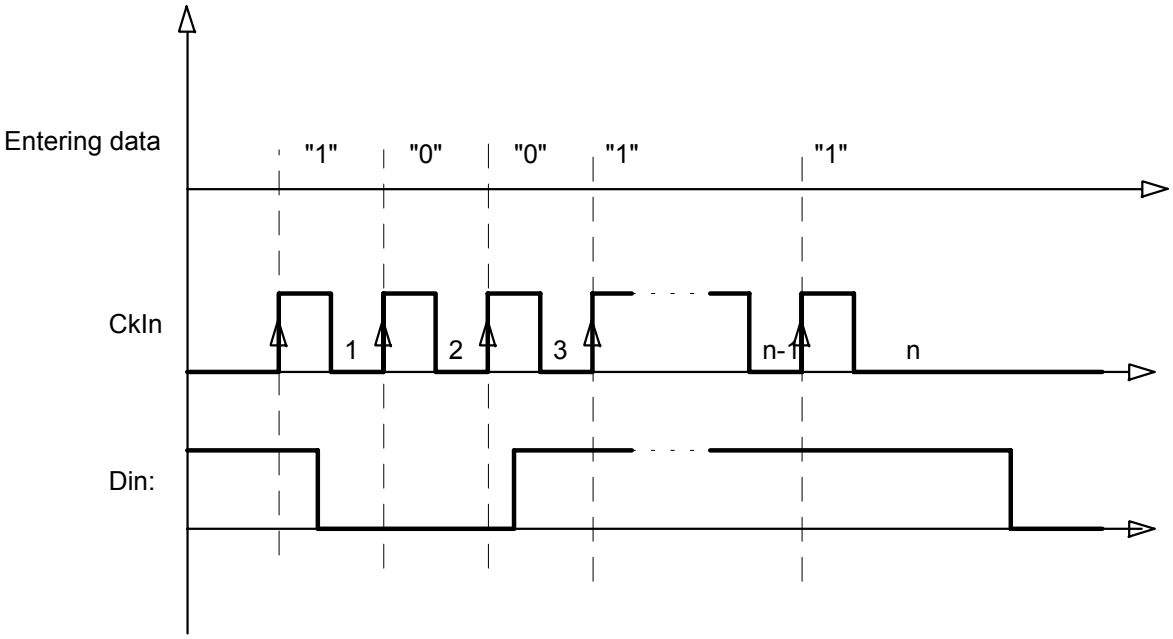


Figure 6

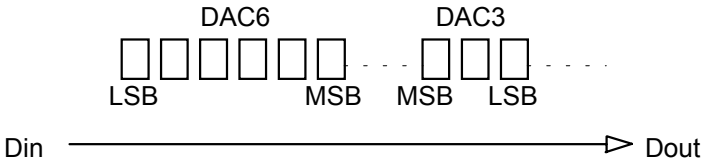


Figure 7

The structure of DAC6 and DAC3 references, and how they are connected together, is shown in Figure 8 . DAC6 is composed by a ladder network whereas DAC3 references are generate by a divider. The currents I0 and I1 set the step and range and are generate by means of two current generator which structure is shown in Figure 9 ; current I is mirrored and divider by a factor 4 to form the current I0 or i1 and its value is set by an internal voltage reference (band gap), of about 1.23 V, and the external resistor values (Rbias3b or Rbias6b). The output voltage range for both DACs is defined by the product of internal resistors and the current flowing in resistors Rbias3b and Rbias6b and can be expressed as:

$$VREF0,VREF1,....,VREF7 = Vdac6+Range\_dac3 / 7* 0,1,.....7,$$

and

$$Vdac6 = Vref + Range\_dac6 /63 * N6 \ , N6=0,1,2, \ldots\ldots 63.$$

where VREF0, ..,VREF7 are the voltage at node REF0,….,REF7 , Range_dac3 and Range_dac6 are the maximum range, for a certain Rbias, for 3 bit and 6 bit DAC respectively.

Resistor R and R1 have the nominal value of 24.12k and 1.25k and a process spread of 16% and 23% respectively.

The external voltage VREF must set to guarantee the signal to be detectable, it can be set equal or lower the analog channel baseline (see table of section 4.6.4).

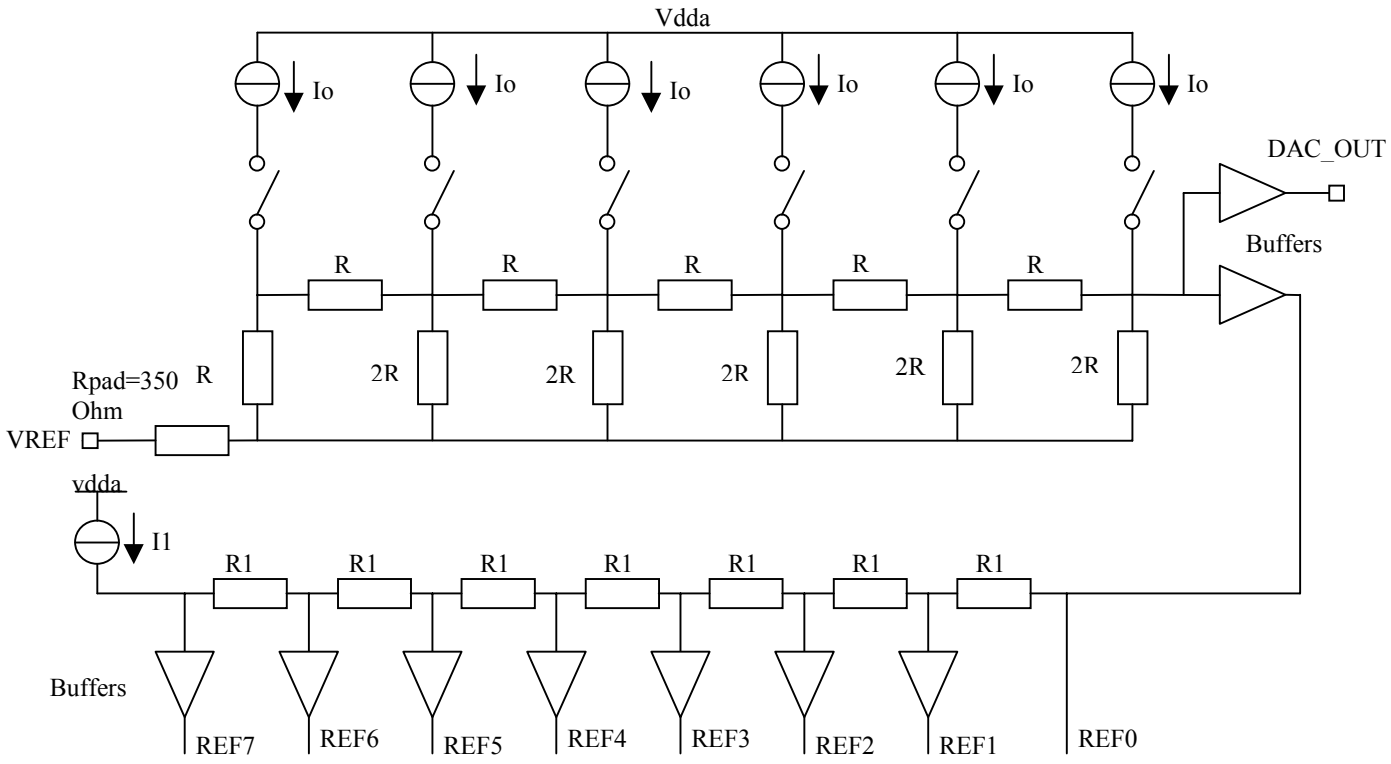


Figure 8

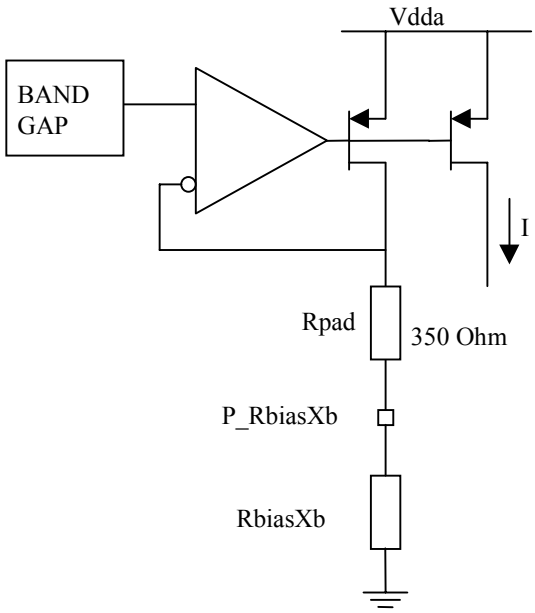


Figure 9

3.5. Calibration

An integrated 200 fF capacitance for each channel can be used for calibration purpose. Pad "Test1" must used to calibrate channel 0 to 31 and pad "Test2" to calibrate channel 32 to 63.

3.6. Digital Section

3.6.1 Digital part features

- 16-bit asynchronous counter ;
- Counter input from comparator (*comp_inp*) , serial (*serial_in*) or common test pin (*common*);
- two bi-directional output signals (*serial_up, ,serial_down*) : *shift_UD* pin selects direction;
- serial readout or counting signal (*shift_count*);
- serial readout clock signal (*shift_clock*);
- fully testable system by means of *test_enable , en_dir* , *shift_clock* and *common* signals;
- overflow signal *ow* (by means of *owpout, owpin, ownor* signals).

3.6.2 Block Diagram

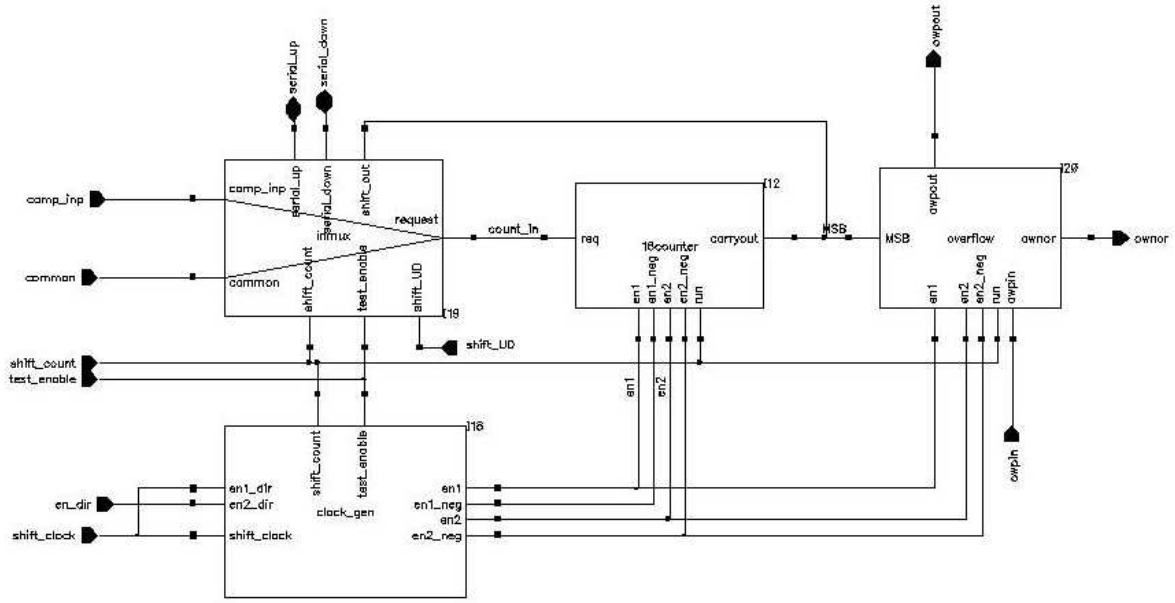
Device block diagram is shown below . The main blocks are:

A) **inmux**; multiplexer to change the input signal of the counter. The *shift_count* and *test_enable* signals allow to select one of the following input: *comp_inp* (counting input), *common* (testing input), *shift_in* (serial input). The signal *shift_in* is connected to *serial_up* or *serial_down* , depending on *shift_UD*.

B) **clock_gen**; this block drives the system in serial readout mode. Internally a four phases clock generator is used.

C) **16counter**; 16 bit asynchronous counter. In counter mode, each cell is an asynchronous toggle flip-flop driven by the previous cell, while in serial reading mode it is a synchronous register controlled by en1, en2 e run signals.

D) **Overflow;** this is the cell that generates the overflow signal and hold it up to the successive reset. It is possible to connect it to other identical devices for a multichannel system.



3.6.3 Functions

The device configuration in the various modes is as follow:

A) reset (o preset)

two ways exists to reset (or preset) the state of the counters : A) activate reading mode (*shift_count* HIGH level and *test_enable* LOW level), put the *serial_in* signal LOW (HIGH for preset) and shift in 16x64 data (16 for one cell); B) put *test_enable*, *shift_count* and *common* signals HIGH (put *common* LOW for the preset), put *en_dir* LOW. In this case the *serial_in* is not necessary but it is mandatory to follow a correct timing

B) counting function

shift_count and *test_enable* signals must be set LOW. If the counter overflows, the *ow signal* (normally HIGH level) goes LOW up to the reset of the counter . The overflow signal is generated by means of a nor gate of the OW signals of each channel: in this way, if, the global ow signals gets LOW if one channel overflows. While in this mode, all changes on *common*, *shift_clock*, *shift_UD*, *en_dir*, *serial_up*, *serial_down* signals have not effect on device.

C) ***reading***

The *shift_count* must be set HIGH (*test_enable* LOW) and the *shift_clock* is the reading clock. The data outputs from MSB to LSB. All changes on *comp_inp and en_dir* have not effect in this mode.

D) test

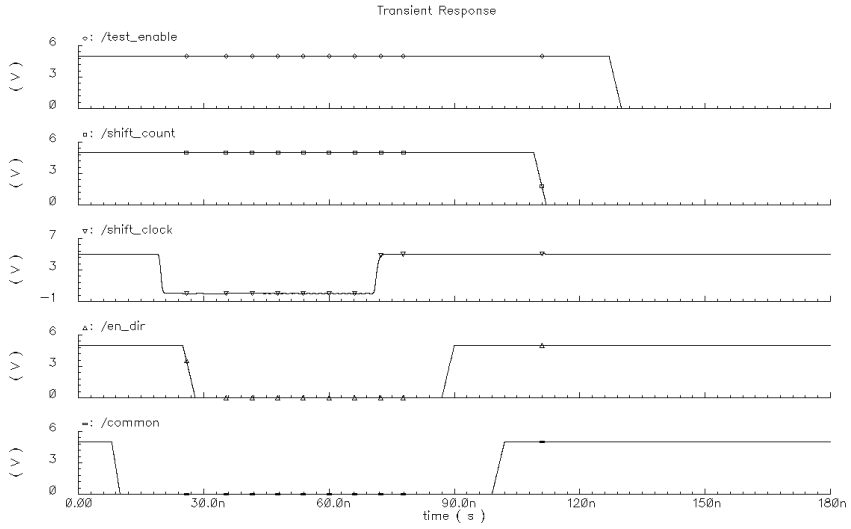
To enter test mode, *test_enable* signal must be set HIGH. The *common* pin is the counter input signal in this mode. In the test mode is possible to test all internal node by means of *en_run*, *shift_clock* and *shift_count* signals.

3.6.4 Timing

The timing follows must be respected for a proper functionality of the chip .

Reset mode

If the reset is made in mode A) the timing is the same as for reading mode, instead in B) mode it is mandatory to follow the following sequence between the *test_enable*, *shift_count*, *en_dir* and *common* signals.



Counting

In this mode the counter is clocked by the *comp_inp* signal. Each comp_inp pulse is counted from device (the pulse is a rectangular wave with LOW initial and final level and HIGH level intermediate). The δI is the minimum length of the pulse whereas the minimum distance between two pulse successive is τc.

Reading

The shift_clock must go HIGH before *shift_count* signal goes HIGH for proper functionality. A single shift for each shift_clock pulse is generated (in this case the pulse is a rectangular wave with HIGH final and initial level and LOW intermediate level). The δsc is the minimum length of the pulse whereas the minimum distance between two pulse successive is f_{max}.

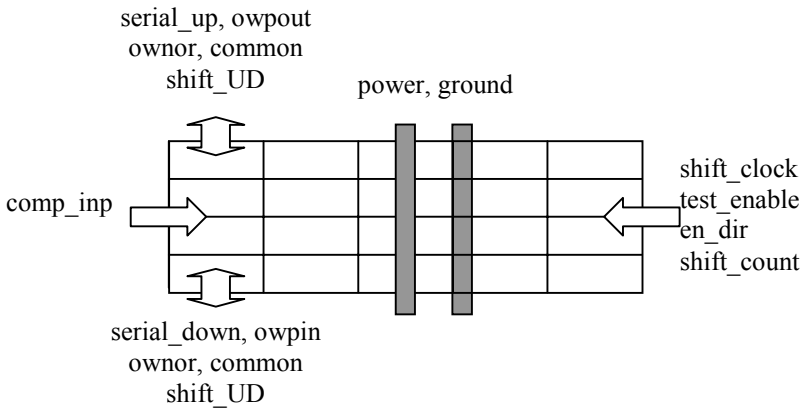
Testing

In this mode the device it's controlled from *en_run*, *shift_clock*, *shift_count* and *common* signals. The internal nodes of the device can be observed by a proper timing of external signals.In particular :

- pulse counting: *shift_count* LOW, the input of the counter is the inverted *common* signal. Then the device counts each common pulse, where pulse is a rectangular waveform with HIGH final and initial level and LOW intermediate level
- counter readout: *shift_count* HIGH level, whereas the clock is replaced from *en_run* and *shift_clock*. There is a shift if we are a *en_run* pulse and subsequently (no superimposes) *shift_clock* pulse .
- Internal node readout .

3.6.5 Layout of the digital part

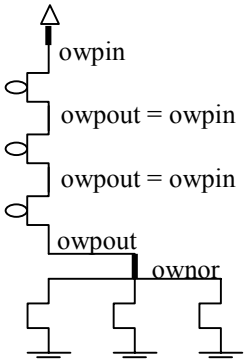
The layout is described below:



The comp_inp is a external signal (from the comparator section in counter mode), the side signals allow to control the device, top and bottom signals are used for serial reading and overflow signalling.

3.6.6 Chip connection

The figure shows how the external overflow signal is generated through the connection of internal nodes of each channel :



- *owpin* signal of the low channel : VDD value ;
- *ownor* and *owpout signals* of the highly channel : connected together ;
- *owpout* signal of the intermediate channel : connected to the *owpin* signal of the channel successive;
- *owpin* of the intermediate channel: connected of the *owpout* of the previously channel;
- ownor of the intermediate channels : connected to the ownor of the previousl and following channel ;

If the *serial_down* and *serial up* pins of different chips are connected together, a single serial readout chain can be implemented.

Note that the *common* pin is the common input of all analogue channels while in test mode.

4 SPECIFICATIONS

3.7. Absolute maximum rating

These are non destructive conditions but normal specification are not guaranteed.

PARAMETER	With respect to	MIN	MAX	Units
POWER SUPPLIES				
vdda	vssa	-0.3	5.1	V
Vddc	vssc	-0.3	5.5	V
vdd	vss	-0.05	0.05	V
INOUT				
DIGITAL INPUTS	vss	-0.3	VDDD+0.3	V
ANALOG INPUTS	vssa,vssc	-0.3	VDDA+0.3	V
DC OUTPUT CURRENTS	vss	-20	20	mA
ANALOG OUT SHORT CIRCUIT CURRENT	vssa vdda	-20	20	mA
TEMPERATURE				
JUNCTION TEMPERATURE			150	°C
CASE TEMPERATURE			100	°C
STORAGE TEMPERATURE		-65	150	°C

3.8. System specification

Specification are given for a typical temperature of 25 °C if not otherwise specified.
All thermal variation are valid for the temperature range from 10 up to 40 °C.

4.6.3 Power Supply

		Min	Typ	Max	Unit
vdda	Supply of analogue section	4.75	5	5.25	V
vddc	Supply of discriminator section	4.75	5	5.25	V
vdd	Supply Supply of analogue section	4.75	5	5.25	V
vssa	ground of analogue section		0		V
vssc	ground of discriminator section		0		V
gnd	ground of digital section		0		V

4.6.4 Analog Section

Some specification are given for two values of the voltage at pin P_Vg , Vg = 0 and –0.2V, that controls the feedback resistance of the charge preamplifier. The other specification are unaffected by this voltage.

Temperature 27 °C , VDDA = 5V ± 5% , VDDD = 5V ± 5%					
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Note**
Total current consumption	82	110	145	mA	(1)
Preamplifier					
Gain Vg = 0V	2.53	3.22	4.20	mV/fC	(2)

Vg = -0.2V	2.50	3.00	3.70		
Risetime Vg = 0V	39	55	105	ns	(2)
Vg = -0.2V	36	46	58		
Falltime Vg = 0V	16	x	x	us	(2)
Vg = -0.2	1.2	2.90	10.3		
Preamplifier and shaper					
Gain	130	170	210	mV/fC	(3)
Gain Spread			±5	%	(4)
Peaking time	200	270	370	ns	(3)
Rise time	93	130	180		
Fall time	375	625	880	ns	(3)
Time spread			±5	%	(3) (4)
Input capacitance			3	pF	(5)
Input dynamic range	0.25		5	fC	
NonLinearity			+/- 1	%	(6)
ENC			850	e-	(3)
Baseline	0.82	0.97	1.11	V	(7)
Counting rate		1		MHz	

(1) This correspond to the total current consumption of the chip if the digital part is not switching.

(2) Gain , rise and fall time are affected by the voltage at pin Vg which controls the preamplifier feedback resistor. For Vg = 0V high fall time can occur up to 1ms.

(3) Input capacitance : 10 pF

(4) Spread for channels of the same chip.

(5) This include preamplifier and pad capacitance.

(6) valid for input charge pulse up to 5 fC; The output buffer doesn't affect the non linearity error.

(7) DC voltage at the shaper output

(8) Min and max can be set changing the appropriate resistor value

4.6.5 Output Buffer

Next table summarize the main characteristics of the output buffer. This buffer does not introduce appreciable distortion in the shaped signal when the capacitive load doesn't exceed 30 pF.

Output Buffer					
Band	10	70	110	MHz	–3db band
Ao	-300	-160	-100	mdB	amplification in DC
Rout	200	340	650	Ohm	output resistance

4.6.6 Discriminator

These specification are valid in the following condition: load 200fF, temperature25°C, power supply 5V; input pulse signal with Trise=250ns, Tf=600nS, min value equal to 1.1V e max value equal to 1.3V. Vth=1.2V.

Parameter	***min***	***typ***	***max***	***unit***	***note***
vddc	4.5	5	5.5	V	Power supply voltage

Temperature	0	25	85	°C	
P_Vg		3.6		V	Bias voltage
Idd	170	320	600	µA	Power supply current
Iis	4	18	50	µA	Max. current ion hysteresis terminal (Vis=5V)
Sigma		0.35		V/ns	Slew-rate rise

Propagation delay*	***min***	***typ***	***max***	***unit***	***note***
rising edge	10	37	60	ns	with Vis=1.6 V
falling edge	8	54	150	ns	with Vis=1.6 V
rising edge		37		ns	with Vis=5 V
falling edge		155		ns	with Vis=5 V
rising edge		37		ns	with Vis floating
falling edge		5		ns	with Vis floating

hysteresis variation (Typ, 25°C, 5V)

The voltage at pin P_vis controls the hysteresis of all the discriminator as indicate in the following table:

Vis (V)	hyst. (mV)
1.4	3.9
1.6	11.2
1.8	19.7
2.0	26.4
2.2	32
2.4	37.7
2.6	40.3
2.8	43
>3.0	44.5

4.6.7 3 bit and 6 bit DACs

To choose of the more appropriate range and step for both DAC3 and DAC6 the next tables helps to identify the values for Rbias3b and Rbias6. Because of the process spread the values in the table are indicative. DAC6 range can be directly measured via pad DAC_OUT.

DAC 6 bit		
Rbias6b (kOhm)	DAC6 range (mV)	DAC6 step (mV)
12	1200	19.0
15	980	15.5
19	780	12.4
23	620	9.8
30	500	7.9
37	400	6.3
47	320	5.1
59	250	3.9
75	200	3.2

DAC 3 bit		
Rbias3b (kOhm)	DAC3 range (mV)	DAC3 step (mV)
7.5	340	48.6
9.5	270	38.6
12	220	31.4
15	175	25
19	140	20
23	110	15.7
30	90	12.8
37	70	10
47	57	8.2

59	45	6.4
75	36	5.1

4.6.8 Thermal drift

Most of the circuit characteristics are not very sensitive to the temperature variation. A table of thermal variation in the range from 10 to 40 °C is given in the next table where Reference temperature Tref is 25 °C.

Parameter	Thermal Drift	Unit	Note
Preamplifier			
Gain	-8.13	uV/°C	(1)
Risetime	+86	ps/°C	(1)
Falltime	-2.3	ns/°C	(1)
Preamplifier and Shaper			
Gain	-0.28	mV/°C	(1)(2)
Peaking time	-0.29	ns/°C	(1)
Rise time	0.0	ns/°C	(1)
Fall time	-0.7	ns/°C	(1)(2)
ENC	+2.3	e^-/°C	(1)
Baseline	-1	mV/°C	
DAC6, Output range drift			
Rbias6b = 75k	+0.25	mV/°C	(3)
Rbias6b = 12k	+1.48	mV/°C	(3)
DAC3, Output range drift			
Rbias6b = 75k	+12.3	uV/°C	(3)
Rbias3b = 7.5k	+142	uV/°C	(3)

Note:

(1) A charge pulse of 5fC has been considered.

(2) The same coefficient is valid at the buffer output

(3) Thermal drift of the external resistor has not been considered

4.6.9 Digital section

Max Counting rate	1	MHz
Max Readout speed	20	MHz

4.6.10 Loads

The given specification are valid if the capacitive load don't exceed the values indicated in the table.

Name	Pin	Type	Description	Max Capacitive Load (PF)
Analog Pads				
DAC_OUT	83	A I/O	6 bit DAC output	50
rbias3b	78	A I/O	DAC3 bias resistor	100
rbias6b	79	A I/O	DAC6 bias resistor	100
BuffOut	114	AO	Channel <0> analogue output	30
Digital Pads				
D_out	106	DO	Stream output to program discriminator section	100p
ck_out	107	DO	Clock output program discriminator section	100p

5 PACKAGED SAMPLES

Sample are housed in CQFP120 package. The pin to pad correspondence and bonding diagram are shown below (n.c. = not connected):

pin	pad	**pin**	pad	**pin**	pad	**pin**	pad
1	P_in<0>	**31**	n.c.	**61**	gnd	**91**	n.c.
2	n.c.	**32**	n.c.	**62**	gnd	**92**	n.c.
3	P_in<1>	**33**	n.c.	**63**	nc	**93**	n.c.
4	vssa	**34**	n.c.	**64**	vdd	**94**	n.c.
5	P_in<4>	**35**	n.c.	**65**	n.c.	**95**	n.c.
6	n.c	**36**	n.c.	**66**	P_Common	**96**	n.c.
7	P_in<5>	**37**	n.c.	**67**	n.c.	**97**	n.c.
8	vssa	**38**	n.c.	**68**	P_ShiftUD	**98**	n.c.
9	P_in<12>	**39**	P_Test2	**69**	n.c.	**99**	vdd
10	n.c.	**40**	vssa	**70**	gnd	**100**	SerialUP
11	P_in<13>	**41**	vdda	**71**	n.c.	**101**	P_Dout
12	vssa	**42**	vssa	**72**	vdd	**102**	P_CkOut
13	P_in<20>	**43**	vdda	**73**	n.c.	**103**	vddc
14	n.c	**44**	P_Rbias3b	**74**	P_ShiftCount	**104**	vssc
15	P_in<21>	**45**	P_Rbias6b	**75**	n.c.	**105**	P_Vg
16	vssa	**46**	P_Vis	**76**	n.c.	**106**	P_Gate
17	vssa	**47**	P_VREF	**77**	P_TestEnable	**107**	vdda
18	P_in<36>	**48**	vssc	**78**	n.c.	**108**	vssa
19	n.c.	**49**	P_DAC_OUT	**79**	gnd	**109**	P_BuffOut
20	P_in<37>	**50**	vddc	**80**	n.c.	**110**	vdda
21	vssa	**51**	P_Din	**81**	vdd	**111**	vssa
22	P_in<44>	**52**	P_CkIn	**82**	n.c.	**112**	P_Test1
23	n.c.	**53**	SerialDown	**83**	P_ShiftClock	**113**	n.c.
24	P_in<45>	**54**	n.c.	**84**	n.c.	**114**	n.c.
25	vssa	**55**	n.c.	**85**	P_EnDir	**115**	n.c.
26	P_in<52>	**56**	n.c.	**86**	n.c.	**116**	n.c.
27	n.c.	**57**	n.c.	**87**	gnd	**117**	n.c.
28	P_in<53>	**58**	n.c.	**88**	n.c.	**118**	n.c.
29	vssa	**59**	n.c.	**89**	vdd	**119**	n.c.
30	P_in<63>	**60**	n.c.	**90**	P_OW	**120**	(ground)

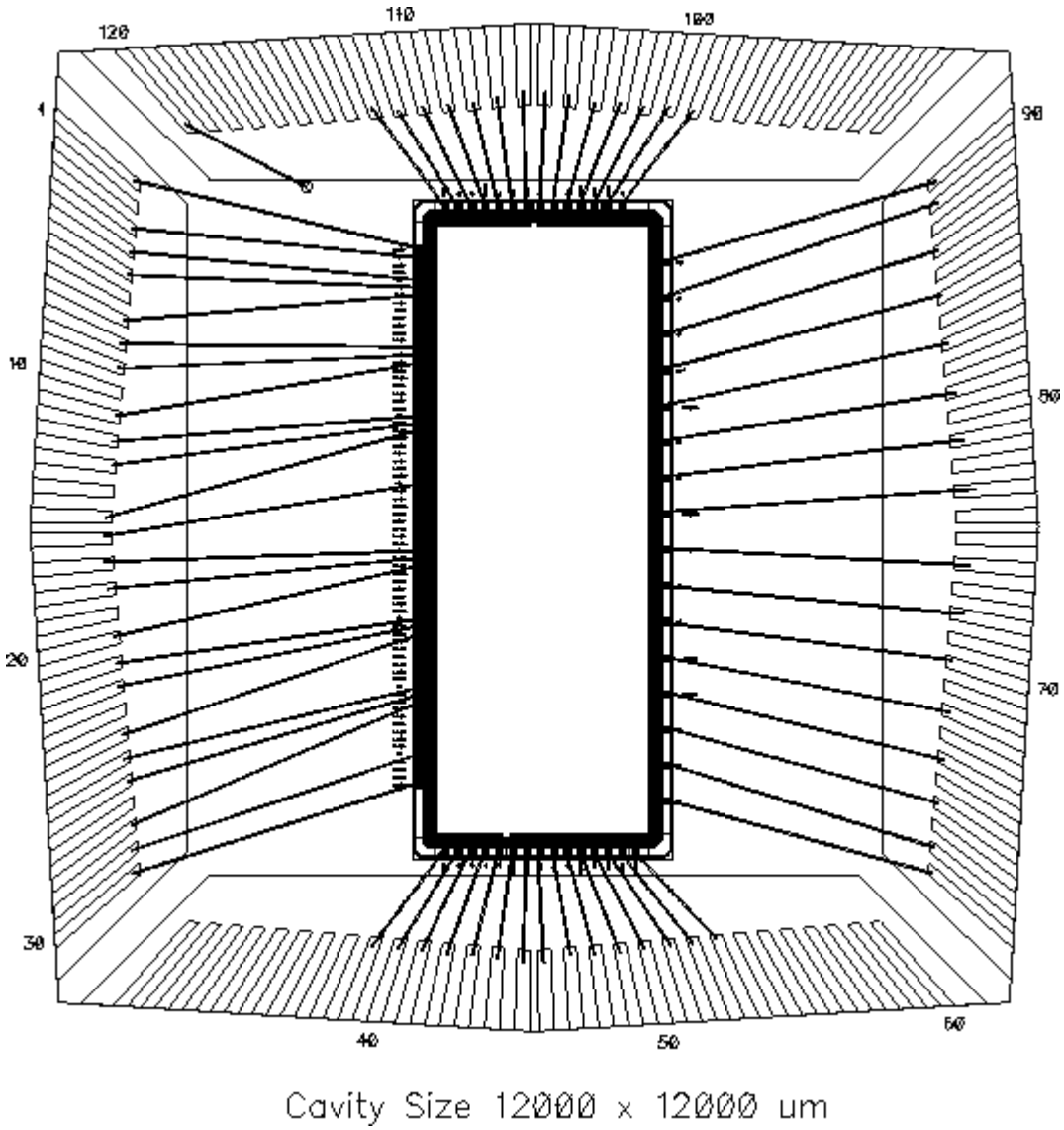

110
120
100
1
90
10
80
20
70
30
40
50
60
Cavity Size 12000 x 12000 um

Figure 10

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