Features

- Up to 6,272 Logic Cells
- Patented Active Repeater™ Architecture
- 5 x 7 Routing Region - Access 35 Logic Blocks With No Repeaters, 117 Blocks With 1 Repeater
- 4-bit Carry Routing For Wide, Fast MUX, AND/OR, XOR, Counters and Arithmetic logic
- Supports Four 66MHz, 64-Bit, Zero-Wait-State PCI Soft Cores for PCI Bridges
- I/O Data-Transfer Rates up to 250MHz
- 21 Selectable I/O Levels Including TTL, CMOS, GTL, GTLP, AGTLP, AGP, CTT, HSTL and SSTL I/O Levels
- LVDS and LV-PECL Inputs
- Differential I/O
- Registered Output Enable in Every I/O
- 32-Bit Dual-Port SRAM in Every Logic Block With Sub-6ns Access
- Two On-Chip PLLs
  - 8 to 200MHz Range
  - Programmable Latency in 80ps Steps
  - Clock Multiplication and Division by 2, 3, 4, 6 and 8
  - Lock Indicators
  - External Feedback for System-Level Clock Generation
- Ten Low-Skew Clock Trees
- SRAM-Based In-System Reprogrammable
- Dynamic Single-Block Reconfigurability
- 2.5 V Core with Multiple-Voltage Selectable I/O (5V-Tolerant)
- Hot-Swappable
- JTAG Programming and Boundary-Scan (IEEE1149.1)

Applications Examples

- Gigabit Ethernet
- ATM
- Fibre Channel
- Frame Relay
- SONET
- High-Speed Image Processing
- Servers and Supercomputers
- PCI Bridges
- Semiconductor Testers
- ASIC Emulation
- On-the-Fly-Reconfigurable Systems

Device	Logic Cells	Gates	Logic Blocks	Max Dual-Port SRAM Bits	Flip- flops	I/O Blocks
DY8105	6,272	105,000	3,136	100,352	7,168	404
DY8080	4,608	80,000	2,304	73,728	5,376	362
DY8055	3,200	55,000	1,600	51,200	3,840	320
DY8035	2,048	35,000	1,024	32,768	2,560	256
DY8020	1,152	20,000	576	18,432	1,536	192

Table 1: DY8000 Family

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DY8000 Enhancements

The DY8000 family incorporates numerous improvements:

- Higher Density
  - Up to 6,272 Logic Cells, 105,000 Usable Gates
- Higher Speed
  - Faster Process (.25 micron)
  - Larger Routing Region
    - 5 columns by 7 rows
  - 4-bit Carry Routing
    - Wide, Fast MUX, AND/OR, XOR, Counter and Arithmetic Logic
  - Sub 6ns SRAM Access Time
- Supports 4, 64-bit, 66MHz PCI Soft Cores for Bridge Applications
- 21 Programmable I/O Levels
  - LV-TTL
  - LV-CMOS
  - LV-CMOS2 (2.5 volt)
  - LV-CMOS1 (1.5 volt)
  - GTL
  - GTL2 (2.5 volt)
  - GLTP
  - GTLP2 (2.5 volt)
  - AGTLP
  - SSTL Class 2 Level 1
  - SSTL Class 2 Level 2
  - SSTL Class 3 Level 1
  - SSTL Class 3 Level 2
  - HSTL Class I
  - HSTL Class III
  - HSTL Class IV
  - AGP
  - CTT
  - LV-PECL - Inputs Only
  - LV-PECL2 (2.5 volt) - Inputs Only
  - LVDS - Inputs Only
- Differential I/O Capability on Adjacent I/O
- 4 Global External I/O References
- 2 Internal I/O References
  - LV-PECL and GTL
- Additional Flip Flop in Every I/O for Registered OE
- Selectable Global and Local OE Routing
- JTAG Programming

High-Performance Active Repeater Technology

Active Repeater Routing, illustrated in Figure 2, is the enabling technology behind DynaChip's patented Fast Field Programmable Gate Arrays.

Conventional FPGA devices use pass gates to create programmable interconnections. When using multiple pass gates to create a net, they act like series resistors with distributed capacitance to ground, as shown in Figure 1. Nets formed as a series of these pass gates slow down dramatically as the number of programmable connections increases, resulting in long, unpredictable delays, especially for those nets which must traverse a long physical distance or drive a large number of loads.

In contrast, DynaChip DY8000-family devices use Active Repeaters to create programmable interconnections. As shown in Figure 2, these repeaters buffer the signal at every interconnection point and isolate the capacitance of the rest of the net.

The result is fast, predictable performance even for long, high-fanout nets.

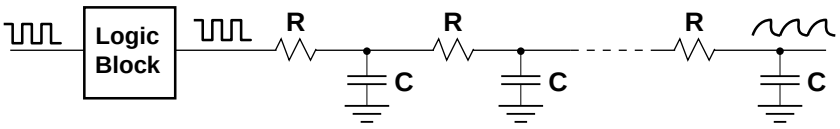


Figure 1: Pass Gates in Series Delay and Degrade Signals

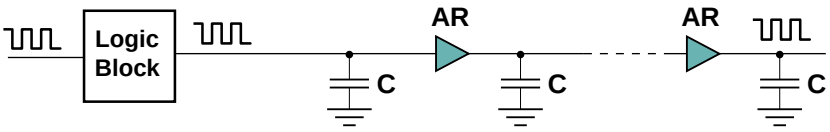


Figure 2: DynaChip's Active Repeaters Build Fast, Predictable Interconnect

Figure 3 illustrates a comparison of net delays between the two circuit technologies as the number of programmable interconnection points grows.

In FPGA devices using pass gate-based interconnect, net delays increase quadratically with the number of interconnection points, resulting in performance bottlenecks for long and/or heavily-loaded nets.

Conversely, using Active Repeater interconnect produces net delays which increase only linearly with the number of interconnection points, and are not affected by increased fanout, resulting in higher performance and superior predictability.

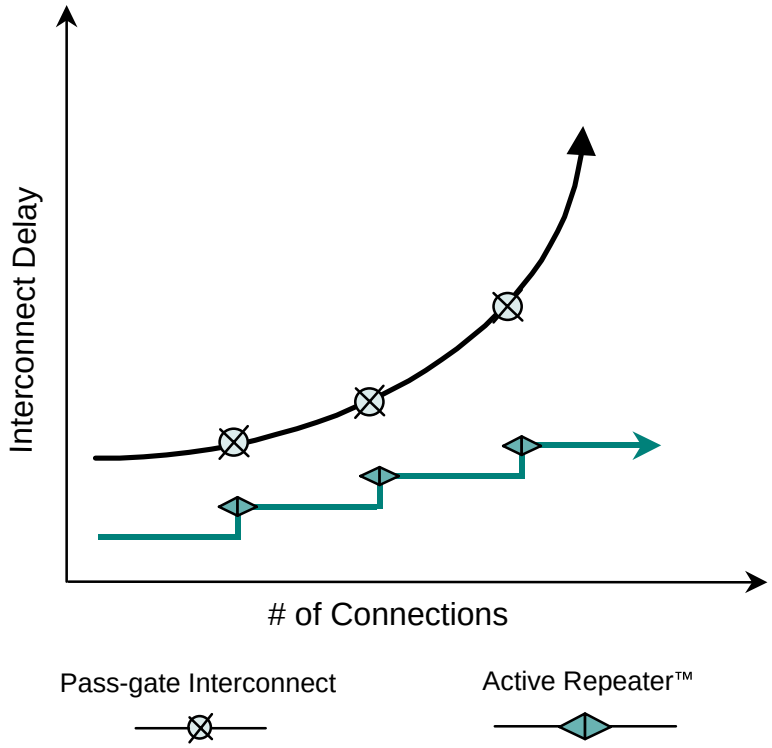


Figure 3: Active Repeater™ vs. Pass Gate Delays

Top-Level Architecture

Figure 4 illustrates the architecture common to all DY8000 family devices, but for a reduced number of blocks. A border of I/O blocks forms the outer perimeter of the device. A rectangular array of logic blocks occupies the device's interior. The spaces between these logic blocks form channels, which are filled by horizontal and vertical routing tracks.

The structure of the individual DY8000 routing tracks is entirely different from the corresponding structures in conventional FPGAs. The illustrations in Figure 1, Figure 2, and Figure 3 emphasize the effect of these differences. Using Active Repeaters eliminates the need for numerous levels of routing tracks of varying lengths, resulting in more predictable convergence to optimized solutions.

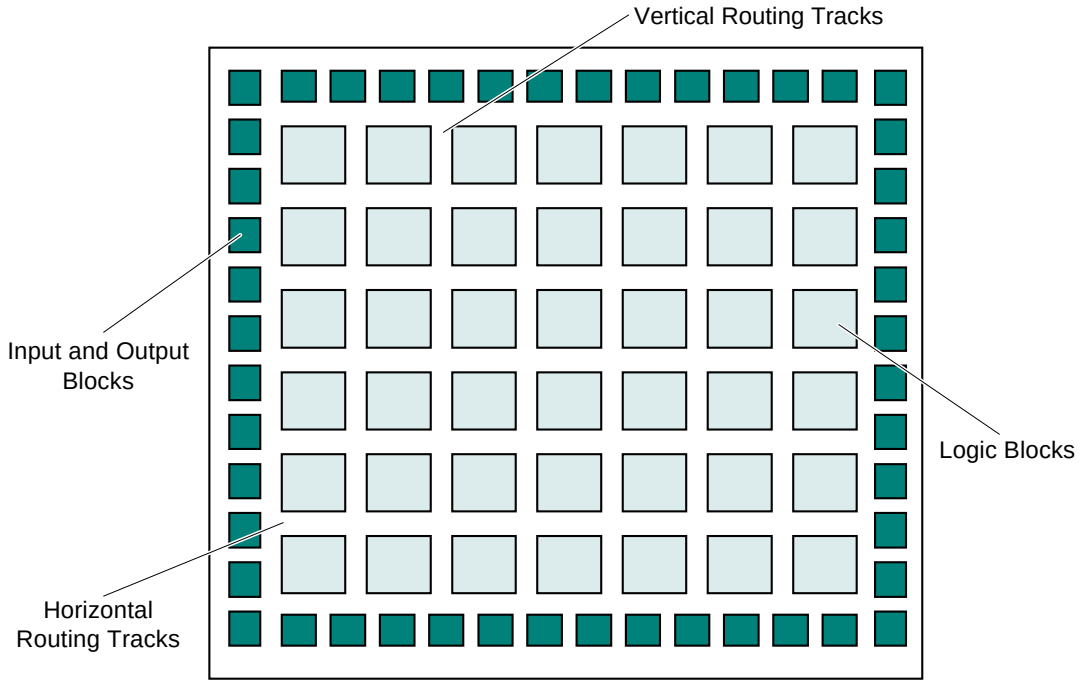


Figure 4: Overview of DY8000 Architecture

Routing Architecture

Dynachip's Active Repeater technology provides higher performance than more complex multi-level routing architectures.

As shown in Figure 5, a routing region consists of logic blocks and a set of horizontal and vertical routing tracks, interconnected by buffers controlled by programmable configuration SRAM bits. All routing is programmed by selecting which of these buffers to turn on; there are no pass gates or other passive routing types.

Active Repeater buffers drive fixed loads and are optimized for those loads. As a result, their logic delays are fixed and the performance of large complex user designs is determinate and predictable. There are four types of Active Repeater buffers:

- Horizontal (Horizontal-to-Horizontal Bidirectional Buffers)
- Vertical (Vertical-to-Vertical Bidirectional Buffers)
- Vertical-to-Horizontal Connection Buffers
- Horizontal-to-Vertical Connection Buffers

As shown in Figure 5, each DY8000 logic block has its own 35-block local routing region; 5 columns wide by 7 rows high. The Active Repeaters are staggered so that every block has an associated routing region, which overlaps the routing regions of nearby blocks.

Routing regions are connected via bidirectional Active Repeater buffers. A signal which has passed through an Active Repeater is available throughout the next routing region.

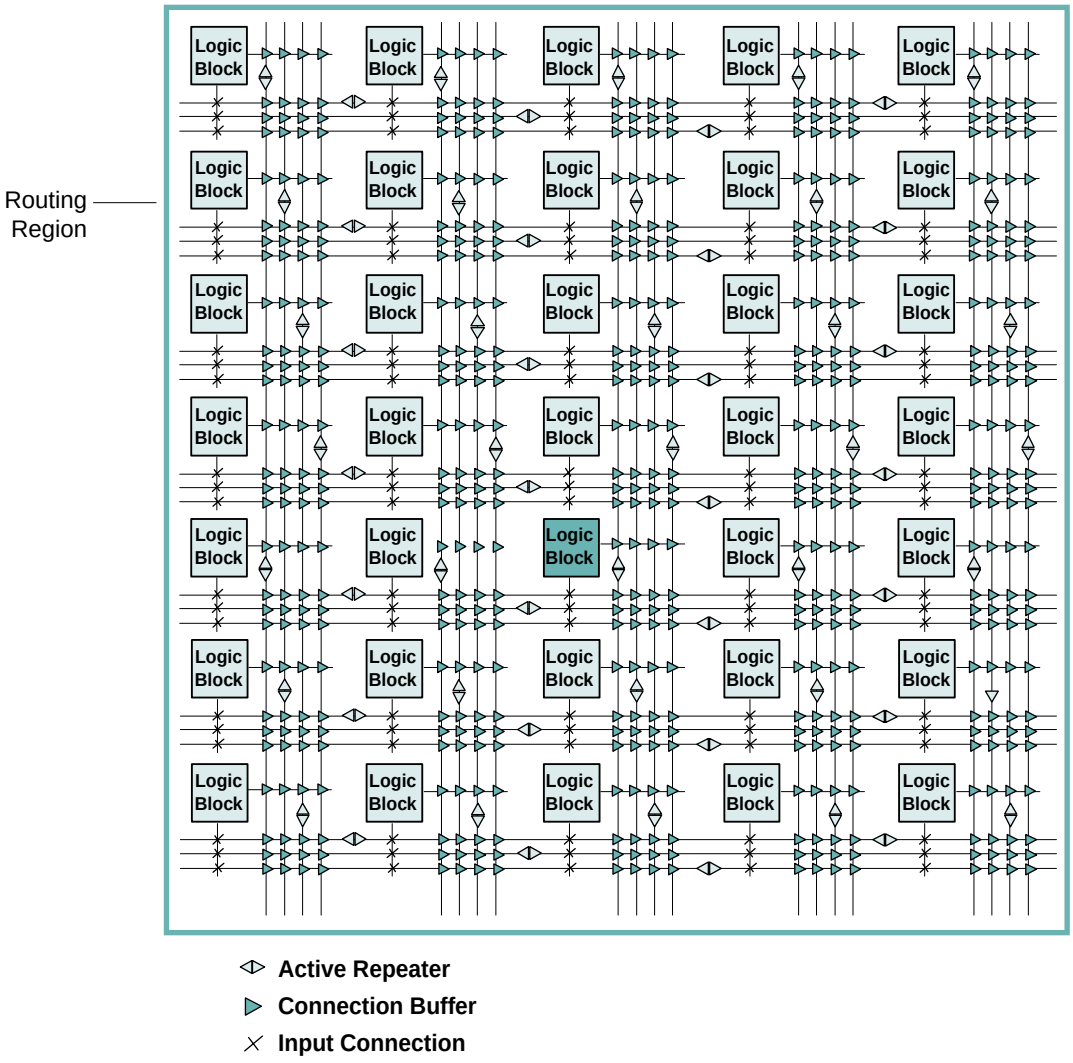


Figure 5: Routing Architecture

The 5 x 7 routing regions allow a logic block to drive up to 35 blocks with zero repeaters and no additional routing delays. As shown in Figure 6, adding a single repeater delay allows a logic block to drive up to 117 blocks with a routing delay of only 500ps. With 2 repeater delays a logic block can drive 247 blocks. Since every interconnect is fully buffered, repeater delays are additive and the resulting 2 repeater net has a delay of only 1.0ns. This enables even high fanout nets to have extremely high performance.

The DY8000 AC parameters presented in Table 19 allow designers to accurately estimate performance because they include all connection buffer delays and other routing delays within the logic block's 5x7 routing region. The DY8000 parameters presented in Table 20 show logic block delays without any connection buffer or routing delays and are useful for comparing the DY8000 to other FPGA technologies.

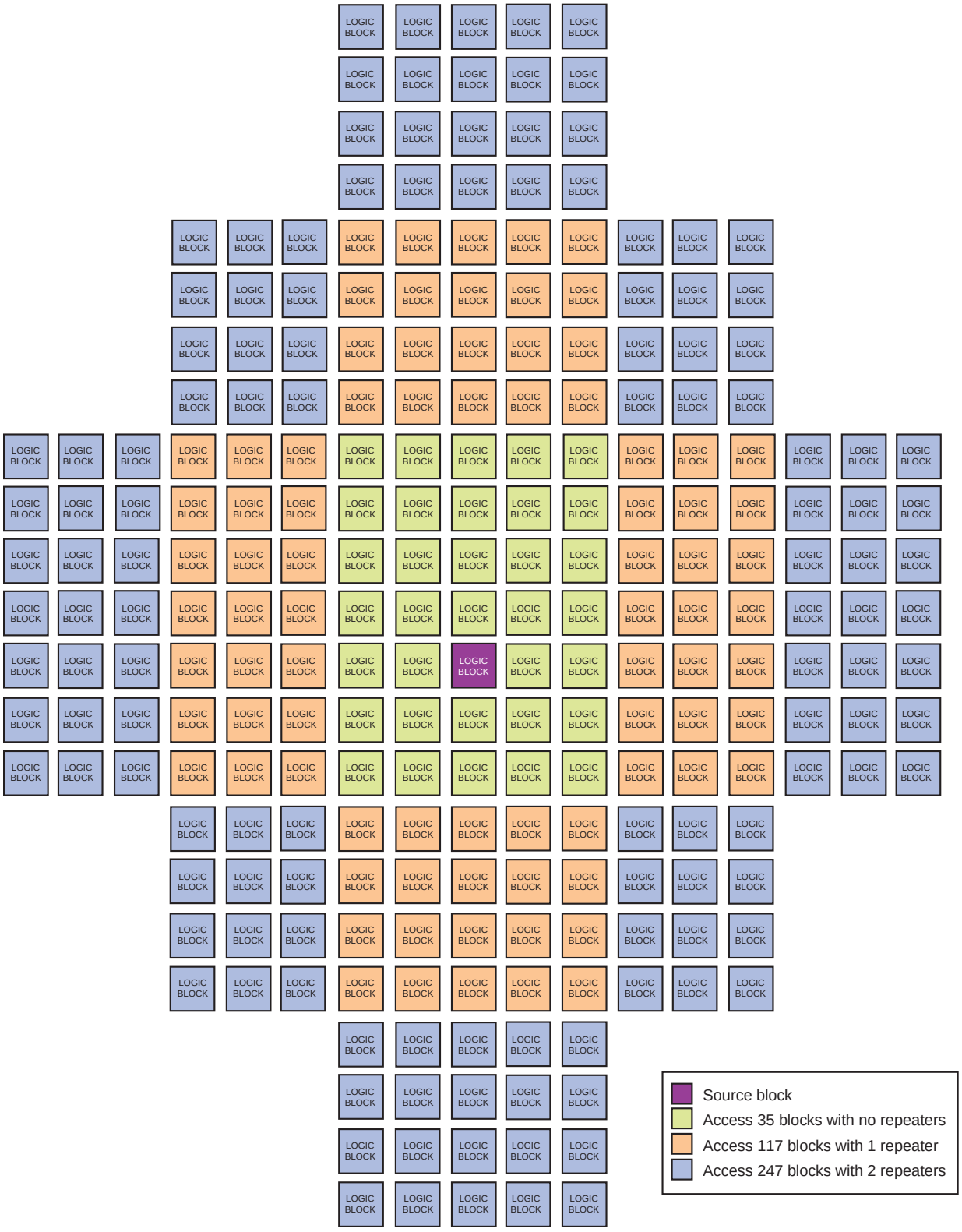


Figure 6: Routing Region With No Interconnect Delay

For a signal driving a block or blocks within the next region, the fixed delay through one Active Repeater is added to the logic block delay. Thereafter, an additional Active Repeater delay is added for every 3 columns or 4 rows the signal traverses.

Active Repeater delays are the only routing delays in a DY8000 device. Active Repeaters performance values are given in Table 23 at the end of this data sheet.

Each logic block typically implements twenty logic gates or thirty-two SRAM bits. The total logic and memory resources which may be reached with 0, 1, or 2 Active Repeater delays are shown in Table 2.

Active Repeater Delays	Logic Blocks	Gates	SRAM Bits
0	35	700	1,120
1	117	2,340	3,744
2	247	4,940	8,151

Table 2: Accessing Neighboring Logic Blocks

Input/Output Blocks

DY8000 I/O block structure is illustrated in Figure 7. Each I/O block includes an input flip-flop, an output flip-flop and an OE flip-flop. Each I/O block includes JTAG Boundary Scan logic, conformant to the IEEE 1149.1 Specification.

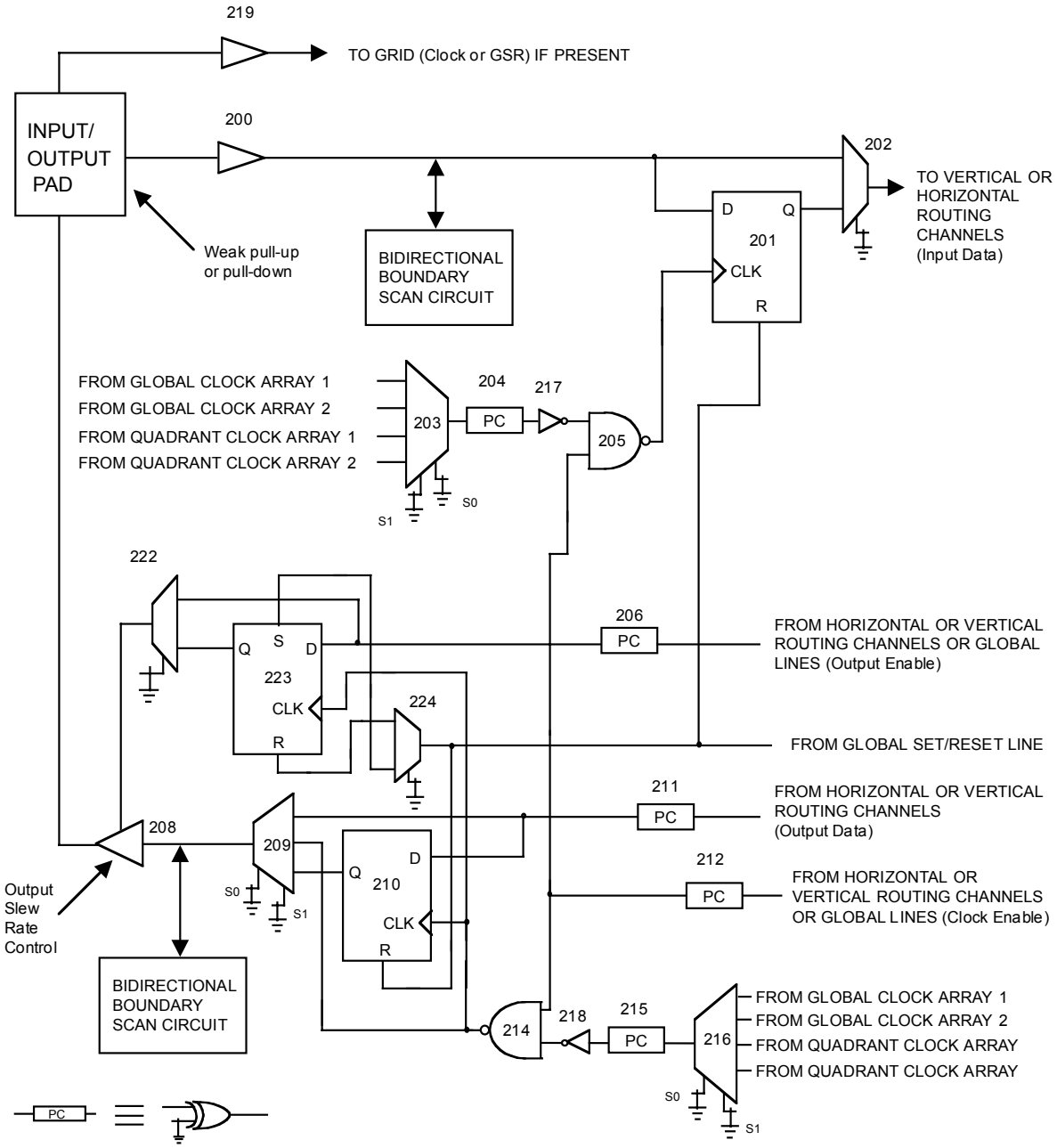


Figure 7: Input/Output Block

Note:

The numbers within the logic symbols are used by DynaTool to identify particular logic elements.

Every I/O can be programmed to any of the following levels.

- AGP
- AGTLP
- CTT
- GTL
- GTL2 (2.5 volt)
- GLTP
- GTLP2 (2.5 volt)
- HSTL Class I
- HSTL Class III
- HSTL Class IV
- LV-CMOS
- LV-CMOS1 (1.5 volt)
- LV-CMOS2 (2.5 volt)
- LVDS (inputs only)
- LV-PECL (inputs only)
- LV-PECL2 (2.5 volt) inputs only
- LV-TTL
- SSTL Class 2 Level 1
- SSTL Class 2 Level 2
- SSTL Class 3 Level 1
- SSTL Class 3 Level 2

When programmed to LVDS, LV-PECL or LV-PECL2 levels, the I/O can be used only as inputs.

Adjacent I/O can be configured as a differential pair. Differential signaling can be used with any of the supported I/O levels.

External Reference Voltage

The DY8000 I/O blocks can use external reference voltages. Up to 4 external reference voltages can be applied. Any I/O block may be programmed to use any of the four externally-supplied reference voltages. Recommended reference voltages for supported I/O levels are shown in Table 3.

Required Compatibility	Reference Voltage
GTL	0.8V ± 5%
GTLP	1.0V ± 5%
LV-PECL, LV-PECL2	(V_{CC} - 1.3V) ± 5%
AGP	1.30
CTT	1.50
HSTL I	.75
HSTL III	.90
HSTL IV, AGTLP	.90
SSTL3 I	1.50
SSTL3 II	1.50
SSTL2 I	1.25
SSTL2 II	1.25

Table 3: Recommended Settings for Reference-Voltage Input

Using an external reference voltage is mandatory for GTLP, AGTLP, HSTL, SSTL, CTT, LV-PECL2, LV-CMOS2 and AGP, and optional for GTL and LV-PECL. If the external reference voltage is not used for GTL and LV-PECL, internal voltage reference is provided. LV-TTL and LV-CMOS always use an internal reference.

Mixing Different I/O Levels

Input reference voltages are selectable on a pin-by-pin basis allowing the user to mix input levels with no limitations.

Output level selectability is determined by V_{CCO} settings which are applied on an I/O group basis. A group consists of all the I/O contained within a half side of the device. Up to 8 different groups are available. The following table shows input and output levels that can be mixed within a group and the required V_{CCO} setting.

V_{CCO} Setting	3.3V	2.5V	1.5V
Supported Output Levels	AGP GTL GTLP LV-TTL LV-CMOS CTT SSTL Class 3 Level 1 SSTL Class 3 Level 2	GTL GTL2 GTLP GTLP2 LV-CMOS2 SSTL Class 2 Level 1 SSTL Class 2 Level 2	AGTLP GTL GTL2 GTLP GTLP2 HSTL Class 1 HSTL Class III HSTL Class IV LV-CMOS1
Supported Input Levels	AGP AGTLP CTT GTL GTL2 GTLP GTLP2 HSTL Class 1 HSTL Class III HSTL Class IV LV-CMOS LV-CMOS1 LV-CMOS2 LV-TTL LV-PECL LV-PECL2 LVDS SSTL Class 2 Level 1 SSTL Class 2 Level 2 SSTL Class 3 Level 1 SSTL Class 3 Level 2	AGP AGTLP CTT GTL GTL2 GTLP GTLP2 HSTL Class 1 HSTL Class III HSTL Class IV LV-CMOS LV-CMOS1 LV-CMOS2 LV-TTL LV-PECL LV-PECL2 LVDS SSTL Class 2 Level 1 SSTL Class 2 Level 2 SSTL Class 3 Level 1 SSTL Class 3 Level 2	AGP AGTLP CTT GTL GTL2 GTLP GTLP2 HSTL Class 1 HSTL Class III HSTL Class IV LV-CMOS LV-CMOS1 LV-CMOS2 LV-TTL LV-PECL LV-PECL2 LVDS SSTL Class 2 Level 1 SSTL Class 2 Level 2 SSTL Class 3 Level 1 SSTL Class 3 Level 2

Table 4: I/O Levels for V_{CCO} Settings

Logic Blocks

The DY8000 Logic Block, simplified in Figure 8, and shown fully in Figure 9, contains AND, OR, and XOR gates, flip-flops, muxes, and a 32-bit, two-clock, two-port SRAM, making this block versatile and powerful. DynaTool™ (DynaChip's development system) automatically maps logic from the designer's application into these logic block resources.

One logic block may implement a two-bit full adder or identity comparator, a nine-input AND gate, a seven-input XOR parity tree, an 8:1 multiplexer, and other logic functions of comparable complexity.

The logic block includes sixteen general purpose logic inputs, plus Clock and Set/Reset inputs. All inputs are equipped with polarity control circuits, which may be programmed to pass their signals either as noninverted (true) or as inverted (false). There are also two Global Clock Inputs, two Quadrant Clock Inputs, a Global Set/Reset Input, and 4 carry signals.

There are three logic outputs that may be driven by the logic blocks' combinatorial logic, its flip-flops, or its SRAM. Two of the logic outputs can be direct or registered. The third output is always direct.

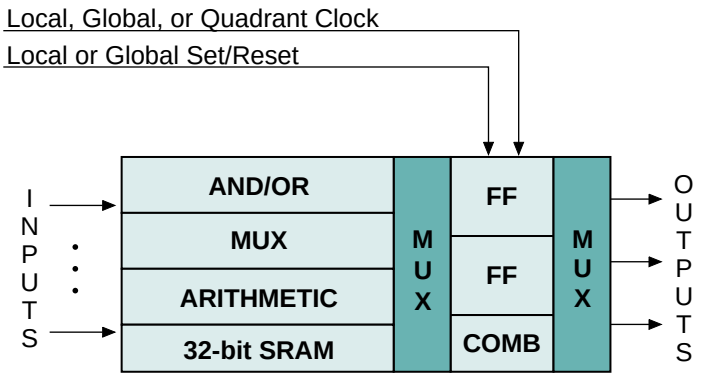


Figure 8: Conceptual Diagram of Logic Block

The functional areas shown in Figure 8 are the AND/OR logic section, multiplexer section, arithmetic logic section, and the thirty two-bit, two-clock, two-port SRAM section.

Each block includes two flip-flops that are configurable to either a D-type or T-type element. Both flip-flops are clocked from one of five sources (local clock (LCLK)), two global clocks (GCLK1 or GCLK2), or two quadrant clocks (QCLK1 or QCLK2), which serve this region. Flip-flops can be programmed to be active on either the rising or the falling clock edge.

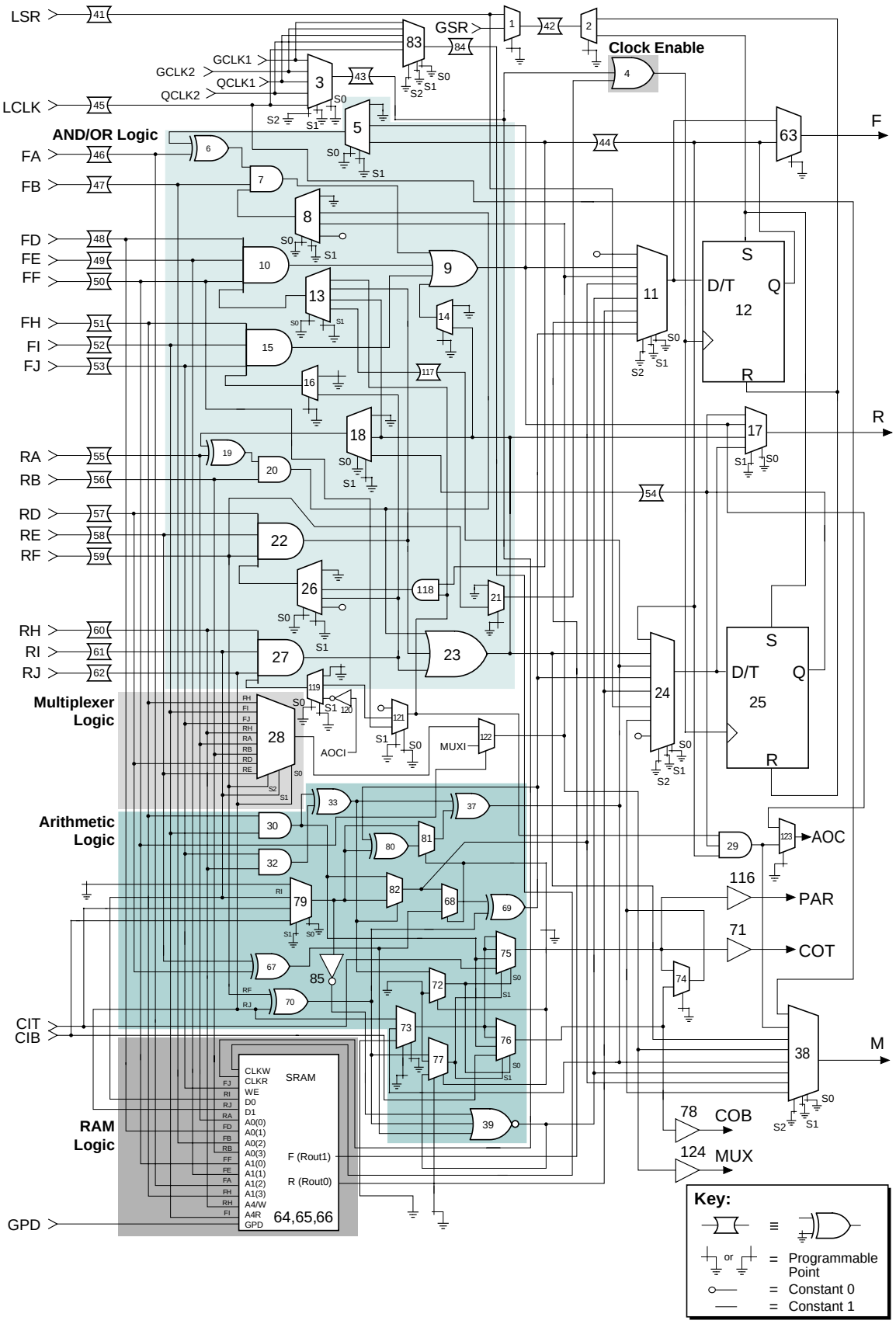


Figure 9: Schematic Diagram of DY8105 Logic Block

The two flip-flops share a common set/reset signal from either of two sources: local interconnect (LSR), or the FPGA's global set/reset (GSR). The set/reset input has programmable polarity control. You may choose assertive-HIGH operation or assertive-LOW operation for resetting the two flip-flops, although your choice must be the same for both. Likewise, you may configure the two flip-flops together to use either a set operation or a reset operation.

SRAM

Each logic block in a DY8000-family FPGA includes 32 bits of fully-synchronous dual-port, two-clock SRAM with three configuration options:

- One 32x1 two-port SRAM.
- One 32x1 single-port SRAM.
- Two separate 16x1 single-port SRAMs.

Functional block diagrams corresponding to each of these configurations are shown in Figure 10, Figure 11, and Figure 12. All signals are one-bit except for addresses, which are five-bit for the two 32x1 configurations, and four-bit for the double-16x1 configuration.

The SRAM has separate read and write clocks. Either of these clocks may originate from any of five sources: local interconnect (LCLK), either of the FPGA's two global clocks (GCLK1 or GCLK2), or either of the FPGA's two quadrant clocks (QCLK1 or QCLK2) serving that region of the chip. For the two single-port configurations, the write clock and the read clock are automatically tied together.

For any of the three SRAM configurations, both writing and reading are synchronous operations.

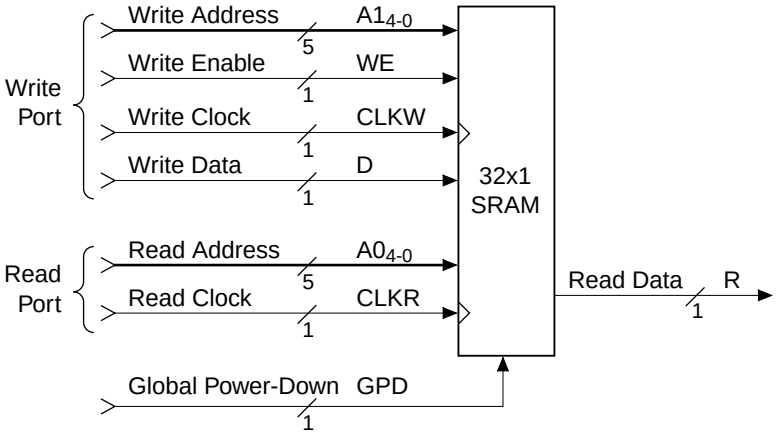


Figure 10: 32x1 Two-Port SRAM

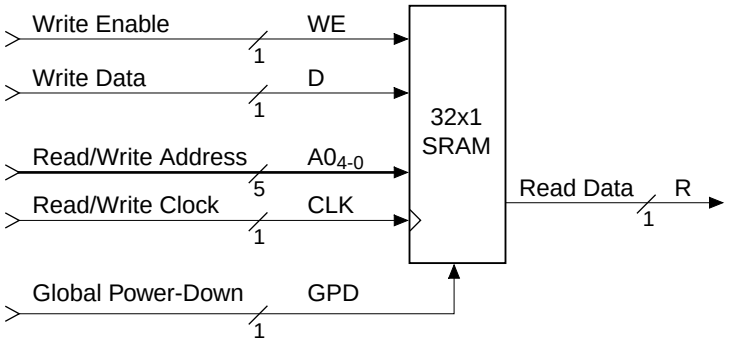


Figure 11: 32x1 Single-Port SRAM

On a rising edge (a LOW-to-HIGH transition) of the write clock, the WE, address, and data inputs are latched. If WE is HIGH, the data is written to the RAM in the same clock cycle. Writing is a single-clock operation. While a write operation is in progress, the state of the SRAM's data output(s) is indeterminate.

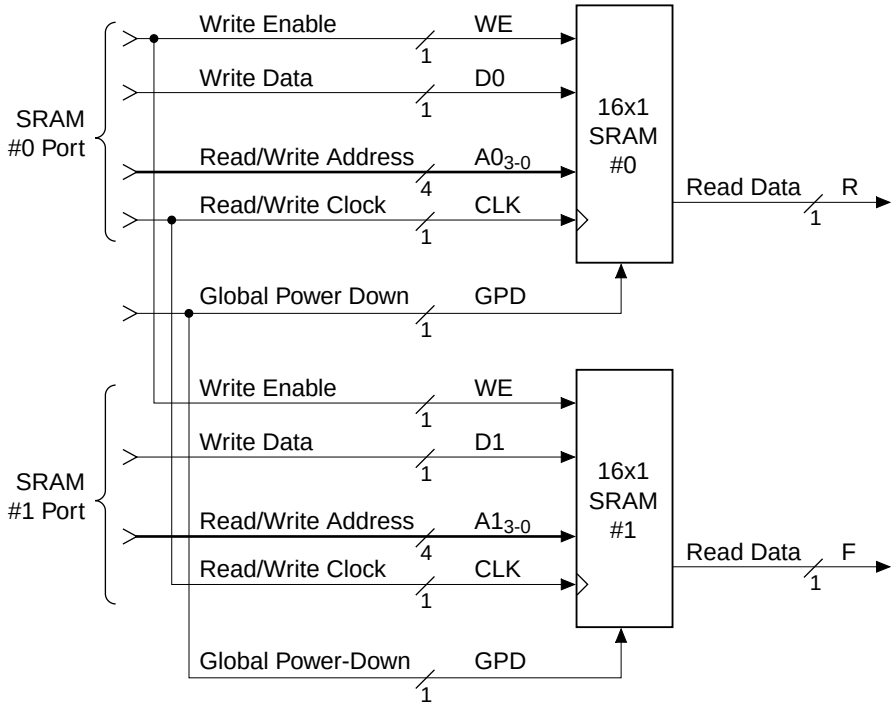


Figure 12: Two Separate 16x1 Single-Port SRAMs

On a rising edge of the read clock, the RAM outputs are latched and are available at the RAM output(s). Reading is a single-clock operation.

The two-port SRAM configuration has a separate write port and read port, with separate read address and clock signals. Single-port configurations have common read/write clocks and addresses.

For two single-port configurations, SRAM is in write mode whenever WE is asserted and in read mode whenever WE is not asserted.

For two-port configurations, the SRAM is always in read mode regardless of the state of WE, except when a read-write collision occurs; that is, when an attempt is made to read and write the same location at the same time. In this case, writing takes precedence over reading, and the data output is indeterminate.

Timing waveforms for the SRAM write and read operations are shown in Figure 13, Figure 14, and Figure 15. Figure 13 and Figure 14 apply to the 32x1 two-port configuration. Figure 13 is for the common case where the write and read addresses are not the same, and Figure 14 applies to the 'read-write collision' case where the addresses are the same. Figure 15 applies to both the 32x1 single-port configuration and the two-16x1 single-port configuration.

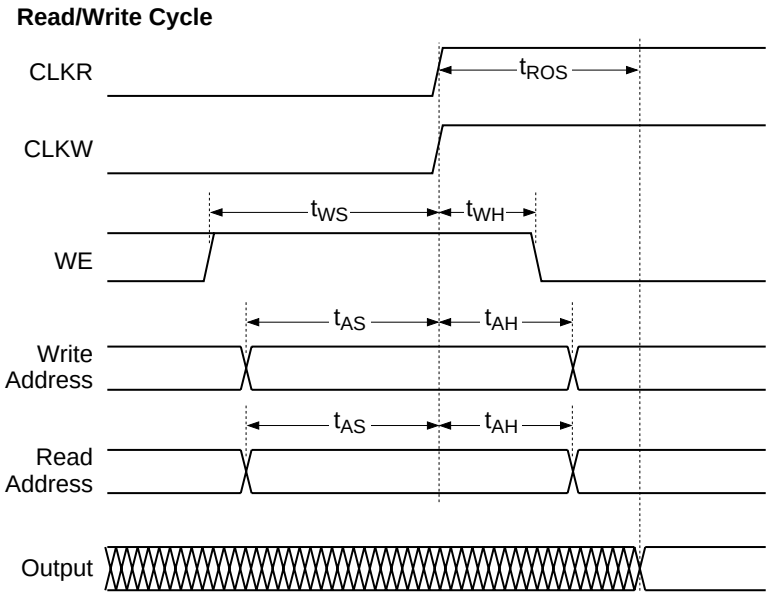


Figure 13: Two-Port SRAM Read/Write Cycle, with Differing Write and Read Addresses

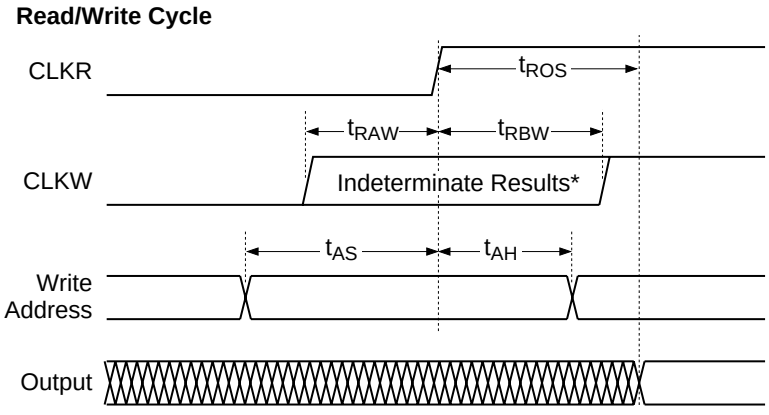


Figure 14: Two-Port SRAM Read/Write Cycle, with Identical Write and Read Addresses

* If the rising edge of CLKW occurs in this region, the output is indeterminate.

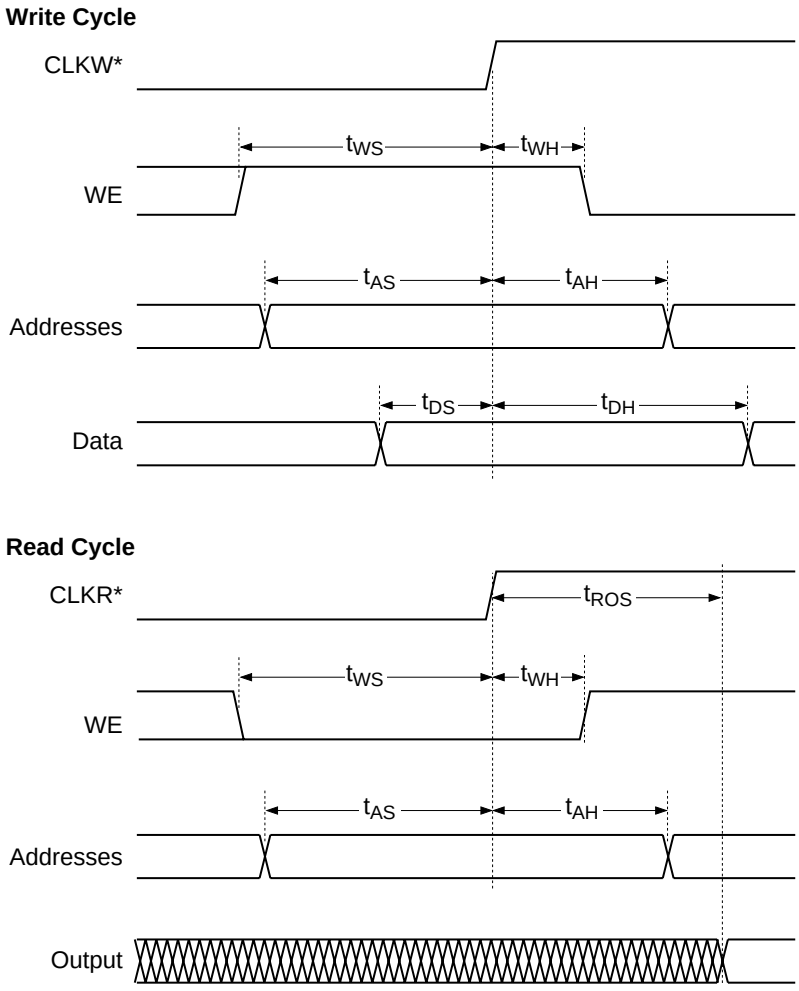


Figure 15: Read/Write Cycle Timing for Single-Port SRAM Configurations

* For single-port operation, CLKW and CLKR are automatically tied together.

The SRAM may be powered down by using the Global Power-Down (GPD) signal. This signal must meet setup-time and hold-time conditions with respect to a clock (write or read), if the entry or exit from powered-down mode is to be effective as of that clock. In powered-down mode, the SRAM bits retain their previously stored information, but cannot be written into or read from as long as the powered-down mode remains in effect, as illustrated in Figure 16.

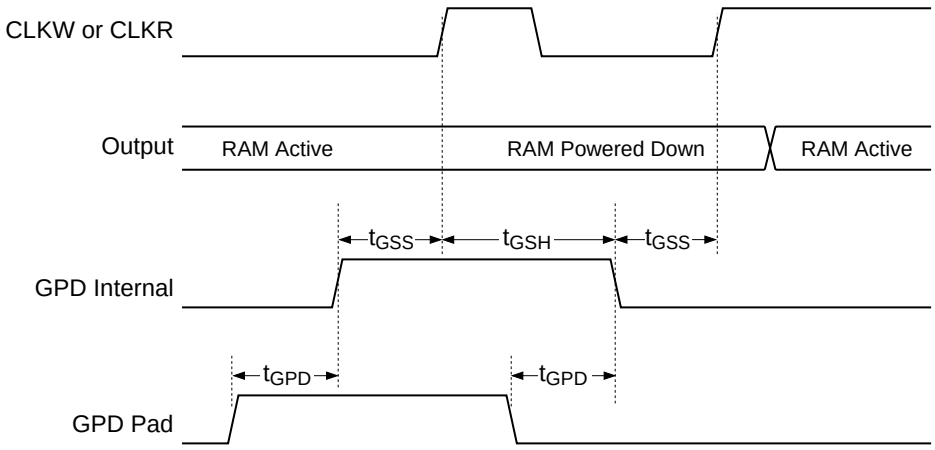


Figure 16: SRAM Power-Down Cycle

Clock Distribution

DY8000-family FPGAs have ten low-skew clock distribution networks. Two of these are global networks which access the entire device; the other eight are quadrant networks which access one quarter of the device. Each of the ten clock networks can be driven from a package pin, from the PLLs, or from signals generated within the FPGA. A signal on any of the ten clock networks can be driven off-chip through package pins.

Every logic block can use any of five clock signals:

- either of the two global clocks
- either of the two quadrant clocks in the quadrant
- local interconnect clock (LCLK) generated by the user's logic

Every I/O block can use any of four clock signals:

- either of the two global clocks
- either of the two quadrant clocks in the quadrant.

Phase-Locked Loops

DY8000 devices contain two PLLs for clock latency reduction, clock multiplication, and clock division. The PLLs support a clock frequency of 8MHz to 200MHz. Each of the two PLLs drive one global clock network and four quadrant-clock networks. The PLLs multiply and divide clock signals by 1, 2, 3, 4, 6, or 8. Table 5 shows the supported input frequency range for different multiplication factors. By default, the PLL reduces clock latency to zero. The latency may be programmed in 80ps increments over the range of -2ns to +2ns.

A filter is required for the PLL power supply. Refer to DynaChip's PLL application note for more information on the filter requirements. External resistors can be connected to device pins PLL1_RES and PLL2_RES for signal optimization.

PLL1 can drive GCLK1, QCLK1TL, QCLK1TR, QCLK1BL, and QCLK1BR. PLL2 can drive GCLK2, QCLK2TL, QCLK2TR, QCLK2BL, and QCLK2BR.

Multiplier	Minimum Input Frequency	Maximum Input Frequency
1	12.5	200
2	24	80
3	19	52
4	14	40
6	10	26
8	8	20

Table 5: PLLs' Supported Input Frequency Ranges

Figure 17 shows, in simplified form, the clock networks for the entire chip.

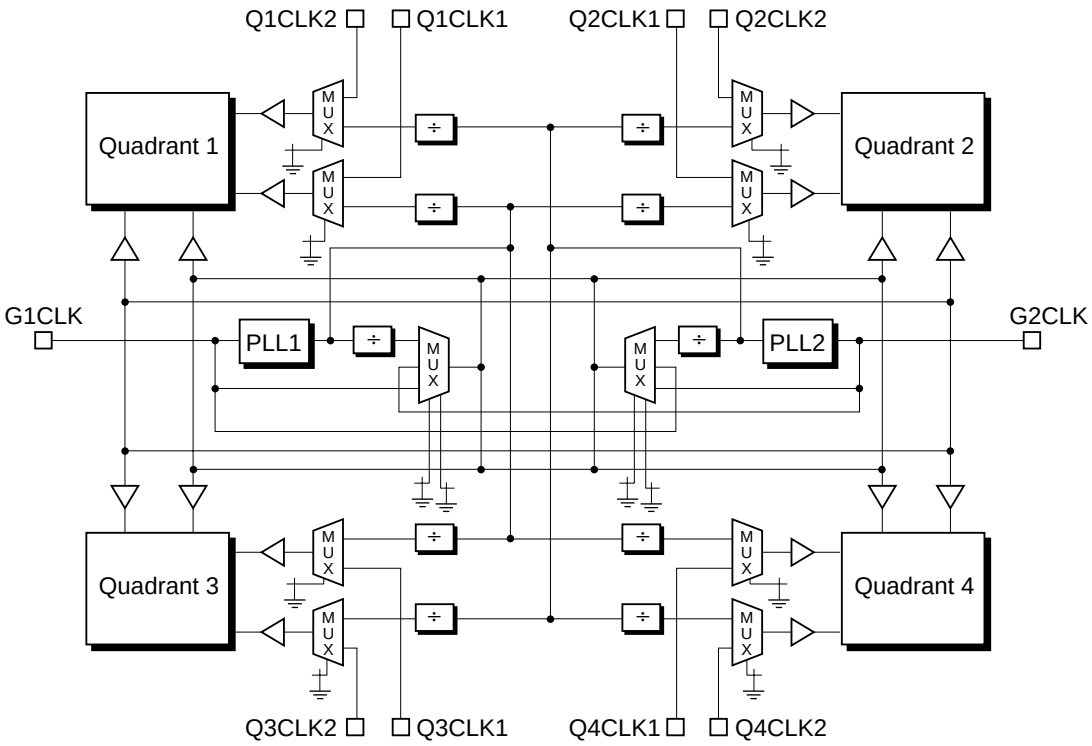


Figure 17: PLL and Clock Networks

Note:

All MUXs have another input which comes from the "derived clock" output of the logic blocks that drive the 10 clock trees.

If the jitter of the incoming clock is 100ps or less, then the jitter of the clock signal produced by the PLL is less than 350ps over commercial voltage and temperature range, or 450ps over industrial voltage and temperature range.

A programmable external feedback option and lock signals are provided for each PLL so they can be used to generate system-level clocks.

JTAG

All devices in the DY8000 family provide JTAG (Joint Test Action Group) Boundary Scan, conformant to the IEEE1149.1 specification. This feature simplifies the testing of boards incorporating devices in surface-mount packages, or in packages with closely-spaced pins.

Four JTAG instructions are supported, as shown in Table 6.

JTAG Instruction	Register	Opcode
SAMPL/PRE	BSC	`1000`
EXTEST	BSC	`0000`
BYPASS	BYPASS	`1111`
IDCODE	ID	`1101`

Table 6: JTAG Instructions

The JTAG ID register is read when the DY8000 device is reset, and when the `1101` opcode is loaded. Upon power-up, the opcode defaults to `1101`. Internal pullup resistors are provided on the TDI and TMS pins.

Product Specifications

Maximum Ratings

Symbol	Description	Value	Unit
V_{CC_INT}	V_{CC} Pin Potential to GND Lead for V_{CC_INT} Pins	-0.5 to +3.0	V
V_{CC_PLL}	V_{CC} Pin Potential to GND Lead for V_{CC_PLL} Pins	-0.5 to +3.0	V
V_{CCO}	V_{CC} Pin Potential to GND Lead for V_{CC_O} Pins	-0.5 to +4.0	V
V_{CCI}	V_{CC} Pin Potential to GND Lead for V_{CC_I} Pins	-0.5 to +4.0	V
V_{IN5V}(4)	Input Voltage (5V Tolerant Mode)	-0.5 to +5.5	V
V_{IN3V}(4)	Input Voltage (3V Tolerant Mode)	-0.5 to +3.6	V
$V_{IN2.5V}$(4)	Input Voltage (2.5V Tolerant Mode)	-0.5 to +3.0	V
V_{TS}	Voltage Applied to 3-State Output Normal Pins	 -0.5 to V_{CC} + 0.5	 V
T_{VCC}	Supply Voltage Rise Time, 1V to 3V	500	ms
T_{STORE}	Storage Temperature (Ambient)	-65 to +150	°C
T_J	Junction Temperature Ceramic Plastic	 +150 +125	 °C °C
T_{SOL}(3)	Soldering Temperature	+260	°C

Table 7: Absolute Maximum Rating

Notes:

(1) Permanent damage to the device may occur if the Absolute Maximum ratings are exceeded. These are stress ratings only. Functional operation of the device at these or any other conditions, other than those listed under the Recommended Operating Conditions, is not implied.

(2) Exposure to Absolute Maximum Ratings conditions for extended periods of time may degrade device reliability.

(3) T_{SOL} should occur for no more than 10 seconds. (EBGA package only.)

(4) On power-up, all I/O are 5V tolerant. After programming, I/O with 3.3V V_{CCO} are 5V tolerant, I/O with 2.5V V_{CCO} are 3V tolerant and I/O with 1.5V V_{CCO} are 2.5V tolerant.

Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V_{CCINT}	Supply Voltage Relative to GND Lead for V_{CC_INT} Pins: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 2.37 2.25	 2.63 2.75	 V V
V_{CCPLL}	Supply Voltage Relative to GND Lead for V_{CC_PLL} Pins: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 2.37 2.25	 2.63 2.75	 V V
V_{CCI}(2)	Supply Voltage Relative to GND Lead for V_{CC_I} Pins: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 3.14 3.0	 3.47 3.6	 V V
V_{CCO}	Supply Voltage Relative to GND Lead for V_{CC_O} Pins: Commercial: 0° C to 85° C Junction Industrial: –40° C to 100° C Junction	 Varies Based on I/O Settings Varies Based on I/O Settings		 V V
T_{IN}	Input Signal Rise or Fall Time	-	250	ns

Table 8: Recommended Operating Conditions

Notes:

(1) All junction temperatures above those listed as Recommended Operating Conditions are unsafe, and may destroy the device.

(2) For reduced power consumption, V_{CCI} can be supplied at 2.5V if V_{CCO} is 2.5V or less.

DC Characteristics

Symbol	Parameter	Min	Max	Test Conditions	Units
V_{IMAX5V}	Max. Voltage Applied to Input (5V Tolerant Mode)	-	5.5		V
V_{IMAX3V}	Max. Voltage Applied to Input (3V Tolerant Mode)	-	3.6		V
$V_{IMAX2.5V}$	Max. Voltage Applied to Input (2.5V Tolerant Mode)	-	3.0		V
V_{DR} (3)	Data-Retention Voltage	2.0	-		V
I_{DDQ}	Quiescent Current (9)	-	10	V_{CC} = Max; All I/Os Open	mA
I_{IL}	Leakage Current	-10	+10		µA
I_{PU}	Pad Pullup Current (When Selected)	-	-150	V_{IN} = 0V V_{CCO} = 3.3V	µA
I_{PD}	Pad Pulldown Current (When Selected)	-	-200	V_{IN} = 5.5V	µA
C_{IN}	Input Capacitance	-	8.0	EBGA Package	pF

Table 9: DC Electrical Characteristics over Operating Conditions

Notes:
(1) All GTL outputs should be terminated to V_{TT} through a 50Ω resistor.
(2) ALL GTLP outputs should be terminated to V_{TT} through a 25Ω termination, configured as a pair of 50Ω resistors, one at each end of the net.
(3) Below this voltage, configuration data may be lost.
(4) All I/O power-up is 5V tolerant.

Input/OUtput Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
AGP	-0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 1	Note 1
AGTLP	-0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	-	-
CTT	-0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
GTL	-0.5	V_{REF} - 0.05	V_{REF} + 0.05	3.6	0.4	-	40	-
GTL+	-0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.6	-	36	-
HSTL I	-0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL III	-0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL IV	-0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
LVCMOS2	-0.5	0.7	1.7	5.5	10% V_{CCO}	90% V_{CCO}	1.5	-0.5
LVDS	-0.5	0.8	2.0	V_{CC} + 0.5	-	-	-	-
LVPECL	1.5	1.8	2.2	2.4	-	-	-	-
LVPECL2	0.7	1.0	1.4	1.6	-	-	-	-
LVTTL	-0.5	0.8	2.0	5.5	0.4	2.4	24	-24
PCI, 3.3V	-0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0V	-0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
SSTL2 I	-0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.5	V_{REF} + 0.5	7.6	-7.6
SSTL2 II	-0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.5	V_{REF} + 0.5	15.2	-15.2
SSTL3 I	-0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.6	V_{REF} + 0.6	8	-8
SSTL3 II	-0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.8	V_{REF} + 0.8	16	-16

Table 10: DC Input and Output Levels

Notes:
(1) Tested to AGP specification.
(2) Tested to PCI specification.

Clock and Set/Reset Buffer Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Global Clock Delay with PLL	T_{GCKDP}	Programmable from -2ns to +2ns in 80ps increments			
Global Clock Delay without PLL(1, 2)	T_{GCKD}	6.4	5.8	5.2	ns
Global Clock Skew	T_{GCKS}	0.18	0.18	0.18	ns
Quadrant Clock Delay with PLL	T_{QCKDP}	Programmable from -2ns to +2ns in 80ps increments			
Quadrant Clock Delay without PLL(1, 2)	T_{QCKD}	4.7	4.3	3.9	ns
Quadrant Clock Skew	T_{QCKS}	0.18	0.18	0.18	ns
Clock Min Pulse Width HIGH	T_{MPH}	2.2	2.0	1.8	ns
Clock Min Pulse Width LOW	T_{MPL}	2.2	2.0	1.8	ns
Global Set/Reset Delay	T_{GSR}	9.9	9.0	8.1	ns

Table 11: Clock and Set/Reset Buffer Switching Characteristics (Input Set to TTL)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip-flop clock input.
(2) Default programming of the PLL offsets actual clock delays, forcing them to 0.0ns.
(3) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(4) Clock delays are also referred to as latency.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Global Clock Delay with PLL	T_{GCKDP}	Programmable from -2ns to +2ns in 80ps increments			
Global Clock Delay without PLL(1, 2)	T_{GCKD}	7.0	6.4	5.8	ns
Global Clock Skew	T_{GCKS}	0.18	0.18	0.18	ns
Quadrant Clock Delay with PLL	T_{QCKDP}	Programmable from -2ns to +2ns in 80ps increments			
Quadrant Clock Delay without PLL(1, 2)	T_{QCKD}	5.4	4.9	4.4	ns
Quadrant Clock Skew	T_{QCKS}	0.18	0.18	0.18	ns
Clock Min Pulse Width HIGH	T_{MPH}	2.2	2.0	1.8	ns
Clock Min Pulse Width LOW	T_{MPL}	2.2	2.0	1.8	ns
Global Set/Reset Delay	T_{GSR}	10.6	9.6	8.6	ns

Table 12: Clock and Set/Reset Buffer Switching Characteristics (Input Set to LV-PECL or LVDS)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip-flop clock input.
(2) Default programming of the PLL offsets actual clock delays, forcing them to 0.0ns.
(3) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(4) Clock delays are also referred to as latency.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Global Clock Delay with PLL	T_{GCKDP}	Programmable from -2ns to +2ns in 80ps increments			
Global Clock Delay without PLL(1, 2)	T_{GCKD}	6.5	5.9	5.3	ns
Global Clock Skew	T_{GCKS}	0.18	0.18	0.18	ns
Quadrant Clock Delay with PLL	T_{QCKDP}	Programmable from -2ns to +2ns in 80ps increments			
Quadrant Clock Delay without PLL(1, 2)	T_{QCKD}	4.8	4.4	4.0	ns
Quadrant Clock Skew	T_{QCKS}	0.18	0.18	0.18	ns
Clock Min Pulse Width HIGH	T_{MPH}	2.2	2.0	1.8	ns
Clock Min Pulse Width LOW	T_{MPL}	2.2	2.0	1.8	ns
Global Set/Reset Delay	T_{GSR}	10.0	9.1	8.2	ns

Table 13: Clock and Set/Reset Buffer Switching Characteristics (input set to AGP, CTT, GTL, GTLP, HSTL, SSTL)

Notes:
(1) Global and quadrant clock delays are measured from the input pin on the device to the flip-flop clock input.
(2) Default programming of the PLL offsets actual clock delays, forcing them to 0.0ns.
(3) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(4) Clock delays are also referred to as latency.

I/O Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input Buffer Combinatorial Delay	T_{INPD}	2.5	2.3	2.1	ns
Input Flip-flop Setup Time (Global Clock)	T_{INIS1}	1.7	1.5	1.4	ns
Input Flip-flop Hold Time (Global Clock)	T_{INIH1}	0.0	0.0	0.0	ns
Input Flip-flop Clock to Output (Global Clock)	T_{INCO1}	1.7	1.5	1.4	ns
Output Buffer Combinatorial Delay (No Load)(2,3)	T_{OUTIS1}	4.0	3.6	3.2	ns
Output Flip-flop Setup Time (Global Clock)	T_{OUTIS2}	2.4	2.2	2.0	ns
Output Flip-flop Hold Time (Global Clock)	T_{OUTIH1}	0.0	0.0	0.0	ns
Output Flip-flop Clock to Output (Global Clock, No Load) (2,3)	T_{OUTCO1}	2.8	2.5	2.3	ns
I/O Flip-flop Clock Enable Setup Time	T_{CES1}	2.1	1.9	1.7	ns
I/O Flip-flop Clock Enable Hold Time	T_{CEH1}	0.0	0.0	0.0	ns
Input Flip-flop GSR Set/Reset Delays	T_{GSRI}	2.5	2.3	2.1	ns
Output Flip-flop GSR Set/Reset Delays	T_{GSRO}	3.5	3.2	2.9	ns
Input Flip-flop GSR Set/Reset Setup Time	T_{GSRIS1}	0.3	0.3	0.3	ns
Output Flip-flop GSR Set/Reset Setup Time	T_{GSROS1}	0.3	0.3	0.3	ns

Table 14: Input and Output Buffer Parameters (I/O Set to TTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(2) Output delays are specified with no load. Add the following delays to adjust for loading.
Fast Slew Rate: 12ps/pF
Medium Slew Rate: 25ps/pF
Slow Slew Rate: 55ps/pF
(3) The maximum loading for outputs switching at the same time in the same direction is shown below. One power/ground pin pair is provided for each eight I/O blocks on the device.
Fast Slew Rate: 200pf between each power/ground pair
Medium Slew Rate: 300pf between each power/ground pair
Slow Slew Rate: 400pf between each power/ground pair
(4) Each output pin has individual slew-rate control.
(5) For V_{CCI} = 3.3V.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
OE to Pad Active (No Load)(2,3)	T_{3SOE}	3.2	2.9	2.6	ns
OE to Pad Hi-Z (No Load) (2,3)	T_{3SOD}	3.6	3.3	3.0	ns
OE Flip-flop Clock to Pad Active (No Load)	T_{Q3SOE}	2.1	1.9	1.7	ns
OE Flip-flop Clock to Hi-Z (No Load)	T_{Q3SOD}	2.4	2.2	2.0	ns
OE Flip-flop Setup Time	T_{OEIS}	2.2	2.0	1.8	ns
OE Flip-flop Hold Time	T_{OEIH}	0.0	0.0	0.0	ns
OE Flip-flop GSR Set/Reset Delay	T_{OEGSRI}	3.6	3.3	3.0	ns
OE Flip-flop GSR Setup Time	$T_{OEGSRIS}$	0.6	0.5	0.5	ns

Table 15: Three-state Buffer Delays (I/O Set to TTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(2) Output delays are specified with no load. Add the following delays to adjust for loading:
Fast Slew Rate: 12ps/pF
Medium Slew Rate: 25ps/pF
Slow Slew Rate: 55ps/pF
(3) Each output pin has individual slew-rate control.
(4) Should be measured with output held at V_{OL} + 0.5V.
(5) For V_{CCI} = 3.3V.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input Buffer Combinatorial Delay	T_{INPD}	2.6	2.4	2.2	ns
Input Flip-flop Setup Time (Global Clock)	T_{INIS1}	1.8	1.6	1.4	ns
Input Flip-flop Hold Time (Global Clock)	T_{INIH1}	0.0	0.0	0.0	ns
Input Flip-flop Clock to Output (Global Clock)	T_{INCO1}	1.7	1.5	1.4	ns
Output Buffer Combinatorial Delay (No Load)(2)	T_{OUTIS1}	3.2	2.9	2.6	ns
Output Flip-flop Setup Time (Global Clock)	T_{OUTIS2}	2.4	2.2	2.0	ns
Output Flip-flop Hold Time (Global Clock)	T_{OUTIH1}	0.0	0.0	0.0	ns
Output Flip-flop Clock to Output (Global Clock, No Load) (2)	T_{OUTCO1}	1.8	1.6	1.4	ns
I/O Flip-flop Clock Enable Setup Time	T_{CES1}	2.1	1.9	1.7	ns
I/O Flip-flop Clock Enable Hold Time	T_{CEH1}	0.0	0.0	0.0	ns
Input Flip-flop GSR Set/Reset Delays	T_{GSRI}	2.5	2.3	2.1	ns
Output Flip-flop GSR Set/Reset Delays	T_{GSRO}	1.9	1.7	1.5	ns
Input Flip-flop GSR Set/Reset Setup Time	T_{GSRIS1}	0.3	0.3	0.3	ns
Output Flip-flop GSR Set/Reset Setup Time	T_{GSROS1}	0.3	0.3	0.3	ns

Table 16: Input and Output Buffer Parameters
(I/O set to AGP, CTT, GTL, GTLP, HSTL, SSTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(2) Output delays are specified with no load. Add the following delays to adjust for loading:
GTL: 7ps/pF
GTLP: 4ps/pF
(3) For V_{CCI} = 3.3V.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
OE to Pad Active (No Load)(2)	T_{3SOE}	3.2	2.9	2.6	ns
OE to Pad Hi-Z (No Load) (2)	T_{3SOD}	3.6	3.3	3.0	ns
OE Flip-flop Clock to Pad Active (No Load)	T_{Q3SOE}	2.1	1.9	1.7	ns
OE Flip-flop Clock to Hi-Z (No Load)	T_{Q3SOD}	2.4	2.2	2.0	ns
OE Flip-flop Setup Time	T_{OEIS}	2.2	2.0	1.8	ns
OE Flip-flop Hold Time	T_{OEIH}	0.0	0.0	0.0	ns
OE Flip-flop GSR Set/Reset Delay	T_{OEGSRI}	3.6	3.3	3.0	ns
OE Flip-flop GSR Setup Time	$T_{OEGSRIS}$	0.6	0.5	0.5	ns

Table 17: Three-state Buffer Delays (I/O set to AGP, CTT, GTL, GTLP, HSTL, SSTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.
(2) Output delays are specified with no load. Add the following delays to adjust for loading:
GTL: 7ps/pF
GTLP: 4ps/pF
(3) Should be measured with output held at V_{OL} + 0.5V.
(4) For V_{CCI} = 3.3V.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input Buffer Combinatorial Delay	T_{INPD}	3.2	2.9	2.6	ns
Input Flip-flop Setup Time (Global Clock)	T_{INIS1}	2.3	2.1	1.9	ns
Input Flip-flop Hold Time (Global Clock)	T_{INIH1}	0.0	0.0	0.0	ns
Input Flip-flop Clock to Output (Global Clock)	T_{INCO1}	1.7	1.5	1.4	ns
I/O Flip-flop Clock Enable Setup Time	T_{CES1}	2.1	1.9	1.7	ns
I/O Flip-flop Clock Enable Hold Time	T_{CEH1}	0.0	0.0	0.0	ns
Input Flip-flop GSR Set/Reset Delays	T_{GSRI}	2.5	2.3	2.1	ns
Input Flip-flop GSR Set/Reset Setup Time	T_{GSRIS1}	0.3	0.3	0.3	ns

Table 18: Input Buffer Parameters (I/O Set to LV-PECL or LVDS)

Note:
All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Logic Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
3-Input AND/OR to Flip-flop Delay	T_{ANDR3}	2.6	2.3	2.1	ns
6-Input AND/OR to Flip-flop Delay	T_{ANDR6}	3.0	2.7	2.4	ns
9-Input AND/OR to Flip-flop Delay	T_{ANDR9}	3.3	3.0	2.7	ns
7-Input XOR to Flip-flop Delay	T_{XORR7}	3.4	3.1	2.8	ns
8:1 Multiplexer Data to Flip-flop	T_{MUXR8}	2.8	2.5	2.3	ns
8:1 Multiplexer Select to Flip-flop	T_{MUXSR8}	2.9	2.6	2.3	ns
2-Bit Adder/Multiplier to Flip-flop (Sum)	T_{ADDCR}	3.3	3.0	2.7	ns
3-Input AND/OR Combinatorial Delay	T_{ANDC3}	2.8	2.5	2.3	ns
6-Input AND/OR Combinatorial Delay	T_{ANDC6}	3.2	2.9	2.6	ns
9-Input AND/OR Combinatorial Delay	T_{ANDC9}	3.6	3.2	2.9	ns
7-Input XOR Combinatorial Delay	T_{XORC7}	3.6	3.2	2.9	ns
2-Input Comparator Combinatorial Delay	T_{COMP3}	3.7	3.3	3.0	ns
Adder/Multiplier Delay (Sum)	T_{ADDC}	3.8	3.4	3.1	ns
8:1 Multiplexer Data Combinatorial Delay	T_{MUXC8}	3.0	2.7	2.4	ns
8:1 Multiplexer Select Combinatorial Delay	T_{MUXS8}	3.1	2.8	2.5	ns
Carry Chain Initial Delay	T_{CRYI}	2.7	2.4	2.2	ns
Carry Chain Delay Per 2 Bits	T_{CRY}	0.3	0.3	0.2	ns
Carry Chain Final Delay	T_{CRYF}	2.3	2.0	1.8	ns
D-Flip-flop Setup Time	T_{SU}	0.4	0.4	0.3	ns
D-Flip-flop Hold Time	T_{HD}	0.0	0.0	0.0	ns
T-Flip-flop Setup Time	T_{SUT}	0.5	0.5	0.4	ns
T-Flip-flop Hold Time	T_{THD}	0.0	0.0	0.0	ns
Flip-flop Clock to Out (GCLK or QCLK)	T_{COG}	1.1	1.0	0.9	ns
Flip-flop Clock to Out (LCLK)	T_{COL}	3.3	3.0	2.7	ns
GSR Set/Reset Delay	T_{GSR}	2.4	2.2	1.9	ns
LSR Set/Reset Delay	T_{LSR}	3.4	3.1	2.8	ns
Logic Block Pass-Through	T_{LBPT}	2.7	2.4	2.2	ns

Table 19: Logic Block Switching Parameters

(Includes All Routing Delays Within Routing Region[5])

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Refer to Figure 9 for a schematic of the logic paths described in Table 19.

(3) The AND/OR combinatorial delay, XOR combinatorial delay, comparator combinatorial delay, adder/multiplier delay, multiplexer combinatorial delay, and carry chain final delay include the complete path through the logic block from inputs through outputs, connection buffers, and routing to the next logic block or Active Repeater.

(4) The AND/OR-to-flip-flop delay, XOR-to-flip-flop delay, and multiplexer-to-flip-flop delay include all elements from inputs to the D/T input of either flip-flop.

(5) Logic block delays shown in Table 19 include all connection buffer and routing delays within a 35-block routing region. Additional delays are incurred only when a net must go through an Active Repeater to reach a block in another routing region.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
3-Input AND/OR Combinatorial Delay	T_{ANDR3}	0.5	0.5	0.4	ns
6-Input AND/OR Combinatorial Delay	T_{ANDR6}	1.0	0.9	0.8	ns
9-Input AND/OR Combinatorial Delay	T_{ANDR9}	1.3	1.2	1.1	ns
7-Input XOR Combinatorial Delay	T_{XORR7}	1.3	1.2	1.1	ns
8:1 Multiplexer Data Combinatorial Delay	T_{MUXR8}	0.7	0.6	0.6	ns
8:1 Multiplexer Select Combinatorial Delay	T_{MUXSR8}	0.8	0.7	0.6	ns
Flip-flop Clock-to-Out (GCLK or QCLK)	T_{COG}	0.5	0.5	0.4	ns

Table 20: Logic Block Switching Parameters

(Excludes All Routing Delays Within Routing Region)

Notes:

(1) All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

(2) Refer to Figure 9 for a schematic of the logic paths described in the above table.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Read/Write Operation		Max	Max	Max	
Address Setup Time Before Clock	T_{AS}	2.2	2.0	1.8	ns
Address Hold Time After Clock	T_{AH}	0.0	0.0	0.0	ns
WE Setup Time Before Clock	T_{WS}	2.2	2.0	1.8	ns
WE Hold Time After Clock	T_{WH}	0.0	0.0	0.0	ns
D_{IN} Setup Time Before Clock	T_{DS}	2.2	2.0	1.8	ns
D_{IN} Hold Time After Clock	T_{DH}	0.0	0.0	0.0	ns
Clock Min Pulse Width HIGH (2)	T_{MPH}	3.5	3.5	3.5	ns
Read Cycle		Min	Min	Min	
Output Data Valid After Clock	T_{ROS}	7.1	6.5	5.8	ns
RAM Enable/Disable		Min	Min	Min	
SRAM Enable/Disable Buffer Delay	T_{GPD}	5.3	4.8	4.3	ns
SRAM Enable Setup with Read/Write Clock	T_{GSS}	2.2	2.0	1.8	ns
SRAM Enable/Disable Hold Time with Read/Write Clock	T_{GSH}	0.0	0.0	0.0	ns
Two Clock Operation		Min	Min	Min	
Read After Write to Same Location	T_{RAW}	2.2	2.0	1.8	ns
Read Before Write to Same Location	T_{RBW}	2.2	2.0	1.8	ns

Table 21: RAM Switching Parameters – Two-Port Mode

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
Read/Write Operation		**Max**	**Max**	**Max**	
Address Setup Time Before Clock	T_{AS}	2.2	2.0	1.8	ns
Address Hold Time After Clock	T_{AH}	0.0	0.0	0.0	ns
WE Setup Time Before Clock	T_{WS}	2.2	2.0	1.8	ns
WE Hold Time After Clock	T_{WH}	0.0	0.0	0.0	ns
DIN Setup Time Before Clock	T_{DS}	2.2	2.0	1.8	ns
DIN Hold Time After Clock	T_{DH}	0.0	0.0	0.0	ns
Read Cycle		**Min**	**Min**	**Min**	
Output Data Valid After Clock	T_{ROS}	7.1	6.5	5.8	ns

Table 22: RAM Switching Parameters – Single-Port Mode

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	**Max**	**Max**	
Horizontal Active Repeater Delay	T_{HRPT}	0.6	0.6	0.5	ns
Vertical Active Repeater Delay	T_{VRPT}	0.6	0.6	0.5	ns
Vertical to Horizontal Active Repeater Delay	T_{VHRPT}	0.6	0.6	0.5	ns
Horizontal to Vertical Active Repeater Delay	T_{HVRPT}	0.6	0.6	0.5	ns

Table 23: Active Repeater Switching Parameters

Note:

All delays are specified over commercial voltage and temperature range. For industrial voltage and temperature range, add 5%.

Pin Description

432-Pin EBGA

Pin Description	DY8105 Ball	Pin Description	DY8105 Ball
VCC_PLL	E28	I/O 54 STD_n	U29
I/O 1 STD_n	F29	I/O 55 STD	U28
I/O 3 STD_n	F28	I/O 56 STD_n	U30
I/O 4 STD cpd	G28	I/O 57 STD	V29
I/O 5 STD_n pll1_fb	G29	I/O 58 STD_n	V28
I/O 6 STD	G30	I/O 59 STD	U31
I/O 9 STD_n pll1_rst	G31	I/O 60 STD_n	V30
I/O 10 STD	H28	I/O 61 STD	V31
I/O 12 STD_n	H29	I/O 62 STD_n	W29
I/O 13 STD	H30	I/O 63 STD	W28
I/O 14 STD_n	H31	I/O 65 STD_n	W30
I/O 15 STD lvpecl_ref	J28	I/O 66 STD	W31
I/O 16 STD_n	J31	I/O 67 we	Y30
I/O 17 STD	J30	I/O 68 ready	Y29
I/O 19 CLK/qck1tl_n	J29	I/O 69 STD_n	Y28
I/O 20 CLK/qck1tl	K29	I/O 70 STD	Y31
I/O 23 STD_n	K28	I/O 72 din7	AA31
I/O 24 STD ref_c	K30	I/O 73 din6	AB31
I/O 28 CLK/qck2tl_n	L29	I/O 75 STD	AA30
I/O 29 CLK/qck2tl	L28	I/O 76 CLK/qck1bl_n	AA28
I/O 30 STD_n	L30	I/O 77 CLK/qck1bl	AA29
I/O 31 STD	K31	I/O 83 din5	AC31
I/O 32 STD	L31	I/O 84 din4	AB30
I/O 33 STD_n ref_b	M31	I/O 86 CLK/qck2bl_n	AB28
I/O 34 STD	M28	I/O 87 CLK/qck2bl	AB29
I/O 35 STD_n	M29	I/O 88 STD_n	AC30
I/O 36 STD	M30	I/O 89 STD	AC29
I/O 37 STD_n ref_a	N31	I/O 90 din3	AC28
I/O 38 STD	N30	I/O 91 din2	AD31
I/O 39 STD	N28	I/O 93 STD_n	AD30
I/O 40 CLK/gck1_n	N29	I/O 94 STD	AD29
I/O 41 CLK/gck1	P29	I/O 95 din1	AE30
I/O 42 STD_n	P30	I/O 96 STD	AD28
I/O 43 STD	P28	I/O 97 STD_n	AE29
I/O 44 STD_n	P31	I/O 98 din0	AE28
I/O 45 STD	R31	I/O 99 JTOUT tdo	AE31
I/O 46 STD_n	R29	I/O 100 STD	AF29
I/O 47 STD	R30	I/O 101 STD_n	AF28
I/O 48 STD_n	R28	reset_n	AG28
I/O 49 STD	T28	strpgm	AH27
I/O 50 STD_n	T31	I/O 102 STD	AH26
I/O 52 STD_n	T30	I/O 103 STD	AJ26
I/O 53 STD	T29	I/O 105 m0	AK26
Pin Description	DY8105 Ball	Pin Description	DY8105 Ball

Table 24: 432-Pin EBGA Package Information

Pin Description	DY8105 Ball	Pin Description	DY8105 Ball
I/O 106_n STD	AH25	I/O 166 STD	AH13
pclkio	AJ25	I/O 167_n STD	AJ13
I/O 107 STD	AK25	I/O 168 STD	AL12
I/O 108 m1	AL25	I/O 169_n STD	AK12
I/O 109_n STD	AH24	I/O 170 STD	AH12
I/O 110 m2	AJ24	I/O 171 STD ref_b	AJ12
I/O 111 STD	AK24	I/O 172_n STD	AL11
I/O 113 done	AL24	I/O 175 STD	AK11
I/O 114_n m3	AH23	I/O 176_n STD	AH11
I/O 115 dout	AJ23	I/O 178 STD	AJ11
I/O 116_n STD	AK23	I/O 179_n STD	AL10
I/O 118 STD	AL23	I/O 180 STD	AK10
I/O 119_n STD	AH22	I/O 181_n STD	AH10
I/O 120 STD	AJ22	I/O 182 STD	AJ10
I/O 121_n STD	AK22	I/O 183_n STD	AL9
I/O 122 STD	AL22	I/O 184 STD	AK9
I/O 123_n STD	AH21	I/O 185 STD	AH9
I/O 125 STD	AJ21	I/O 186_n STD	AJ9
I/O 126_n STD	AK21	I/O 189 STD	AL8
I/O 127 STD	AL21	I/O 190_n STD	AK8
I/O 128_n STD	AH20	I/O 192 STD	AH8
I/O 131 STD	AJ20	I/O 193_n STD	AJ8
I/O 132 STD	AK20	I/O 194 STD	AL7
I/O 133_n STD	AL20	I/O 195_n STD	AK7
I/O 136 STD	AH19	sysdone	AH7
I/O 137_n STD	AJ19	I/O 197 STD	AJ7
I/O 139 STD	AK19	I/O 198_n STD	AJ6
I/O 140_n STD	AL19	I/O 199 JTAGIN_TMS	AH6
I/O 141 STD	AH18	I/O 200_n JTAGIN_TCK	AH5
I/O 142_n STD	AJ18	I/O 201 lvpecl_ref	AG4
I/O 143 STD	AK18	I/O 202 JTIN tdi	AG3
I/O 144_n STD	AL18	I/O 203 STD	AF4
I/O 145 STD	AH17	I/O 205 STD	AF3
I/O 146_n STD	AJ17	I/O 206 STD_n	AF2
I/O 147 STD	AK17	I/O 207 STD gtl_ref_ext / ref_a	AE4
I/O 148_n STD	AL17	I/O 208 STD_n	AE3
I/O 149 STD	AK16	I/O 209 STD	AE2
I/O 150_n STD	AH16	I/O 210 STD_n	AD4
I/O 151 STD	AJ16	I/O 211 STD	AE1
I/O 152_n STD	AL16	I/O 212 STD	AD3
I/O 153 STD	AL15	I/O 213 STD_n	AD2
I/O 154_n STD	AK15	I/O 214 STD	AC4
I/O 155 STD	AH15	I/O 215 STD_n	AD1
I/O 156_n STD	AJ15	I/O 216 STD	AC3
I/O 157 STD par_2	AL14	I/O 217 STD_n	AC2
I/O 158_n STD	AK14	I/O 218 STD	AC1
I/O 159 STD	AH14	I/O 219 CLK/qck2br	AB4
I/O 160_n STD	AJ14	I/O 220 CLK/qck2br_n	AB3
I/O 161 STD	AL13	I/O 223 STD	AB2
I/O 162_n STD	AK13	I/O 224 STD_n	AB1
Pin Description	**DY8105 Ball**	**Pin Description**	**DY8105 Ball**

Table 24: 432-Pin EBGA Package Information

Pin Description	DY8105 Ball	Pin Description	DY8105 Ball
I/O 226 CLK/qck1br	AA4	I/O 286 STD	J2
I/O 227 CLK/qck1br_n	AA3	I/O 287 STD_n	J1
I/O 230 STD	AA2	I/O 288 STD	H1
I/O 231 STD_n	AA1	I/O 289 STD_n	H4
I/O 232 STD	Y4	I/O 292 STD	H3
I/O 233 STD	Y3	I/O 293 STD	H2
I/O 234 STD_n	Y2	I/O 294 STD_n pll2_res	G1
I/O 235 STD	Y1	I/O 297 STD	G4
I/O 236 STD	W4	I/O 298 STD_n pll2_fb	G3
I/O 237 STD	W3	I/O 301 STD	G2
I/O 238 STD_n	W2	I/O 302 STD_n	F4
I/O 239 STD ref_c	W1	VCC_PLL	E4
I/O 240 GSR/gsr	V2	GND_PLL	D5
I/O 241 STD_n	V4	I/O 303 STD_n pllres2	D6
I/O 242 STD	V3	I/O 304 STD	C5
I/O 244 STD	V1	I/O 305_n STD	C6
I/O 245 STD_n	U1	I/O 307_n STD	B5
I/O 246 STD	U2	I/O 308 STD	D7
I/O 247 STD_n	U4	I/O 309_n STD lock2	C7
I/O 248 STD	U3	I/O 310 STD	B6
I/O 249 STD_n	T1	I/O 311_n STD	A6
I/O 250 STD	T2	I/O 312 STD	D8
I/O 252 STD	T4	I/O 314_n STD	C8
I/O 253 STD_n	T3	I/O 315 STD	B7
I/O 254 STD	R3	I/O 318_n STD	B8
I/O 255 STD_n	R4	I/O 319 STD	A7
I/O 256 STD	R2	I/O 321_n STD	D9
I/O 257 STD_n	R1	I/O 322 STD	C9
I/O 258 STD	P3	I/O 323_n STD	B9
I/O 259 STD_n	P4	I/O 324 STD	A8
I/O 260 STD	P2	I/O 325_n STD	A9
I/O 261 STD_n	P1	I/O 326 STD	D10
I/O 262 CLK/gck2	N3	I/O 328_n STD	C10
I/O 263 CLK/gck2_n	N4	I/O 329 STD	B10
I/O 264 STD	N2	I/O 330_n STD	A10
I/O 265 STD	N1	I/O 331 STD	B11
I/O 266 STD_n ref_b	M2	I/O 332_n STD	D11
I/O 267 STD	M3	I/O 333 STD	C11
I/O 268 STD_n	M4	I/O 335_n STD	A11
I/O 269 STD	M1	I/O 336 STD	B12
I/O 270 STD_n	L1	I/O 337_n STD ref_c	C12
I/O 271 STD	L2	I/O 338 STD	D12
I/O 272 STD	L4	I/O 342_n STD	A12
I/O 273 STD_n	L3	I/O 343 STD	A13
I/O 274 CLK/qck2tr	K3	I/O 344_n STD	B13
I/O 275 CLK/qck2tr_n	K4	I/O 345 STD	A14
I/O 279 STD	K2	I/O 346_n STD	D13
I/O 280 STD_n	K1	I/O 347 STD	C13
I/O 283 CLK/qck1tr	J3	I/O 348_n STD	D14
I/O 284 CLK/qck1tr_n	J4	I/O 349 STD	C14
Pin Description	**DY8105 Ball**	**Pin Description**	**DY8105 Ball**

Table 24: 432-Pin EBGA Package Information

Pin Description	DY8105 Ball	Pin Description	DY8105 Ball
I/O 350_n STD	B14	I/O 378_n STD	A22
I/O 351 STD	C15	I/O 379 STD	B22
I/O 352_n STD	B15	I/O 381_n STD	C22
I/O 353 STD	C16	I/O 382 STD	D22
I/O 354_n STD	B16	I/O 383_n STD	A23
I/O 355 STD	B17	I/O 384 STD	A24
I/O 356_n STD	C17	I/O 385_n STD	B23
I/O 357 STD	B18	I/O 386 STD	C23
I/O 358_n STD	C18	I/O 388_n STD	D23
I/O 359 STD	D18	I/O 389 STD	A25
I/O 360_n STD	C19	I/O 390_n STD	B24
I/O 361 STD	D19	I/O 391 STD	B25
I/O 362_n STD	A18	I/O 392_n STD	C24
I/O 363 STD	B19	I/O 393 STD	D24
I/O 364_n STD adoe	A19	I/O 395_n STD	A26
I/O 365 STD	A20	I/O 396 STD	B26
I/O 367_n STD	D20	I/O 397_n STD	C25
I/O 368 STD	C20	I/O 398 STD	D25
I/O 371_n STD	B20	I/O 399_n STD lock1	B27
I/O 372 STD	A21	I/O 400 STD	C26
I/O 373 STD lvpecl_ref	C21	I/O 403_n STD	C27
I/O 376_n STD	D21	I/O 404 STD pllres1	D26
I/O 377 STD	B21	GND_PLL	D27
Pin Description	**DY8105 Ball**	**Pin Description**	**DY8105 Ball**

Table 24: 432-Pin EBGA Package Information

432-Pin EBGA - Internal V_{CC} and Ground Connections

V_{CC}_Int Balls	GND_Int Balls	V_{CC}_I/O Balls	GND_I/O Balls
C3	B3	A1	A2
D2	C2	A3	A4
D4	C4	A5	B1
E3	D3	B2	D1
F2	E2	C1	F1
AH2	F3	E1	AG1
AH4	AG2	AF1	AJ1
AJ3	AH3	AH1	AK2
AJ5	AJ2	AK1	AK6
AK4	AJ4	AL2	AL1
AK28	AK3	AL4	AL3
AJ27	AK5	AL6	AL5
AJ29	AK27	AL27	AL26
AH28	AK29	AL29	AL28
AH30	AJ28	AL31	AL30
AG29	AJ30	AK30	AK31
AF30	AH29	AJ31	AH31
F30	AG30	AG31	AF31
E29	E30	E31	F31
D28	D29	C31	D31
D30	C28	B30	B31
C29	C30	A31	A30
B28	B29	A29	A28
D16	D17	A27	A17
B4	D15	A16	A15
V_{CC}_Int Balls	GND_Int Balls	V_{CC}_I/O Balls	GND_I/O Balls

Table 25: 432-Pin EBGA - Internal V_{CC} and Ground Connections

240-Pin EQFP

Pin Description	DY8105 Pin ID	Pin Description	DY8105 Pin ID
I/O 10 STD	175	I/O 213 STD	55
I/O 101 JTOUT tdo	122	I/O 214 STD_n	54
I/O 102 STD	119	I/O 216 STD	52
I/O 105 m0	118	I/O 217 STD_n	51
I/O 108 m1	116	I/O 219 CLK/qck2br	49
I/O 110 m2	114	I/O 220 CLK/qck2br_n	48
I/O 113 done	111	I/O 226 CLK/qck1br	45
I/O 114 m3	110	I/O 227 CLK/qck1br_n	44
I/O 115 dout	109	I/O 23 STD_n	167
I/O 118 STD_n	107	I/O 230 STD	43
I/O 122 STD_n	106	I/O 231 STD_n	42
I/O 123 STD	105	I/O 235 STD	40
I/O 128 STD	103	I/O 236 STD	39
I/O 132 STD	101	I/O 24 STD ref_c	166
I/O 133_n STD	100	I/O 240 GSR/gsr	36
I/O 136 STD	99	I/O 241 STD_n	35
I/O 137_n STD	98	I/O 244 STD	34
I/O 141 STD	94	I/O 245 STD_n	33
I/O 142_n STD	93	I/O 248 STD	32
I/O 147 STD	92	I/O 255 STD_n	30
I/O 148_n STD	91	I/O 258 STD	29
I/O 15 STD lvpecl_ref	171	I/O 259 STD_n	28
I/O 151 STD	90	I/O 262 CLK/gck2	27
I/O 152_n STD	89	I/O 263 CLK/gck2_n	26
I/O 155 STD	88	I/O 266 STD_n ref_b	23
I/O 156_n STD	87	I/O 269 STD	21
I/O 161 STD cbe6_2	85	I/O 270 STD_n	20
I/O 162_n STD	84	I/O 274 CLK/qck2tr	18
I/O 166 STD	81	I/O 275 CLK/qck2tr_n	17
I/O 167_n STD	80	I/O 279 STD	15
I/O 171 STD ref_b	78	I/O 28 CLK/qck2tl_n	164
I/O 172_n STD	77	I/O 280 STD_n	14
I/O 175 STD	76	I/O 283 CLK/qck1tr	13
I/O 180 STD	74	I/O 284 CLK/qck1tr_n	12
I/O 181_n STD	73	I/O 288 STD	10
I/O 186_n STD	71	I/O 29 CLK/qck2tl	163
I/O 189 STD	69	I/O 293 STD	6
I/O 19 CLK/qck1tl_n	169	I/O 294 STD_n pll2_res	5
I/O 190_n STD	68	I/O 297 STD	4
I/O 194 STD	65	I/O 298 STD_n pll2_fb	3
I/O 195_n STD	64	I/O 301 STD	2
I/O 199 JTAGIN_TMS	62	I/O 303 STD_n pllres2	239
I/O 20 CLK/qck1tl	168	I/O 304 STD	238
I/O 200_n JTAGIN_TCK	61	I/O 309 STD lock2	237
I/O 201 lvpecl_ref	60	I/O 310 STD_n	236
I/O 203 JTIN tdi	59	I/O 314_n STD	233
I/O 207 STD gtl_ref_ext / ref_a	58	I/O 318_n STD	231
Pin Description	**DY8105 Pin ID**	**Pin Description**	**DY8105 Pin ID**

Table 26: 240-Pin EQFP Package Information

Pin Description	DY8105 Pin ID	Pin Description	DY8105 Pin ID
I/O 319 STD	230	I/O 67 we	142
I/O 323_n STD	228	I/O 68 ready	141
I/O 324 STD	227	I/O 72 din7	139
I/O 328_n STD	225	I/O 73 din6	138
I/O 329 STD	224	I/O 76 CLK/qck1bl_n	137
I/O 33 STD_n ref_b	161	I/O 77 CLK/qck1bl	136
I/O 333 STD	223	I/O 83 din5	133
I/O 337_n STD ref_c	221	I/O 84 din4	132
I/O 338 STD_n	220	I/O 86 CLK/qck2bl_n	130
I/O 34 STD	160	I/O 87 CLK/qck2bl	129
I/O 342_n STD	217	I/O 9 STD_n pll1_rst	176
I/O 343 STD	216	I/O 90 din3	127
I/O 348_n STD perr_4	214	I/O 91 din2	126
I/O 349 STD	213	I/O 95 din1	124
I/O 352_n STD	212	I/O 98 din0	123
I/O 353 STD	211	pclkio	117
I/O 356_n STD	210	reset_n	121
I/O 357 STD	209	strpgm	120
I/O 362_n STD	208	sysdone	63
I/O 363 STD	207	Vcc_int	8
I/O 368 STD	203	Vcc_int	25
I/O 37 STD_n ref_a	158	Vcc_int	37
I/O 371_n STD	202	Vcc_int	56
I/O 372 STD	201	Vcc_int	67
I/O 376_n STD	199	Vcc_int	83
I/O 377 STD	198	Vcc_int	96
I/O 381_n STD	196	Vcc_int	113
I/O 382 STD	195	Vcc_int	125
I/O 385_n STD	194	Vcc_int	144
I/O 386 STD	193	Vcc_int	156
I/O 390_n STD	191	Vcc_int	173
I/O 391 STD	190	Vcc_int	188
I/O 396 STD	186	Vcc_int	205
I/O 399_n STD lock1	185	Vcc_int	218
I/O 4 STD cpd	179	Vcc_int	234
I/O 40 CLK/gck1_n	155	VCC_PLL	180
I/O 400 STD	184	VCC_PLL	1
I/O 403_n STD	183	VCCI	16
I/O 404 STD pllres1	182	VCCI	47
I/O 41 CLK/gck3	154	VCCI	75
I/O 44 STD_n	153	VCCI	104
I/O 45 STD	152	VCCI	134
I/O 48 STD_n	151	VCCI	165
I/O 5 STD_n pll1_fb	178	VCCI	197
I/O 55 STD	149	VCCI	226
I/O 58 STD_n	148	VCCO 1	159
I/O 59 STD	147	VCCO 1	172
I/O 6 STD	177	VCCO 2	187
I/O 62 STD_n	146	VCCO 2	204
I/O 63 STD	145	VCCO 3	215
Pin Description	DY8105 Pin ID	Pin Description	DY8105 Pin ID

Table 26: 240-Pin EQFP Package Information

Pin Description	DY8105 Pin ID	Pin Description	DY8105 Pin ID
VCCO 3	232	Gnd_I/O	157
VCCO 4	9	Gnd_I/O	174
VCCO 4	22	Gnd_I/O	189
VCCO 5	38	Gnd_I/O	206
VCCO 5	50	Gnd_I/O	219
VCCO 6	70	Gnd_I/O	235
VCCO 6	86	Gnd_int	11
VCCO 7	97	Gnd_int	19
VCCO 7	115	Gnd_int	46
VCCO 8	131	Gnd_int	72
VCCO 8	143	Gnd_int	79
Gnd_I/O	7	Gnd_int	102
Gnd_I/O	24	Gnd_int	108
Gnd_I/O	31	Gnd_int	135
Gnd_I/O	41	Gnd_int	162
Gnd_I/O	53	Gnd_int	170
Gnd_I/O	66	Gnd_int	192
Gnd_I/O	82	Gnd_int	200
Gnd_I/O	95	Gnd_int	222
Gnd_I/O	112	Gnd_int	229
Gnd_I/O	128	GND_PLL	181
Gnd_I/O	140	GND_PLL	240
Gnd_I/O	150		
Pin Description	**DY8105 Pin ID**	**Pin Description**	**DY8105 Pin ID**

Table 26: 240-Pin EQFP Package Information

Package Drawings

432-Pin EBGA

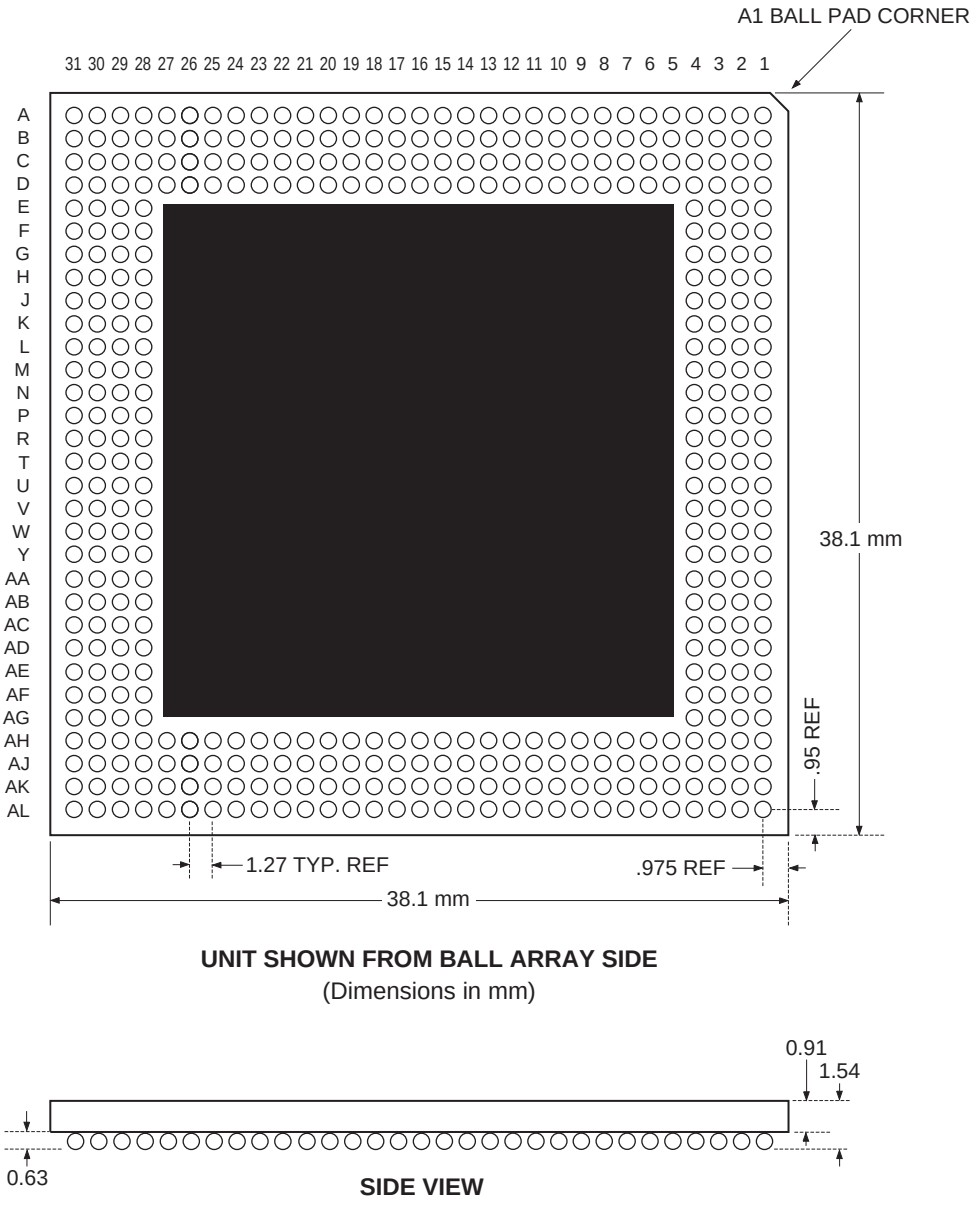


Figure 18: Package Drawing of 432-pin EBGA

Note:
All power and ground pins must be connected.

240-Pin Thermal Enhanced EQFP

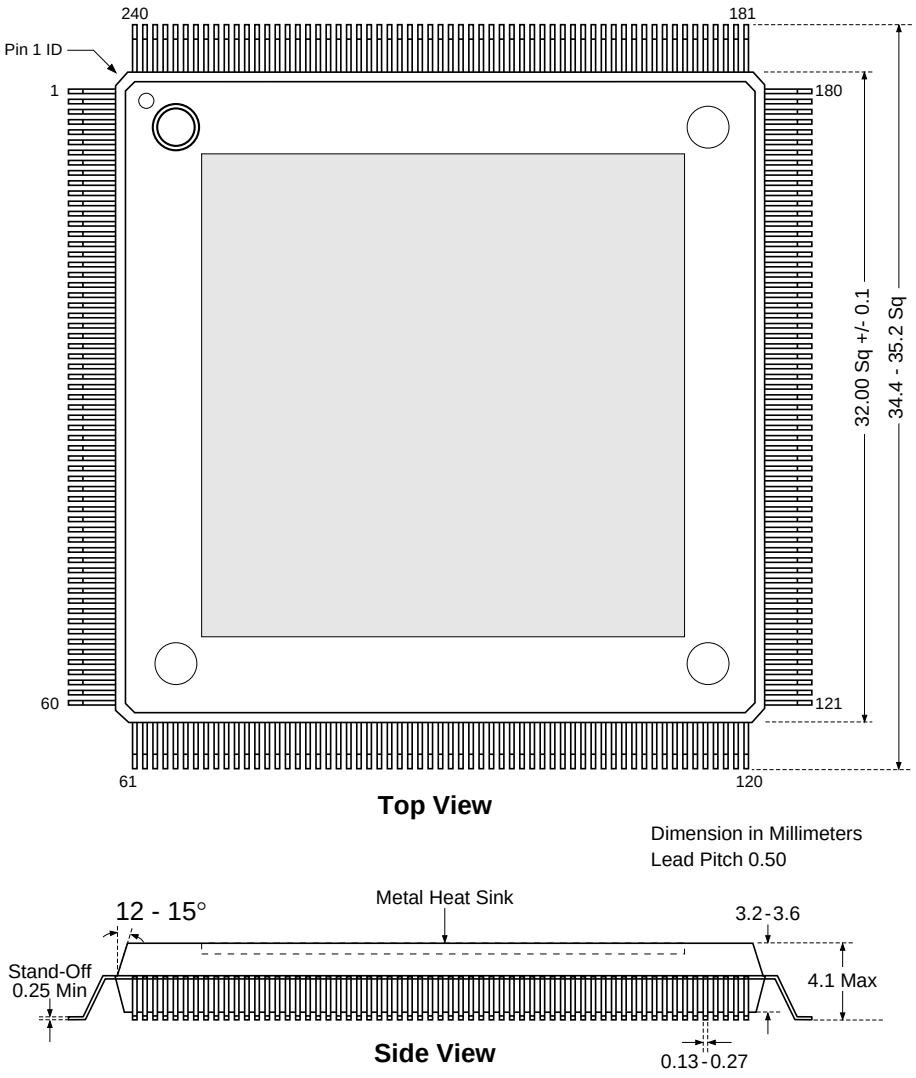


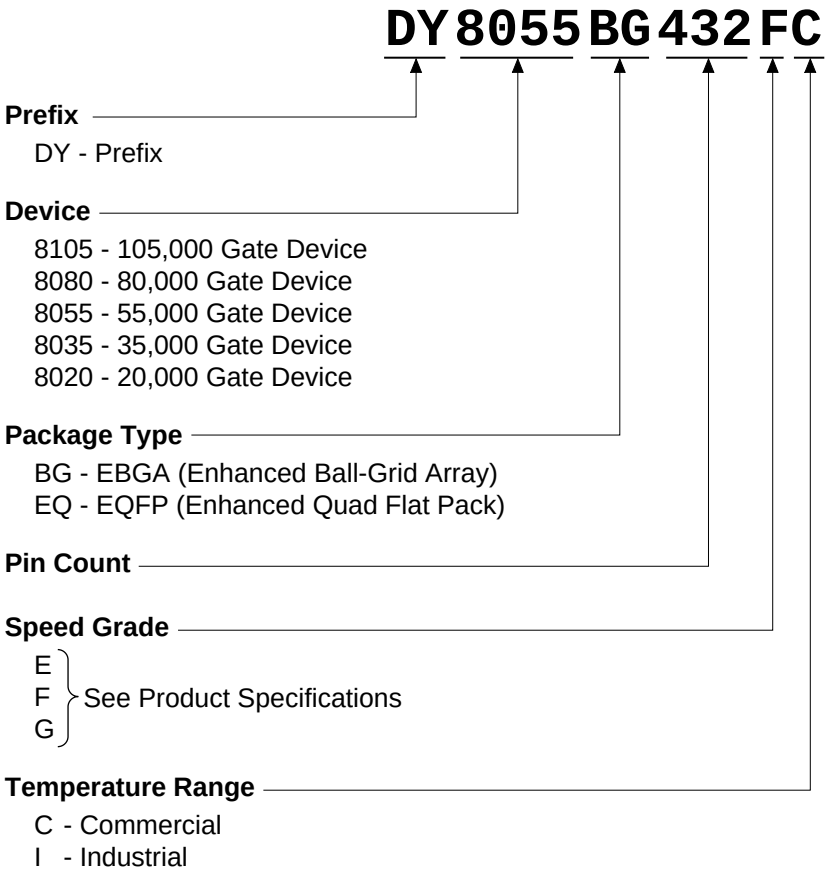
Figure 19: Package Drawing of 240-pin EQFP

Note:

All power and ground pins must be connected.

Ordering Information

Order codes are shown below.



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