DSTni-LX

Description

The DSTni-LX is a high-performance version of the 16-bit Intel® 80186 microprocessor that includes 256 KBytes of on-chip SRAM and a number of on-chip communications peripherals. Developed to simplify the design and reduce the cost of network-enabled products, DSTni-LX is ideal for products that require remote monitoring and control capabilities.

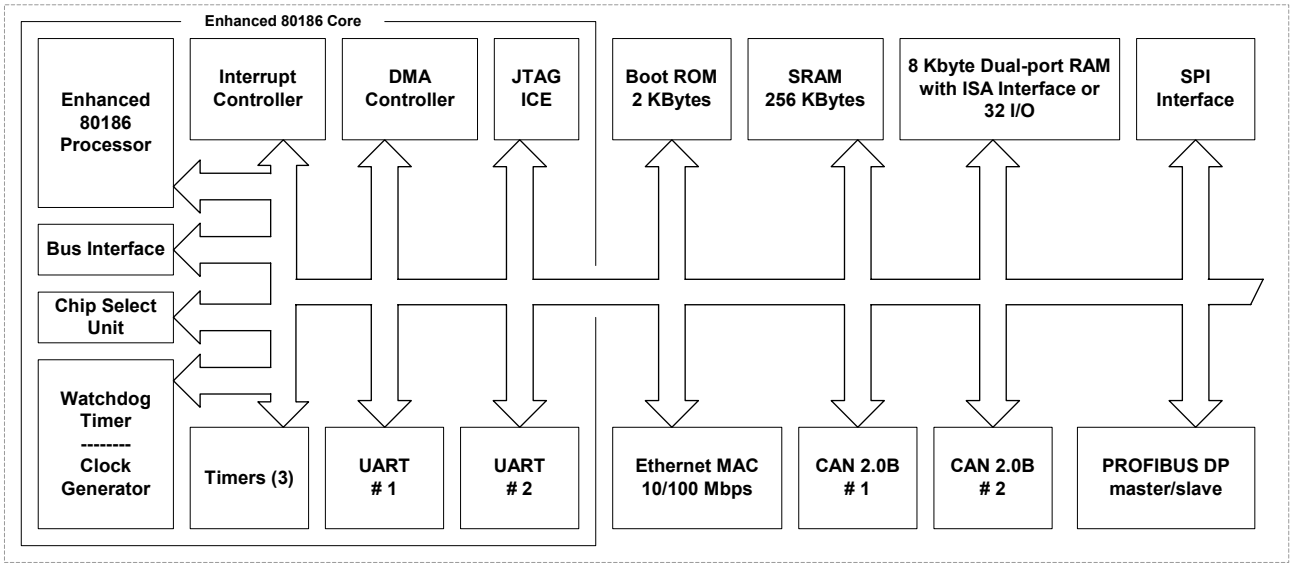
Through reduced clock cycle memory access and a pipelined micro-architecture, DSTni-LX provides 12.5 MIPS of throughput at 48 MHz. For standalone applications, DSTni-LX can be used as the primary processor in a system. In more complex applications, it can function as a network coprocessor, utilizing the built-in ISA bus interface and dual-port RAM, or a network connection, to interface with the host system.

On-chip communications include a 10/100 Mbps Ethernet controller (MAC), two separate 1 Mbps CAN 2.0B channels, a 12 Mbps PROFIBUS DP controller, two full-duplex UARTs and a SPI interface.

The DSTni-LX is supported by a large base of mature x86 tools, including an integrated set of development tools from Lantronix that contain an IDE, C compiler, RTOS, TCP/IP protocol suite, in-circuit emulator, debugger and evaluation board.

Features

- Intel compatible 80186 16-bit microprocessor providing 12.5 MIPS throughput at 48 MHz
- 256 KBytes of on-chip SRAM with support for up to 16 Mbytes of external memory
- 2 KBytes of on-chip masked boot ROM
- 8 KByte dual-port RAM with ISA bus interface or 32 general purpose I/O lines
- 10/100 Mbps Ethernet controller with AMD 960 compatible register interface
- Two CAN V2.0B 1 Mbps controllers with Express Message Technology for time critical messages
- PROFIBUS DP 12 Mbps master/slave controller (licensed from Siemens)
- Two full-duplex UARTS, with RTS/CTS and DMA support
- Serial Peripheral Interface (SPI)
- Integrated DMA controller, interrupt controller, timers, chip select logic and watchdog timer
- JTAG interface with in-circuit emulator support for breakpoints and trace buffer
- Extended temperature range –40° to +105°C
- 160-pin LQFP package



DSTni-LX Block Diagram

1. DSTni-LX Features

The DSTni-LX is high-performance version of the 16-bit Intel® 80186 microprocessor that includes 256 KBytes of on-chip SRAM and integrated communications peripherals. Through reduced clock cycle memory access and a pipelined micro-architecture, DSTni-LX provides up to 12.5 MIPS throughput at 48 MHz.

On-chip peripherals include: three programmable timer/counters, interrupt controller, 4-channel DMA controller, bus interface, programmable chip-select unit, JTAG port, and a watchdog timer.

Integrated communications peripherals include a 10/100 Mbps Ethernet controller (MAC), two separate 1 Mbps CAN 2.0B channels, a 12 Mbps PROFIBUS DP controller, two full-duplex UARTs and an SPI interface.

The DSTni-LX is software compatible with the 8088, 8086, 80188 and 80186 microprocessors from Intel and AMD, and uses standard x86 compilers and development tools.

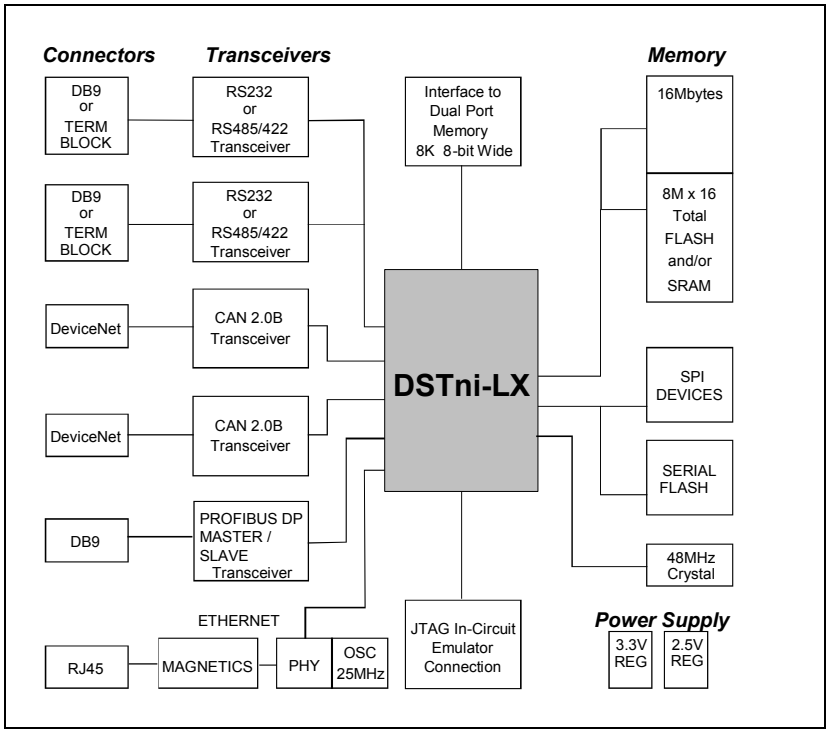


Figure 1-1: DSTNI-1 System Block Diagram

1.1 Programmable Timers

The processor provides three (3) internal 16-bit programmable timers. They can be used to count external events, time external events, generate nonrepetitive waveforms, etc.

Timer 0 connects to two external pins, one input and one output. The output can be used to generate waveforms with programmable duty cycles.

Timers 1 and 2 are not connected to any external pins, and may be used for real-time coding and time delay functions. Timer 2 can also be used as a prescaler to the other two, as a DMA request source, or as an SPI clock source when the SPI port is in master mode.

1.2 Interrupt Controller

The integrated interrupt controller manages and prioritizes the internal and external interrupt sources. Internal interrupt sources include the Timers and DMA channels. External sources include the INT lines. These sources can be disabled by their own control register or by the mask bits within the interrupt controller.

The interrupt controller also has the ability to resolve priority among simultaneous interrupt requests. This interrupt controller is a functional subset of the 80C186 interrupt controller and it only supports master mode, and fully nested mode.

1.3 DMA Controller

An integrated direct memory access (DMA) controller permits transfer of data between memory and peripherals without CPU involvement.

The DMA unit in the DSTni-LX processor provides four high-speed DMA channels to transfer data between memory and I/O spaces (e.g., memory to I/O) or within the same space (e.g., memory-to-memory or I/O-to-I/O).

The DMA channels can be directly connected to the asynchronous serial ports. DMA transfer for the asynchronous serial ports is accomplished by programming the DMA controller to perform transfers between a data source in memory or I/O space and an asynchronous serial port transmit or receive register.

1.4 Chip Select Logic

The DSTni-LX contains logic that provides programmable chip select generation for both external memory and peripherals. In addition, the logic can be programmed to provide ready or wait-state signals. The chip select lines are active for all memory and I/O cycles in their programmed areas, whether they are generated by the CPU or by the integrated DMA unit.

There are four chip select outputs for use with memory mapped devices, and six more for use with peripherals in the I/O space. The memory chip selects can be used to address up to four memory ranges. Each peripheral chip select addresses a 256-byte block offset from a programmable base address.

1.5 External Bus Interface

For applications that require external peripherals or additional memory, DSTni-LX offers an external 24-bit address, 16-bit data bus.

This interface provides for up to 16 Mbytes of external memory, like Flash or Static RAM, when an application requires more resources than are internal to the chip.

1.6 Asynchronous Serial Ports

The DSTni-LX provides two asynchronous serial ports (UARTs), supporting rates up to 115.2 kbps.

Both ports provide full duplex operation, 4-word receive buffer FIFOs, RTS/CTS handshaking and support for driving the transmit enable pin of common RS-422/485 line drivers. In addition, both ports provide DMA support, both to and from the transmit and receive buffers.

Any combination of the following are supported:

- 7 or 8-bit data bits
- 1 or 2 stop bits
- Even, odd or no parity

The receive portion of the serial ports provide break character recognition and error detection for frame, parity and overrun errors. In addition, they are programmable to generate interrupts whenever one of these error conditions is detected. Interrupts can be generated by the serial port to signal that the next segment of data is being sent or that valid data has been received.

1.7 Hardware Watchdog Timer

The DSTni-LX watchdog timer (WDT) can be configured to generate either an NMI interrupt or a system reset upon timeout.

After reset, the watchdog timer defaults to enabled. The application program must periodically reset the timer by writing a specific key sequence to the watchdog timer control register. An external pin is available to externally monitor that a watchdog reset or timeout has occurred.

1.8 On-Chip Static RAM

The DSTni-LX includes 256 KBytes of on-chip memory. This memory is zero wait state, 16-bit wide, 10nS static RAM, which allows for maximum processor performance.

1.9 Boot ROM Memory

An on-chip 2 kByte Boot ROM, provides power-up or reset testing/zeroing of the on-chip SRAM, and supports loading code from the following sources:

- Serial flash device
- Parallel non-volatile memory (flash or EPROM)
- Serial port

1.10 SPI Controller

The Serial Peripheral Interface (SPI) controller provides a synchronous serial link for interfacing with other processors and peripherals.

The SPI port can be used to load code from a serial flash device at power-up or reset.

1.11 10/100 Mbps Ethernet Controller

The DSTni-LX has an integrated Ethernet 10/100 Mbps controller with Media Independent Interface (MII), for connection to an external physical layer device (PHY).

The controller interfaces directly to the DSTni-LX internal system bus, operating with no wait states. It is register compatible with the Advanced Micro Devices AM7990 LANCE and AM79C960 PCnet-ISA Ethernet controllers.

It includes individual transmit and receive FIFOs and a DMA buffer management unit to reduce system overhead. Supported protocols include IEEE 802.3 and ANSI 8802-3.

1.12 Dual 1 Mbps CAN Controllers

Two completely independent CAN 2.0B controllers provide fast and reliable, multicast/multimaster, prioritized serial communications for up to 127 nodes over inexpensive twisted-pair cable.

Both CAN channels are capable of high-speed (1Mbps) data transmission at distances up to 40m, and low-speed (5 kbps) transmissions at lengths of up to 10,000 meters.

Programmable message acceptance filters reduce system overhead. Data throughput is enhanced with Express Message Technology, which continuously monitors the transmit buffer, transmitting the highest priority message first.

1.13 PROFIBUS DP Master/Slave Controller

PROFIBUS is a high-speed, RS-485 based, serial bus, specifically designed specifically for industrial process, manufacturing, and building automation applications, supporting up to 127 field devices.

DSTni-LX includes a fully licensed PROFIBUS DP master/slave controller from Siemens, that emulates their ASPC2 controller. It supports all the recent technology extensions like DPV1 and DPV2, and includes an integrated DMA unit to reduce system overhead.

All the standard communications rates from 9600 bps to 12 Mbps are supported by the controller. With appropriate bus transceivers, high-speed (12 Mbps) data transmission at distances up to 100m, and low-speed (9600 bps) transmissions at lengths of up to 24,000 meters are possible.

1.14 Dual Port Memory / General Purpose I/O

For applications in which the DSTni-LX is to be used as a communications coprocessor, a dual port memory with a PC/ISA bus is available. The signals required for this interface are shared with the 27 of the 32 user-programmable I/O pins.

The 8 Kbyte dual port memory is functionally compatible with the Integrated Device Technology (IDT) IDT7005 chip. It includes 8-semaphores for ease of data consistency in the application.

Some of the 32 user-programmable I/O pins are multiplexed with other I/O or control functions, like the dual port memory interface. The function of each pin is individually controlled by setting the appropriate mode and direction registers.

1.15 JTAG Debugger / ICE Interface

An integrated JTAG interface (IEEE 1149.1) provides access to the DSTni-LX processor and its peripherals. The architecture contains logic for four hardware breakpoints and a 256 word trace buffer.

With appropriate tools, developers can: load application software, set breakpoints, single-step, read/write memory and I/O, interrogate the state of the processor, view the trace buffer, and perform many other in-circuit emulation (ICE) functions.

First Silicon Solutions has developed a system analyzer, designed to support the special features and integrated peripherals of the DSTni-LX. Special “silicon hooks” for system development are integrated into the DSTni-LX to provide a powerful debug tool with advanced features.

2. Pin Configuration

Figure 2-1: DSTni-LX Pin Configuration

3. Pin Descriptions

Name	Pin No.	Type	Description
ADDR22 ADDR21 ADDR20 ADDR19 ADDR18 ADDR17 ADDR16 ADDR15 ADDR14 ADDR13 ADDR12 ADDR11 ADDR10 ADDR09 ADDR08 ADDR07 ADDR06 ADDR05 ADDR04 ADDR03 ADDR02 ADDR01 ADDR00	79 66 55 49 48 43 42 37 36 32 31 28 27 16 15 12 11 8 158 157 154 153 151	Address Bus (Outputs)	These 23 signals are output pins. They supply non-multiplexed memory or I/O addresses to the connected system. ADDR22 is the MSB and ADDR00 is the LSB. Note: Although not available as an external pin, ADDR23 is internally used and is the MSB of the Address Bus. All lines are always enabled which means they do not enter a high-impedance state. Following a system reset, ADR22-20 remain in the logic low state for “Real” or 20-bit mode. In “extended” or 24-bit mode, ADR22-20 function as normal address lines.
DATA15 DATA14 DATA13 DATA12 DATA11 DATA10 DATA09 DATA08 DATA07 DATA06 DATA05 DATA04 DATA03 DATA02 DATA01 DATA00	86 87 92 93 96 97 102 103 107 108 115 124 125 128 129 132	Data Bus (Bi-Directional)	These 16 signals make up the external Data Bus pins. DATA15 is the MSB and DATA00 is the LSB. This Data Bus is bi-directional to allow system data to be passed in and out through READ and WRITE accesses respectively. This bus also goes into the high-impedance state when the system is not accessing external I/O or memory.
X1	20	Crystal Input	This pin and the X2 pin provide connections for the internal oscillator circuit. If an external crystal is used, the X2 pin is required as well. For external clock or oscillator circuits with digital output drivers, this pin can be connected directly and the X2 pin is left unconnected.
X2	21	Crystal Output	This pin and the X1 pin provide connections for the internal oscillator circuit (see X1 description above).
RES_N	30	Reset (Input)	This input pin forces the microcontroller to perform a reset. When RES_N is asserted, the microcontroller immediately terminates its present activity, clears its internal logic, and CPU control is transferred to the reset address, FFFF0h (20-bit mode) or FFFFE0H (24-bit mode). Note: This processor has an internal 2048 bytes of “BOOT-ROM” located at the top of the address space, so execution will always start here when reset occurs. Any externally connected devices in the reset vector address will be overridden by the internal logic.

Name	Pin No.	Type	Description
TCK	2	JTAG Clock (Input)	The JTAG interface is used by the In-Circuit Emulator to access the hardware registers that support the breakpoint and trace functions. The four interface pins are TCK, TMS, TDI, and TDO. See the “In-Circuit Emulator” section for more details. The ESD tolerance for the TDO output, pin 5 is only about 500 Volts. This output is used by the JTAG interface to the FS-2 In-System Emulator. ESD precautions such as a grounded work area, using wrist straps, and making the connection, or removing the connection when the power is off, need to be used. When the JTAG interface is not being used, there is no issue.
TMS	3	JTAG Mode (Input)	
TDI	6	JTAG Data In (Input)	
TDO	5	JTAG Data Out (Output)	
WDOG_N	100	Watchdog (Output)	This output pin is used to indicate that a Watchdog Reset or timeout has occurred. The signal is active low and will revert back to high when the processor has gone through the reset vector. Typically this output signal is used to reset or signal external circuitry that the Watchdog timer has timed out.
SP0_RXD	118	Serial Port 0 Receive Data (Input)	This pin is used to receive asynchronous serial data from an externally connected device through serial Port 0. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features.
SP0_TXD	119	Serial Port 0 Transmit Data (Output)	This pin is used to send asynchronous serial data to an externally connected device through serial Port 0. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features.
SP0_RTS_N	116	Serial Port 0 Request to Send (Output)	If enabled, this “flow control” pin is used to signal an external device that the processor has serial data and is requesting to send it through serial Port 0. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features.
SP0_CTS_N	117	Serial Port 0 Clear to Send (Input)	If enabled, this “flow control” input pin is used to signal the processor that an externally connected device is ready to receive serial data through serial Port 0. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features.
SP1_RXD/ DIAG2	84	Serial Port 1 Receive Data (Bi-directional)	This is a multiplexed pin. In the default Serial Port mode, this input pin is used to receive asynchronous serial data from an externally connected device through serial Port 1. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features. The alternate mode of operation for this pin provides support for the Profibus DPV2 Isochron Mode of Operation. In this mode, the pin is an output utilizing the Profibus specific function of “DIAG2”.
SP1_TXD/ DIAG3	85	Serial Port 1 Transmit Data (Output)	This is a multiplexed pin. In the default Serial Port mode, this input pin is used to send asynchronous serial data to an externally connected device through serial Port 1. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features. The alternate mode of operation for this pin provides support for the Profibus DPV2 Isochron Mode of Operation. In this mode, the pin is an output utilizing the Profibus specific function of “DIAG3”.

Name	Pin No.	Type	Description
SP1_RTS_N/ DIAG4	83	Serial Port 1 Request to Send (Output)	This is a multiplexed pin. The default mode for this pin is the RTS Serial Port function. If this “flow control” function is enabled, this output pin is used to signal an external device that the processor has serial data and is requesting to send it through serial Port 1. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features. The alternate mode of operation for this pin provides support for the Profibus DPV2 Isochron Mode of Operation. In this mode, the pin is an output utilizing the Profibus specific function of “DIAG4”.
SP1_CTS_N/ ASPC2_CTS_N	82	Serial Port 1 Clear to Send (Input)	This is a multiplexed pin. The default mode for this pin is the CTS Serial Port function. If this “flow control” function is enabled, this input pin is used to signal the processor that an externally connected device is ready to receive serial data through serial Port 1. See the “Asynchronous Serial Ports” section for more details including enhanced RS-485 and DMA features. The alternate mode of operation for this pin provides support for the Profibus DPV2 Isochron Mode of Operation. In this mode, the pin is an input utilizing the Profibus specific function of “ASPC2_CTS_N”.
OE_N	71	Output Enable (Output)	This pin (Output Enable) is an active low output signal used to access external memory along with the chip select signals. This signal goes active for all external memory access made by the processor. It is typically connected to the output enable pin of static RAM, or Flash device. It provides the tri-state bus disable function to the device when in the inactive or high state.
WRL_N	136	Write Low Byte (Output)	This pin (Write Low Byte) is an active low output signal used to indicate an external memory write access is being performed on the low byte of the system data bus, D07-D00. It is typically connected to the Write enable pin of the external memory device.
WRH_N	141	Write High Byte (Output)	This pin (Write High Byte) is an active low output signal used to indicate an external memory write access is being performed on the upper byte of the system data bus, D15-D08. It is typically connected to the Write enable pin of the external memory device.
UMCS_N	75	Upper Memory Chip Select (Output)	This pin is an active low output signal and indicates to the system that an external memory access is in progress to the upper memory block. The starting address and size of the upper memory block are programmable up to 512 Kbytes in 20-bit mode and up to 8 Mbytes in 24-bit mode. When the system comes out of reset, UMCS_N is active for the top 64 Kbyte memory block. This signal is typically connected to the chip enable of an external non-volatile storage device. Note that the on-chip BOOTROM overrides the very top 2048 bytes of the UMCS_N memory area.

Name	Pin No.	Type	Description
MCS0_N	72	Middle Chip Select 0 (Output)	This pin is an active low output signal and indicates to the system that an external memory access is in progress to the middle memory block range. The internal logic is hard wired so that the MCS0_N pin is always active in the range of 40000h to 7FFFFh in 20-bit mode and 040000h to 7FFFFFh in 24-bit mode. MCS0_N is automatically enabled after a reset or power up.
READY_N	60	External Ready (Input)	This pin is an active low input signal. It is a true asynchronous ready that indicates to the processor that the addressed memory space or I/O device will complete a data transfer. This input contains an internal pull-down resistor, so to always assert the ready condition to the processor, this pin can be left open.
E_COL	77	Ethernet MII Bus Collision (Input)	The PHY asserts this output when a collision is detected. This output remains High for the duration of the collision. This signal is asynchronous and is inactive during full duplex operation.
E_CRS	78	Ethernet MII Carrier Sense (Input)	During half-duplex operation (bit 0.8 = 0), the PHY asserts this output when either transmitting or receiving data packets. During full-duplex operation (bit 0.8 = 1), E_CRS is asserted only during receive. E_CRS assertion is asynchronous with respect to E_RX_CLK. E_CRS is de-asserted on loss of carrier, synchronous to E_RX_CLK.
E_RX_DV	73	Ethernet MII Receive Data Valid (Input)	The PHY asserts this signal when it drives valid data on E_RXD. This output is synchronous to E_RX_CLK.
E_RXD3 E_RXD2 E_RXD1 E_RXD0	56 57 58 59	Ethernet MII Receive Data (Inputs)	E_RXD3-0 are parallel signals that transition synchronously with respect to the E_RX_CLK. E_RXD0 is the least significant bit.
E_RX_ER	54	Ethernet MII Receive Error (Input)	Signals a receive error condition has occurred. This input is synchronous to E_RX_CLK.
E_RX_CLK	62	Ethernet MII Receive Clock (Input)	Clock input for the Ethernet device. 25 MHz for 100 Mbps operation, 2.5 MHz for 10 Mbps operation.
E_TX_EN	74	Ethernet MII Transmit Enable (Output)	The controller asserts this signal when it drives valid data on E_TXD. This signal is synchronized to E_TX_CLK.
E_TXD3 E_TXD2 E_TXD1 E_TXD0	70 69 68 67	Ethernet MII Transmit Data (Outputs)	TXD3-0 are parallel data signals that are driven by the Ethernet Controller. TXD<3:0> will transition synchronously with respect to the E_TX_CLK. E_TXD0 is the least significant bit.
E_TX_ER	50	Ethernet MII Transmit Error (Output)	Signals a transmit error condition. This signal is synchronized to E_TX_CLK.
E_TX_CLK	65	Ethernet MII Transmit Clock (Input)	E_TX_CLK is sourced by the PHY in both 10 and 100 Mbps operations. 2.5 MHz for 10 Mbps operation, 25 MHz for 100 Mbps operation.

Name	Pin No.	Type	Description
E_MDIO	44	Ethernet Management Data (Bi-directional)	Bi-directional serial data channel for PHY/STA communication.
E_MDC	45	Ethernet Management Clock (Output)	Clock output for the E_MDIO serial data channel.
PIO31/ LED3_N/ Address Mode Sel	88	LED Control 3 (Bi-directional)	This is a programmable multifunction pin. It can be used with the normal function or can be programmed for alternate general-purpose I/O use. This pin is also takes on a special function only during reset, Address Mode Select. It is sampled internally by the processor when going through the reset state to select the processor mode. Address Mode Sel: When left open or pulled up to a logic high during hardware reset, it places the processor into 20-bit address mode. When connected to Ground during hardware reset, it places the DSTni-LX into 24-bit address mode. LED3_N: This is the Normal function for this pin. It is typically used to drive a status LED but can be used freely. PIO31: Can be programmed as a general-purpose digital I/O pin through the PIO Mode and Direction registers. There are three options to choose from, Normal, Input, or Output. Note that regardless of the mode selected, this pin always contains a weak internal pull-up circuit.
PIO30/LED2_N/ Watchdog Disable_N	89	LED Control 2 (Bi-directional)	This is a programmable multifunction pin. It can be used with the normal function or can be programmed for alternate general-purpose I/O use. This pin is also takes on a special function only during reset, Watchdog Disable. It is sampled internally by the processor when going through the reset state. Watchdog Disable_N: When this pin is held low during power up or reset, it causes the watchdog timer to be disabled. LED2_N: This is the Normal function for this pin. It is typically used to drive a status LED but can be used freely. PIO30: Can be programmed as a general-purpose digital I/O pin through the PIO Mode and Direction registers. There are three options to choose from, Normal, Input, or Output. Note that regardless of the mode selected, this pin always contains a weak internal pull-up circuit.
PIO29/LED1_N	104	LED Control 1 (Bi-directional)	This is a programmable multifunction pin. It can be used with the normal function or can be programmed for alternate general-purpose I/O use. LED1_N: This is the Normal function for this pin. It is typically used to drive a status LED but can be used freely. During execution of the internal Boot ROM code, this pin and LED0 are used to indicate system status. PIO29: Can be programmed as a general-purpose digital I/O pin through the PIO Mode and Direction registers. There are three options to choose from, Normal, Input, or Output. Note that regardless of the mode selected, this pin always contains a weak internal pull-up circuit.

Name	Pin No.	Type	Description
PIO28/LED0_N	105	LED Control 0 (Bi-directional)	This is a programmable multifunction pin. It can be used with the normal function or can be programmed for alternate general-purpose I/O use. LED0_N: This is the Normal function for this pin. It is typically used to drive a status LED but can be used freely. During execution of the internal Boot ROM code, this pin and LED1 are used to indicate system status. PIO28: Can be programmed as a general-purpose digital I/O pin through the PIO Mode and Direction registers. There are three options to choose from, Normal, Input, or Output. Note that regardless of the mode selected, this pin always contains a weak internal pull-up circuit.
PIO27	106	General Purpose I/O Pin (Bi-directional)	This is a general purpose Programmable I/O pin. PIO27: Can be programmed as a general-purpose digital I/O pin through the PIO Mode and Direction registers. There are three options to choose from, Normal, Input, or Output. Note that regardless of the mode selected, this pin always contains a weak internal pull-down circuit.
PIO26/DPCS_N	122	I/O – DPRAM Chip Select (Bi-directional)	DPCS_N: Dual Port RAM Chip Select. When used in this normal mode, this active low input pin is used during an external Read or Write Access to enable data transfers to and from the “External-Side” of the internal 8k dual port RAM. Note this signal must be used in conjunction with the DPRAM Data Bus, Address Bus, and one of the following control signals, DPWR_N, or DPOE_N to perform a valid data transfer.
PIO25/DPSS_N	123	I/O – DPRAM Semaphore Select (Bi-directional)	DPSS_N: Dual Port RAM Semaphore Select. When used in this normal mode, this active low input pin is used during an external Read or Write Access to obtain or release one of the eight semaphore flags contained in the dual port RAM interface. Note this signal must be used in conjunction with the DPRAM Data Bus, Address Bus, and one of the following control signals, DPWR_N, or DPOE_N to perform a valid semaphore transfer.
PIO24/DPWR_N	126	I/O – DPRAM Memory Write (Bi-directional)	DPWR_N: Dual Port RAM Memory Write. When used in this normal mode, this active low input pin is used during an external Write Access to enable data transfers from the DPRAM Data bus to the “External-side” port of the internal 8k bytes of dual-port memory. Note this signal must be used in conjunction with the DPRAM Data Bus, Address Bus and the DPCS_N to perform a valid data transfer.
PIO23/DPOE_N	127	I/O – DPRAM Output Enable (Bi-directional)	DPOE_N: Dual Port RAM Output Enable. When used in this normal mode, this active low input pin is used during an external Read Access to enable data transfers from the “External-side” port of the internal 8k bytes of dual-port memory to the DPRAM Data bus. Note this signal must be used in conjunction with the DPRAM Data Bus, Address Bus and the DPCS_N to perform a valid data transfer.

Name	Pin No.	Type	Description
PIO22/DPINT_N	130	I/O – DPRAM External Port Interrupt (Bi-directional)	DPINT_N: Dual Port RAM External Port Interrupt. When used in this normal mode, this active low output pin is generally used to signal the external "External-side" user of the DPRAM that the internal-side port has information to be read or service is required. Note this interrupt is fully controlled by the user software and can be used to indicate any user-defined action. This signal will revert to the inactive state when the "External-side" makes a READ access from DPRAM address 1FFEh. The "External-side" user is also given the ability to generate an interrupt that will be sent to the internally connected "Internal-side" interrupt logic. To generate this interrupt, the "External-side" user simply writes to location 1FFFh. The "Internal-side" user resets and acknowledges this interrupt by making a READ access from DPRAM address 1FFFh.
PIO21/ DPBUSY_N	131	I/O – DPRAM Busy (Bi-directional)	DPBUSY_N: Dual Port RAM Busy. When used in this normal mode, this active low output pin is used to signal the external "External-side" user of the DPRAM that a simultaneous access of a memory location has occurred and the Internal side currently has valid access control. Under this Busy condition, the "External-side" user will not be guaranteed valid data, so interface logic must take this into account. Typically this is handled by simply extending the current access until the busy condition is complete at which time the access is able to complete with valid data. Note that if the built in semaphores are used and managed correctly by the software on both sides, the Busy condition can be completely eliminated thus eliminating the need for external hardware logic.
PIO20/DPA12 PIO19/DPA11 PIO18/DPA10 PIO17/DPA09 PIO16/DPA08 PIO15/DPA07 PIO14/DPA06 PIO13/DPA05 PIO12/DPA04 PIO11/DPA03 PIO10/DPA02 PIO09/DPA01 PIO08/DPA00 PIO07/DPD7 PIO06/DPD6 PIO05/DPD5 PIO04/DPD4 PIO03/DPD3 PIO02/DPD2 PIO01/DPD1 PIO00/DPD0	133 134 135 139 142 143 144 145 146 150 152 155 156 159 7 9 10 13 14 25 26	I/O – DPRAM ADR and DATA (Bi-directional)	DPA12-DPA00: Dual Port RAM External Port Address Lines. When used in the normal mode, these 13 input signals make up the Address Bus for accessing the external "External-side" locations of the DPRAM. DPA12 is the MSB while DPA00 is the LSB of the Address Bus. These address lines are used in conjunction with the DPRAM Data Bus and control signals enabling full access to the "External-side" memory and semaphore locations. DPD7-DPD0: Dual Port RAM Data Bus. When used in the normal mode, these 8 Bi-directional signals make up the Data Bus for accessing the external "External-side" locations of the DPRAM. DPD7 is the MSB while DPD0 is the LSB of the Data Bus. These data lines are used in conjunction with the DPRAM Address Bus and control signals enabling full access to the data on "External-side" memory and semaphore locations.

Name	Pin No.	Type	Description
PCS6_N	76	External Peripheral Chip Select (Output)	This pin is a dedicated active low output signal and indicates to the system that an external I/O access is in progress to this I/O memory block. The starting address is determined by the Peripheral Base Address (PBA) + 600h, which is set in the PACS register. The size of the I/O block is fixed at 256 bytes. This signal is typically connected to the chip enable of any user-selected device that contains less than or equal to 256 bytes of data.
CAN0_TX	95	CAN Bus 0 Transmit (Output)	This pin is a dedicated output signal used for transmitting CAN type protocol messages on channel CAN-0. +3.3 volt output. (See Note) For more details, see the CAN Controller section.
CAN0_RX	94	CAN Bus 0 Receive (Input)	This pin is a dedicated input signal used for receiving CAN type protocol messages on channel CAN-0. This pin must be current limited. (See Note) For more details, see the CAN Controller section.
CAN1_TX	91	CAN Bus 1 Transmit (Output)	This pin is a dedicated output signal used for transmitting CAN type protocol messages on channel CAN-1. +3.3 volt output. (See Note) For more details, see the CAN Controller section.
CAN1_RX	90	CAN Bus 1 Receive (Input)	This pin is a dedicated input signal used for receiving CAN type protocol messages on channel CAN-1. This pin must be current limited. (See Note) For more details, see the CAN Controller section.
PROFI_TX	113	Profibus Transmit Data (Output)	This pin is a dedicated output signal used for transmitting Profibus type protocol messages. +3.3 volt output. (See Note) For more details, see the Profibus Controller section. (DSTni-LX002 only)
PROFI_RX	109	Profibus Receive Data (Input)	This pin is a dedicated input signal used for receiving Profibus type protocol messages. This pin must be current limited. (See Note). For more details, see the Profibus Controller section.(DSTni-LX002 only)
PROFI_ENB	114	Transmit Enable (Output)	This pin is a dedicated output signal used for enabling the external Profibus transceivers when the controller is in the “transmit” mode. This signal is typically tied directly to the enable pin of the external transceiver. +3.3 volt output. (See Note) For more details, see the Profibus Controller section.(DSTni-LX002 only)
TMR0_OUT	47	Timer 0 Output (Output)	This pin is a dedicated output signal that is logically connected to TIMER0, an internal 16-bit programmable timer. The duty cycle and rate of this signal is controlled through the Timer Registers. See the Timer section for more details.
TMR0_IN	46	Timer 0 Input (Input)	This pin is a dedicated input signal that can be programmed as the clock input to TIMER0, an internal 16-bit programmable timer. This pin is typically connected to an external clock when the user wants to use a different time base other than the internally supplied clock. Note that if this pin is not used, it must be pulled to logic high externally. See the Timer section for more details.

Name	Pin No.	Type	Description
INT5	29	External Interrupt (Input)	This is a dedicated input pin that can be used to indicate to the processor that an external device requires servicing through an interrupt vector. The interrupt specific parameters for this pin are settable through the Interrupt control registers.
DFLASH_N	24	SPI Slave 0 Select: Serial Flash (Output)	This is a dedicated active low signal used with the SPI Port. It is normally tied directly to the chip select of an externally supplied Serial Data Flash. This signal is controlled through the SPI Slave Select Register. Note this pin requires an external pull-up resistor.
MOSI	33	SPI:Master Out / Slave In (Bi-directional)	This is a dedicated bi-directional signal used with the SPI Port. It is normally tied directly to the Serial Input pins of externally supplied SPI slave devices. This signal is controlled through the SPI Data and Control Registers. Note this pin requires an external pull-up resistor.
MISO	35	SPI:Master In / Slave Out (Bi-directional)	This is a dedicated bi-directional signal used with the SPI Port. It is normally tied directly to the Serial output pins of externally supplied SPI slave devices. This signal is controlled through the SPI Data and Control Registers. Note this pin requires an external pull-up resistor.
SCLK	38	SPI:Master Clock Out / Slave Clock Input (Bi-directional)	This is a dedicated bi-directional signal used with the SPI Port. It currently is only supported in “master” mode. In master mode, this pin is an output that supplies the programmed SPI clock signal. It is normally tied directly to the Serial Clock input pins of externally supplied SPI slave devices. This signal is controlled through the SPI Data and Control Registers. Note this pin requires an external pull-up resistor.
MSCS_N	39	SPI:Master Collision Input	This is a dedicated active low input signal used with the SPI Port. It functions as the SPI Port, Master Collision Input for use with multiple masters. When driven low, an SPI collision will be detected. Note this pin requires an external pull-up resistor.
GND	23, 40, 52, 63, 80, 99, 111, 120, 138, 148, 160	Ground	Logic Ground.
VCC	1, 18, 41, 51, 64, 81 98, 110, 121, 137, 147	+3.3V	Supply voltage, +3.3VDC I/O Power.
VCC2	4, 34, 53 61,101, 112, 140, 149	+2.5V	Supply voltage, +2.5VDC Core Power.
VSS_OSC	19	Ground	Ground for Internal Oscillator. (Must be connected to Ground)
VCC_OSC	22	+3.3V	+3.3V Supply voltage for internal oscillator. (Must be connected to +3.3V.)

4. Timing Diagrams

4.1 External Clock

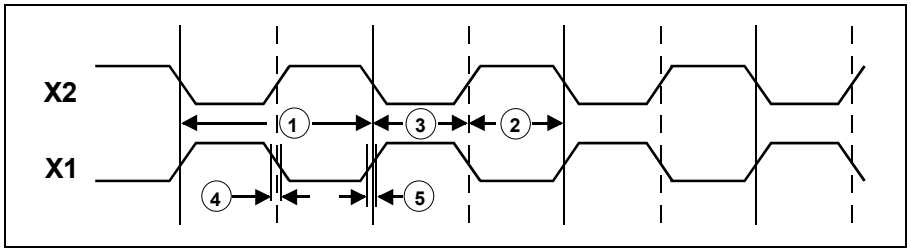


Figure 4-1: External clock timing

No.	Symbol	Description	Min	Max	Unit
1	t_{CKIN}	X1 Period	20.8		ns
2	t_{CLCK}	X1 Low Time	8		ns
3	t_{CHCK}	X1 High Time	8		ns
4	t_{CKHL}	X1 Fall Time		5	ns
5	t_{CKLH}	X1 Rise Time		5	ns

Table 4-1: External clock timing

4.2 External Memory Read

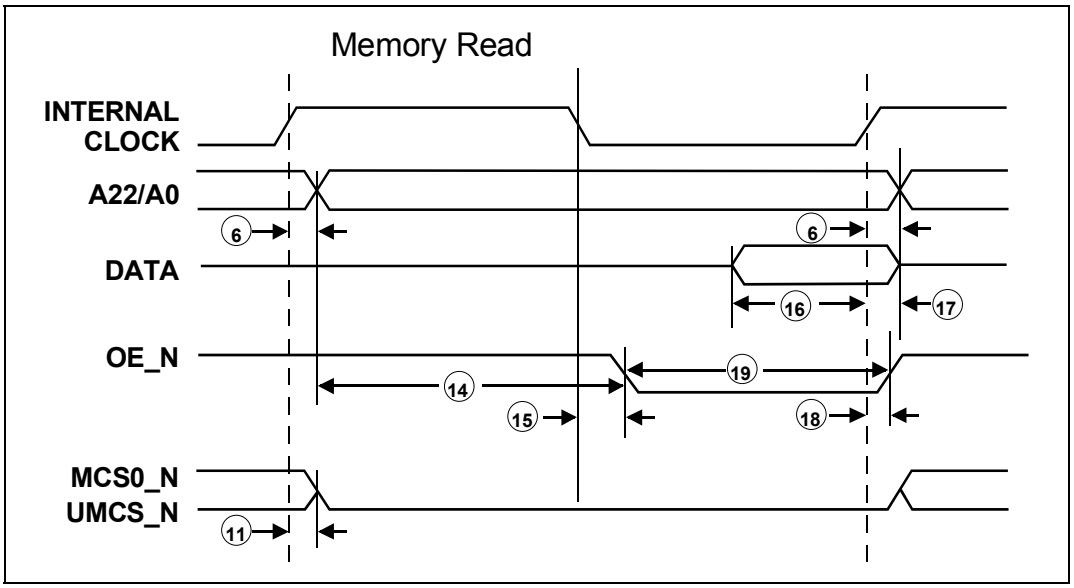


Figure 4-2: External memory read timing

No.	Symbol	Description	Min	Max	Unit
6	t_{CHAV}	X1 high to Address Available			ns
14	t_{AVRL}	Address Available to OE_N			ns
15	t_{CLRL}	Clock Low to OE_N			ns
16	t_{DVCH}	Data Setup			ns
17	t_{CHDX}	Data Hold			ns
18	t_{CHRH}	OE_N Inactive Delay			ns
11	t_{CHCSV}	X1 High to MCS0_N Low			ns
19	t_{RLRH}	OE_N Pulse Width			ns

Table 4-2: External memory read timing

4.3 External Memory Write

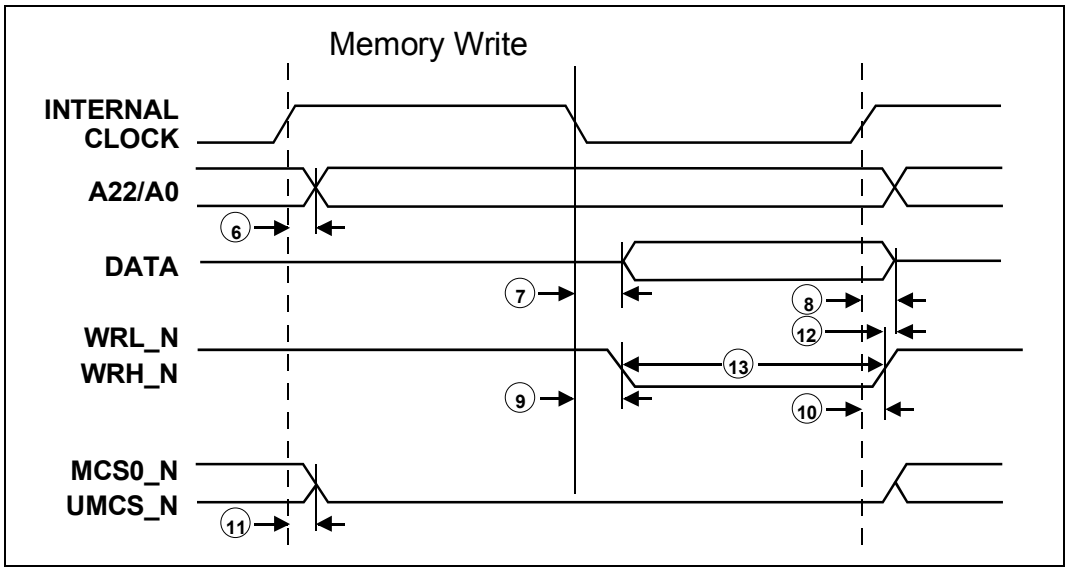


Figure 4-3: External memory write timing

No.	Symbol	Description	Min	Max	Unit
6	t_{CHAV}	X1 high to Address Available			ns
7	t_{CLDV}	X1 Low to Data Available			ns
8	t_{CLDOX}	Data Hold Time			ns
9	t_{CLCTV}	X1 Low to WR Low			ns
10	t_{CHCTX}	X1 High to WR High			ns
11	t_{CHCSV}	X1 High to MCS0_N Low			ns
12	t_{WHDX}	Data Hold after WR_N			ns
13	t_{WLWH}	WR_N Pulse Width			ns

Table 4-3: External memory write timing

5. Specifications

5.1 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_A	Operating Temperature	Industrial	-40		+105	°C
T_{ST}	Storage Temperature		-65		+150	°C
T_J	Junction Temperature				+135	°C

Table 5-1: Absolute maximum ratings

5.2 Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V DD	DC Supply Voltage	Core and Std. I/Os	2.25	2.5	2.75	V
V DD3	DC Supply Voltage	3V Interface I/Os	3	3.3	3.6	V
V I	DC Input Voltage		0		V DD3	V
V O	DC Output Voltage		0		V DD3	V
V I 5	DC Input Voltage	5V Tolerant I/O	0		V DD3 + 2.0V	V
V O 5	DC Output Voltage	5V Tolerant I/O	0		V DD3 + 2.0V	V

Table 5-2: Operating conditions

5.3 DC Characteristics

Symbol	Parameter		Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{cc}	V
V_{IL}	Low-level input voltage		0	0.8	
V_{OH}	High-level output voltage (I_{OH} = -2.5 mA)	Commercial	2.4		
V_{OL}	Low-level output voltage (I_{OL} = +3.0 mA)			0.4	
V_{OH}	High-level output voltage (I_{OH} = -2.0 mA)	Industrial	2.4		
V_{OL}	Low-level output voltage (I_{OL} = +3.0 mA)			0.4	
$I_{CC(Core)}$	Supply current, 2.5V			300	mA
$I_{CC\ (I/O)}$	Supply current, 3.3V			TBD	mA
I_L	Input or output leakage current (V_{IN} = V_{CC} or GND)		-10	10	uA

Table 5-3: DC characteristics

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

6. Ordering Information

Ordering Code	Description	Speed (MHz)	Package	Temperature (Operating)
DSTNI-LX-001	DSTni-LX without PROFIBUS DP	48	160-pin LQFP	-40°C to 105°C
DSTNI-LX-002	DSTni-LX with PROFIBUS DP (Available Q1 2002)	48	160-pin LQFP	-40°C to 105°C

Table 6-1: Ordering information

7. Packaging Information

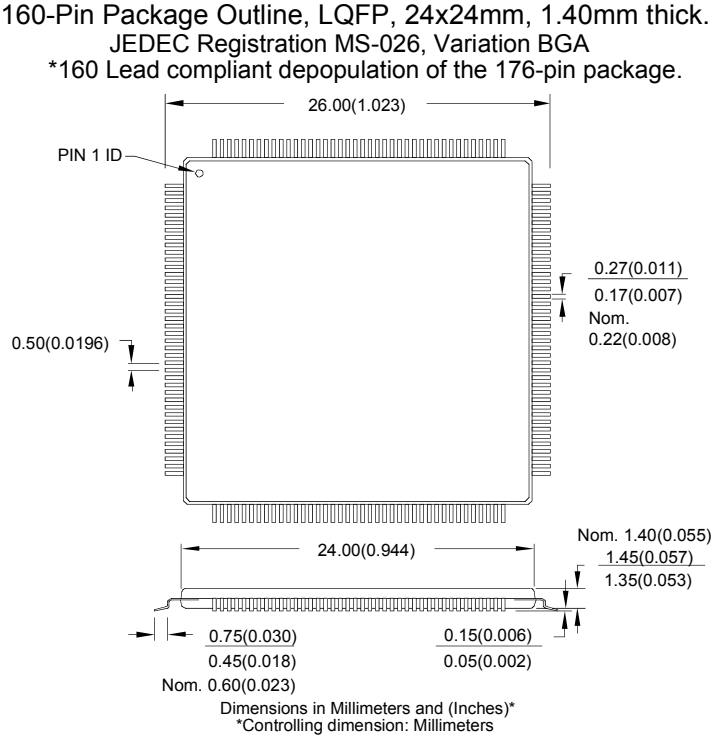


Figure 7-1: DSTni-LX 160-Pin Package

For More Information:

For more information on this product and all of the products and services provided by Lantronix, please visit us at www.lantronix.com. For more immediate needs, you can contact us directly at any of our corporate and regional headquarters. A complete listing of all our sales offices can be found at our web site.

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