- DL6035 With External GTL/GTLP Reference Voltage
- Enables GTL or GTLP Operation
- Every I/O Programmable to TTL or GTL/GTLP
- Eliminates the Need for GTL Translators
  - Saves Cost
  - Saves Board Space
  - Saves Translator Delays
  - Saves Power
- Provides Higher Current Drive
  - 48 mA in GTLP mode
- Retains All the High-Speed Features of the DL6035

The DL6035X enables the user to provide an external GTL/GTLP reference voltage to the high-speed DL6035 Fast Field Programmable Gate Array. This enables the user to set the GTL/GTLP reference by applying the required voltage to a special pin on the device.

This external reference voltage enables the device to connect directly to GTL or GTLP signals eliminating the need for external translator devices. This results in a cost savings as well as savings in board space, power consumption and delay.

All other features and specifications of the DL6035X are identical to the DL6035 including the high-speed active repeater architecture, 2 PLLs, 150 ps clock skew and ability to implement 125 MHz FIFO buffers.

Device	Gates	Logic Blocks	Max User RAM Bits	Flip Flops	Clock Trees	I/O Blocks
DL6035X	35,000	1,024	32,768	2,560	10	253

Table 1: DL6035X

Product Specifications

Recommended Operating Conditions

Symbol	Description	Min	Max	Unit
V_{CC}	Supply voltage relative to GND			
	Commercial 0° C to 85° C junction	3.14	3.47	V
	Industrial –40° C to 100° C junction	3.0	3.6	V
$V_{TT\ (GTL)}$	GTL terminating voltage relative to GND			
	Commercial 0° C to 85° C junction	1.14	1.26	V
	Industrial –40° C to 100° C junction	1.08	1.32	V
$V_{TT\ (GTLP)}$	GTLP terminating voltage relative to GND			
	Commercial 0° C to 85° C junction	1.43	1.58	V
	Industrial –40° C to 100° C junction	1.35	1.65	V
V_{REF} (2)	GTL/GTLP reference voltage relative to GND(2)	2/3 V_{TT} -5%	2/3 V_{TT} +5%	

Table 2: Recommended Operating Conditions

Notes:

(1) All junction temperatures above those listed as Operating conditions are illegal.

(2) This voltage should be applied to I/O_131 which is the V_{REF} pin on the DL6035X device.

DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IMAX} (5)	Max. voltage applied to input	-	5.5	V	
V_{CMAX} (6)	Max. voltage applied to clock inputs	-	3.6	V	
$V_{IH(TTL)}$	High-level Input Voltage	2.0	V_{CC} + 0.3	V	
$V_{IL(TTL)}$	Low-level input voltage	0.0	0.8	V	
$V_{IH(CMOS)}$	High-level Input Voltage	$0.7V_{CC}$	V_{CC}	V	
$V_{IL(CMOS)}$	Low-level input voltage	0.0	$0.3V_{CC}$	V	
$V_{IH(GTL\ or\ GTLP)}$	High-level Input Voltage	V_{REF} + 0.2	V_{TT}	V	
$V_{IL(GTL\ or\ GTLP)}$	Low-level input voltage	0.0	V_{REF} - 0.2	V	
$V_{IH(LVPECL)}$	High-level input voltage	2.135	2.420	V	When V_{CC} = 3.3V
$V_{IL(LVPECL)}$	Low-level input voltage	1.490	1.825	V	When V_{CC} = 3.3V
$V_{OH\ (TTL)}$	High level output voltage	2.4	-	V	V_{CC} min, See note 2 for I_{OH}
$V_{OL(TTL)}$	Low level output voltage (1,2)	-	0.4	V	V_{CC} min, See note 2 for I_{OL}
$V_{OH(GTL)}$	High level output voltage (3,4)	-	V_{TT}	V	
$V_{OL(GTL)}$	Low level output voltage (3)	-	0.4	V	I_{OL} = 20 mA, V_{TT} max
$V_{OH(GTLP)}$	High level output voltage (3,4)	-	V_{TT}	V	
$V_{OL(GTLP)}$	Low level output voltage (3)	-	0.55	V	I_{OL} = 40 mA, V_{TT} max
I_{CC}	Quiescent current (without RAM)	-	10	mA	V_{CC} = MAX; All I/O's open
I_{IL}	Leakage Current	-10	+10	µA	
C_{IN}	Input capacitance	-	8.5	pF	BGA package

Table 3: DC Electrical Characteristics

Notes:
(1) With 50% of the outputs simultaneously sinking 16 mA each.
(2) Sink/Source current in TTL mode varies with slew rate setting:
Fast slew rate: sink/source current = 16 mA (at V_{CC} min)
Medium slew rate: sink/source current = 11 mA (at V_{CC} min)
Slow slew rate: sink/source current = 5 mA (at V_{CC} min)
(3) Sink current in GTL mode = 20 mA. Sink current in GTLP mode = 40 mA. Source current is provided by external pull-up resistor.
(4) V_{REF} = 2/3 V_{TT} +/- 5%
(5) All I/O pins except LV-PECL capable inputs are 5 volt tolerant.
(6) The maximum voltage applied to LV-PECL capable input pins should not exceed this value, even if they are used as single ended TTL I/O.
(7) All GTL outputs should be terminated to V_{TT} through a 50 ohm resistor.
(8) All GTLP outputs should be terminated to V_{TT} through a 25 ohm termination configured as a pair of 50 ohm resistors.

Input and Output Block Switching Characteristics

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input buffer combinatorial delay	T_{INPD}	3.7	3.2	2.9	ns
Input Register Set-up Time (global clock)	T_{INIS1}	1.9	1.6	1.4	ns
Input Register Hold Time (global clock)	T_{INIH1}	0	0	0	ns
Input Register Clock to Output (global clock)	T_{INCO1}	3.0	2.6	2.3	ns
Output buffer combinatorial delay (no load)(2,3)	T_{OUTIS1}	5.2	4.3	3.8	ns
Output Register Set-up Time (global clock)	T_{OUTIS2}	3.5	2.3	2.0	ns
Output Register Hold Time (global clock)	T_{OUTIH1}	0	0	0	ns
Output Register Clock to Output (global clock, no load)(2,3)	T_{OUTCO1}	3.6	2.9	2.6	ns
I/O Register Clock Enable Setup Time	T_{CES1}	2.4	2.0	1.6	ns
I/O Register Clock Enable Hold Time	T_{CEH1}	0	0	0	ns
Input Register GSR set/reset delays	T_{GSRI}	3.0	2.6	2.3	ns
Output Register GSR set/reset delays	T_{GSRO}	3.5	3.0	2.7	ns
Input Register GSR set/reset setup time	T_{GSRIS1}	0.5	0.4	0.3	ns
Output Register GSR set/reset setup time	T_{GSROS1}	0.5	0.4	0.3	ns
OE to Pad Active (no load)(2,3)	T_{3SOE}	4.5	3.7	3.3	ns
OE to Pad HI-Z (no load)(2,3)	T_{3SOD}	4.5	3.7	3.3	ns

Table 4: Input and Output Buffer Parameters (I/O Set to TTL)

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Output delays are specified with no load. Add the following delays to adjust for loading.
Fast Slew Rate: 12 ps/pf
Medium Slew Rate: 25 ps/pf
Slow Slew Rate: 55 ps/pf
(3) The maximum loading for outputs switching at the same time in the same direction is shown below. One power/ground pair is provided for each 8 I/O on the device.
Fast Slew Rate: 200 pf between each power/ground pair
Medium Slew Rate: 300 pf between each power/ground pair
Slow Slew Rate: 400 pf between each power/ground pair
(4) Each output pin has individual slew rate control.

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input buffer combinatorial delay	T_{INPD}	4.7	4.0	3.6	ns
Input Register Set-up Time (global clock)	T_{INIS1}	3.0	2.4	2.2	ns
Input Register Hold Time (global clock)	T_{INIH1}	0	0	0	ns
Input Register Clock to Output (global clock)	T_{INCO1}	4.0	2.6	2.3	ns
Output buffer combinatorial delay (no load)(2)	T_{OUTIS1}	4.5	3.6	3.2	ns
Output Register Set-up Time (global clock)	T_{OUTIS2}	3.5	2.3	2.0	ns
Output Register Hold Time (global clock)	T_{OUTIH1}	0	0	0	ns
Output Register Clock to Output (global clock, no load)(2)	T_{OUTCO1}	2.8	2.3	2.1	ns
I/O Register Clock Enable Setup Time	T_{CES1}	2.4	2.0	1.6	ns
I/O Register Clock Enable Hold Time	T_{CEH1}	0	0	0	ns
Input Register GSR set/reset delays	T_{GSRI}	3.0	2.6	2.3	ns
Output Register GSR set/reset delays	T_{GSRO}	2.9	2.4	2.2	ns
Input Register GSR set/reset setup time	T_{GSRIS1}	0.5	0.4	0.3	ns
Output Register GSR set/reset setup time	T_{GSROS1}	0.5	0.4	0.3	ns
OE to Pad Active (no load)(2)	T_{3SOE}	4.5	3.7	3.3	ns
OE to Pad HI-Z (no load)(2)	T_{3SOD}	4.5	3.7	3.3	ns

Table 5: Input and Output Buffer Parameters (I/O Set to GTL or GTLP)

Notes:
(1) All delays are specified over commercial voltage and temperature range.
(2) Output delays are specified with no load. Add the following delays to adjust for loading.
GTL: 7 ps/pf
GTLP: 4 ps/pf

Description	Symbol	Speed Grade			Units
		-E	-F	-G	
		Max	Max	Max	
Input buffer combinatorial delay	T_{INPD}	4.7	4.0	3.6	ns
Input Register Set-up Time (global clock)	T_{INIS1}	3.0	2.4	2.2	ns
Input Register Hold Time (global clock)	T_{INIH1}	0	0	0	ns
Input Register Clock to Output (global clock)	T_{INCO1}	4.0	2.6	2.3	ns
I/O Register Clock Enable Setup Time	T_{CES1}	2.4	2.0	1.6	ns
I/O Register Clock Enable Hold Time	T_{CEH1}	0	0	0	ns
Input Register GSR set/reset delays	T_{GSRI}	3.0	2.6	2.3	ns
Input Register GSR set/reset setup time	T_{GSRIS1}	0.5	0.4	0.3	ns

Table 6: Input Buffer Parameters (I/O Set to PECL or LVDS)

Notes:
(1) All delays are specified over commercial voltage and temperature range.

Pin Description

DL6035X Pin Assignments

DL6035X pin assignments are identical to the DL6035 except for I/O_131 which is used for the external GTL reference voltage (V_{REF}).

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