CX3000 0.35µ CMOS Gate Array Family

Introduction

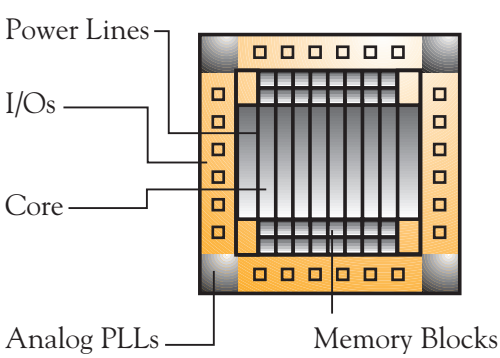
The CX3000 0.35µ CMOS technology is a high performance gate array product family, offering rapid prototype turnaround time and low-cost, high-volume production. These benefits are achieved using Chip Express' unique architecture and manufacturing through our world-class foundry partner, Chartered Semiconductor (Singapore).

The CX3000 technology features high density (10K gates/mm^2) and logic capacity of up to 1.5M gates. This high density results from utilizing a four-layer metal interconnection, enabling competitive prices for high-volume production. Additionally, the CX3000 technology features extremely low power dissipation of 0.3µW/MHz/gate, and a unique voltage flexibility utilizing a dual-oxide process that allows operating with solely 5V Vcc. This product family offers up to four embedded analog PLLs.

Embedded Configurable Memory

An inherent feature of CX3000 technology is the availability of high performance configurable embedded memory. The CX 3000 product family offers synchronous memory ranging from 8K to 416K bits of single-port or dual-port SRAM or ROM with up to 52 different block configurations. The high-speed programmable SRAM is capable of operating at speeds in excess of 360MHz @ 3.3V for worst case (single-port or dual-port). The CX3000 technology also includes a BIST (Built-In Self Test) that enables the testing of the embedded memory and ensures high fault coverage.

Device Outline



Features

Density	• 40K to 1.5M logic gates (2 input NAND gate equivalent)
Power	• Low power dissipation 0.3µW/MHz/Gate @3.3V
Voltage	• Solely 5V, solely 3.3V, mixed 3.3V/5V
Performance	• High speed 8x8 multiplier with 5.6ns cycle (one stage pipeline)
I/Os	• Rich I/O libraries (2308 cells) • Up to 592 I/Os • All I/O pads can be used for power and/or ground • 5V drive or 3.3V operation with 5V tolerance, mixed 3.3V & 5V • 3.3V PCI-compliant at 66MHz • Differential input support modes such as GTL and USB
Memory	• Embedded synchronous single or dual-port SRAM or ROM • Configurable 8K to 416K bits • High speed-360MHz SRAM @ 3.3V for worst case
Analog PLL	• 3 or 4 APLLs with clock synchronization and multiplication of 200MHz @ 3.3V
ATPG	• Built-in scan capability with minimum impact on performance and 1-2% utilization impact
CAE Tools	• DRC utilities (Check_all) • Clock Tree Synthesis (CTS) with <500ps clock-skew • Automatic cross-talk handling • BIST for memory testing

ASIC Services

Laser Prototypes - CX3001
One-day turnaround time is available for LPGA (Laser Programmable Gate Array) prototypes using the Chip Express *QuICk*® laser micro-machining system, which rapidly customizes one die at a time.

Low-Mid Volume - CX3001
One-week turnaround time is available for low volume gate array production with the proprietary *OneMask*® technology. Customization is done using single mask, single wafer processing.
One-month lead-time for mid-volume production is available with the *TwoMask*™ technology. No conversion or additional engineering development is required after the prototyping phase is complete.

High Volume Production - CX3002
Two-month lead-time for smooth migration to a smaller die size for price reduction is available for high volume production. This is accomplished using the *HardArray*™ technology with a multi-mask process that provides high gate utilization.

Design Services

Chip Express provides the following optional design services:

IP Cores
With its ***CorExpress***™ program, Chip Express has partnered with leading core suppliers like Mentor Graphics/ Inventra Group, Sierra Research and Virtual Chips to provide system designers with pre-verified IP blocks (PCI, micro-controllers, ethernet controllers, bus interface, etc.). In addition, Chip Express has access to some Lucent IP cores.

ATPG
Recognizing that testability is a critical issue in today's large and complex ASIC designs, Chip Express offers ATPG implementation that is based on full-scan fault coverage methodology. This is accomplished in the CX3000 technology with minimum performance impact and only 1-2% utilization impact. This service can be provided as an add-on at the end of the design.

RTL Sign-off
Chip Express has developed an RTL sign-off flow to further shorten time-to-market, where instead of submitting the gate-level netlist, the designer can now interface at a higher level of abstraction.

Conversion
Chip Express offers conversion of FPGA (Actel, Altera, Xilinx) or gate array designs from other ASIC vendors (LSI Logic, VLSI) to Chip Express libraries. Functionality of converted designs is maintained.

Furthermore, the CX3000 technology features the unique capability of converting 5V gate array designs from older process geometries to 0.35µ technology for reduced production costs.

Design Kits

CX3000 libraries for popular EDA design environments are available at no charge at the Chip Express web-site.

	Tool	Format	Vendor	Platform
Synthesis	Design Compiler	Verilog/ VHDL	Synopsys	Sun/HP
	Leonardo†	Verilog/ VHDL	Exemplar	Sun/PC
	BuildGate†	Verilog/ VHDL/ EDIF	Ambit	Sun/HP
Simulation	Verilog XL	Verilog	Cadence	Sun/HP
	VSS	Vital95 VHDL	Synopsys	Sun/HP
	Modeltech†	Vital95 VHDL	Mentor	Sun/HP
	Modeltech	Vital95 VHDL	Mentor	PC - NT
Static Timing	Design Time	Verilog/ VHDL	Synopsys	Sun/HP
ATPG*	Turbocheck	Verilog	SynTest	Sun
	Test Compiler	Verilog/ VHDL	Synopsys	Sun/HP

* Turbocheck is available upon special request
† Consult factory for availability

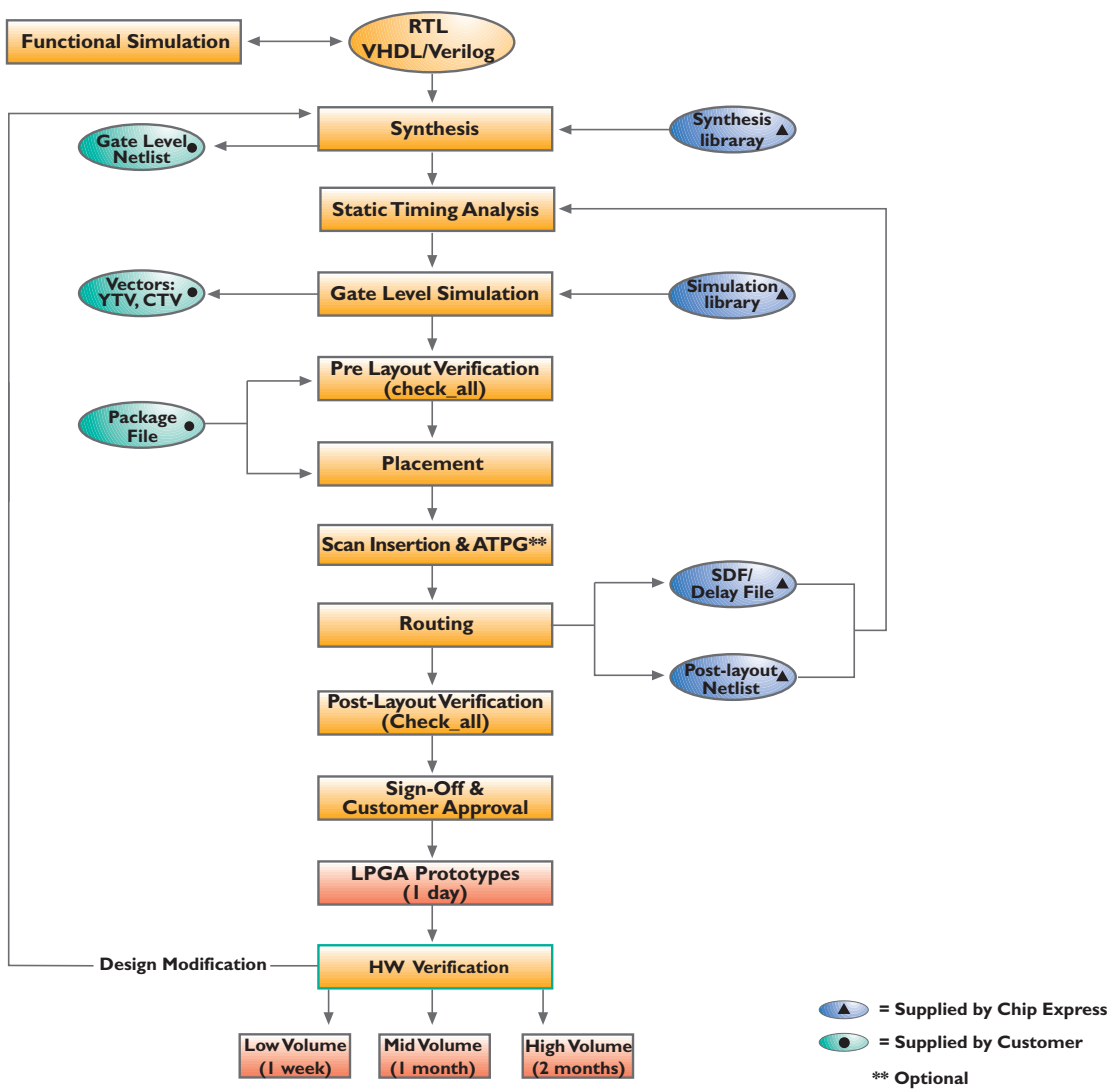
Input, Output & Bi-directional Cells

The libraries for the CX3000 technology contain a large selection of input, output and bi-directional cells facilitating a wide range of designs. Input cells can be personalized with internal pull-up or pull-down resistors and with or without hysteresis. If required, outputs can be connected in parallel to provide increased drive capability. There can be several sections of 3.3V and 5V I/O interfaces. The CX3000 technology features PCI compliance and differential input support such as GTL and USB.

Mixed Voltage Features

Using the dual-oxide process the CX3000 product family enables mixed 3.3V/5V I/Os and 5V tolerance. The CX3000 technology core device operates at 3.3V. The I/O macros can be 3.3V I/O or 5V I/O. When 3.3V supply is not possible, the Chip Express special Voltage Regulator is used. This Special Circuit enables 5V-based designs to be implemented in CX3000 devices.

LPGA Design Flow*



* For a detailed Design Flow please check the CX Design Manual

Product Families

The CX3000 technology is comprised of two gate array families: the CX3001, designed for fast prototyping and low volume production, implemented in three-layer metal technology, and the CX3002, aimed at cost reduction for high volume production, implemented in four-layer metal technology.

Architecture

The basic building block of the CX3000 technology is a module that is configurable to operate in a very broad range of simple and complex circuit functions and combinations. This modular structure is an innovative approach combining improved silicon utilization and low power consumption with a fast-turn manufacturing capability. Each module is made up of three multiplexers and one AND gate and is logically equivalent to three or four logic gates (depending on the application).

CX3001 Family - Prototypes & Low/Mid Volume

Base Array	I/Os	Pads	Memory Bits	No. of Configur-ations	Modules/ Logic Cells	Max Logic Gates	Usable Logic Gates*
CX3041	160	178	24K	6	13K	40K	22K-32K
CX3061	208	208	64K	8	20K	60K	33K-48K
CX3141	304	304	96K	12	45K	140K	77K-112K
CX3301	424	432	144K	18	100K	300K	165K-240K
CX3551	592	608	416K	52	185K	550K	303K-440K

CX3002 Family - High Volume Production

Base Array	I/Os	Pads	Memory Bits	No. of Configur-ations	Modules/ Logic Cells	Max Logic Gates	Usable Logic Gates*
CX3042	100	108	8K	2	14K	40K	22K-32K
CX3072	128	168	16K	4	24K	70K	39K-56K
CX3122	160	224	24K	6	40K	120K	66K-96K
CX3182	208	280	64K	8	60K	180K	99K-144K
CX3422	304	408	96K	12	140K	420K	231K-336K
CX3902	424	576	144K	18	300K	900K	495K-720K
CX31502	592	808	416K	52	550K	1.5M	825K-1.2M

* Actual array utilization is dependent upon characteristics of the design netlist. Utilization increases accordingly with advanced process and software tools.

Operating Conditions

	Characteristic	Condition	Best	Nominal	Worst	Unit
Vcc	3.3 V Supply Voltage	All	3.6	3.3	3.0	V
Vcc	5 V Supply Voltage	Commercial	5.25	5.0	4.75	V
Ta	Ambient Temp Range	Commercial	0	25	70	°C
		Industrial	-40	25	85	°C
		Military	-55	25	125	°C

DC Characteristics

	Characteristic	Condition	Value	Unit
Vol	Output Voltage Low	CMOS - Compatible	0.3 Vcc	V
Vol	Output Voltage Low	TTL - Compatible	0.45	V
Voh	Output Voltage High	CMOS - Compatible	0.7 Vcc	V
Voh	Output Voltage High	TTL - Compatible	2.45	V
Ioh	High Level Current		As specified on individual cells	A
Iol	Low Level Current		As specified on individual cells	A

Package Support

Type	Package Name	Pins
CPGA	Ceramic Pin Grid Array	100, 120,132,144, 180, 208, 224, 225, 256, 299†, 391†
CerQuad	Ceramic Quad Pack	100, 120, 128, 144, 160, 176, 208, 240, 256, 304
CQFP	Ceramic Quad Flat Pack	208, 304
PQFP*	Plastic Quad Flat Pack	100, 120, 128, 144, 160, 208, 240, 304
TQFP*	Thin Quad Flat Pack	100, 120, 128, 144, 160, 176, 208, 256
MQUAD*	Metal Quad Flat Pack	100, 128, 144, 160, 208, 240, 304
EQFP*	Enhanced Quad Flat Pack	144, 160, 176, 208
PBGA	Plastic Ball Grid Array (cavity up)	225, 256, 272, 352, 388, 420, 456, 493
CDEBGA*	Cavity Down Enhanced Ball Grid Array	256, 352, 420, 432
EBGA*	Enhanced Ball Grid Array (cavity down)	256, 352,420,432

† Cavity down

* Consult factory for prototype package availability

Chip Express®

The ASIC Time-to-Market Solution®

Chip Express Corporation
2323 Owen Street, Santa Clara, California 95054
Tel: (408) 988-2445, Fax: (408) 988-2449
E-mail: moreinfo@chipx.com

www.chipexpress.com