Numerically Controlled Oscillator

Data Sheet **July, 1999, ver. 1**

Target Applications:

Communications
Digital Signal Processing

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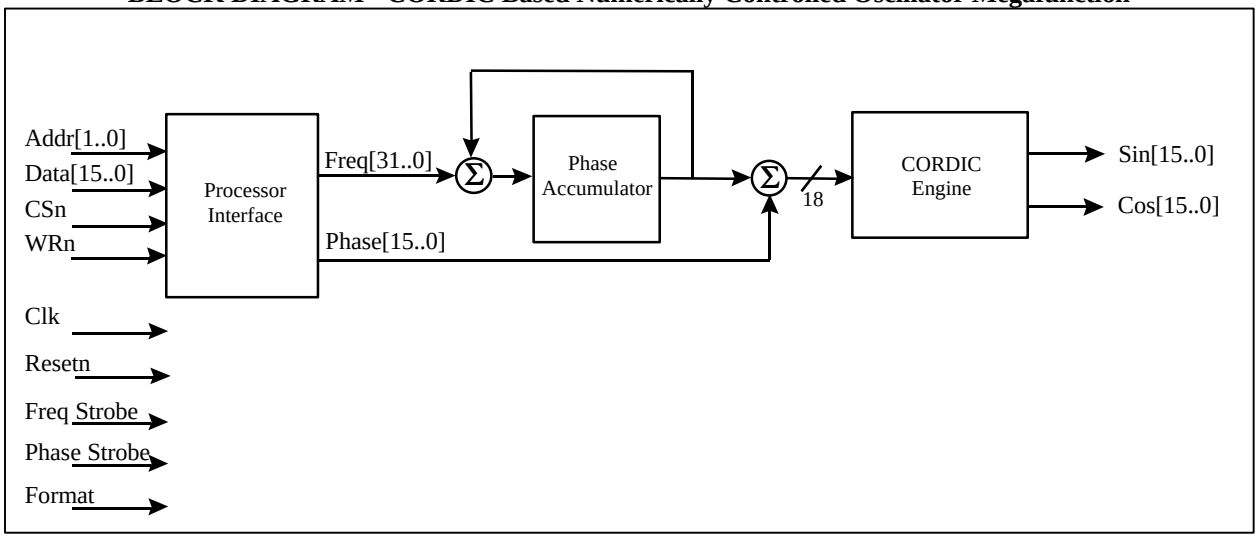
Features

- CORDIC Algorithm for accurate Sine/Cosine Generation
- 16-bit Quadrature Output
- 32-bit Frequency Tuning Register
- 16-bit Phase Offset Register
- Fully Pipelined for maximum speed
- Worst Case Spurs < -90dBc
- Includes 16-bit Microprocessor Interface

General Description

The CORDIC based Numerically Controlled Oscillator (NCO) from Nova Engineering produces digital sine and cosine waveforms at a programmable periodic rate. The 32-bit Frequency Tune Register enables the sine and cosine outputs to be tuned over a wide range of frequencies with a high degree of resolution. The sine and cosine values are calculated by a CORDIC engine to minimize spurious frequency components. A Phase Offset Register enables phase offsets of the sine and cosine outputs. The sine and cosine data values can be output in either two's complement or offset binary format.

BLOCK DIAGRAM - CORDIC Based Numerically Controlled Oscillator Megafunction



The table below indicates the logic usage for the CORDIC Based NCO Megafunction.

Device	Speed Grade	Logic Cells	% LC's Used	EABs	%EAB's Used	Fmax
EPF10K50V	-1	1800	60%	0	0	54MHz
EPF10K100A	-1	1800	35%	0	0	64MHz
EPF10K100E	-1	1800	35%	0	0	81MHz

1.0 Functional Description

The heart of the NCO is the CORDIC algorithm. The algorithm operates on the angle argument (x) output by the phase accumulator and the phase offset summer. The CORDIC algorithm works by rotating the coordinate system through constant angles until the angle is reduced to near zero.

The frequency of the NCO clock, Fclk, is generally fixed. Therefore, the frequency, Fout of the sine and cosine waves produced by the NCO is given by;

$$Fout = Fclk * Freq[31..0] / 2^{32}.$$

where; Freq is the input Frequency Tune Word in twos complement format.

The width of the phase accumulator, and the NCO clock, combine to determine the minimum frequency of the NCO. The lowest frequency occurs when the Frequency Tune Word is set to 1. Mathematically, the tune frequency, $Freq[31..0]/ 2^{32}$ represents a fraction. This fraction multiplies Fclk to determine the output frequency. The smallest fraction, and therefore the frequency resolution is

$$\text{Frequency Resolution} = Fclk / 2^{32} .$$

For Fclk = 50MHz, the frequency tuning resolution is approximately 0.012 Hz.

The maximum output frequency is theoretically limited by the Nyquist sampling theory to Fclk/2. Practical applications typically utilize fractions smaller than ½ to simplify realization of the reconstruction filter. In general, when the fraction $Freq[31..0]/ 2^{32}$ is large, the number of points output per cycle of the sinusoid is small, and filtering becomes more difficult to realize. Conversely, when the fraction is small, the number of output points per cycle is large, and filtering becomes much easier to realize.

The Frequency Tune Word, Freq[31..0], and the Phase Offset Word, Phase[15..0], are double buffered to internally synchronize frequency and phase changes to the NCO clock. Sixteen bits of the tune word are written to the tune register contained within the microprocessor interface. This is accomplished by a write to the upper and lower words of the 32-bit frequency tune register. Assertion of the external Frequency Strobe signal, causes the contents of the frequency tune register to load into the phase accumulator on the next rising edge of the NCO clock. The Frequency Strobe signal must be de-asserted before a new tune word is written to the frequency tune register. The complete 16-bit Phase Offset word is written in one write cycle. Assertion of the Phase Strobe signal, transfers the phase offset value contained in the Phase Offset Register, to the phase accumulator/phase offset summer.

The latency from Frequency Strobe sampled high to the corresponding sine/cosine output, is equal to 20 clock cycles. The latency from Phase Offset Strobe sampled high to the resulting output phase offset is equal to 19 clock cycles.

2.0 Interface Descriptions

The interfaces to the CORDIC based NCO are described in Table 2.0-1. Signal types are defined as Input (I), Output (O), and Bi-directional (B). Unused inputs must be pulled to VDD or Ground. Signal names ending in the lower case letter "n" are active low.

TABLE 2.0-1 INTERFACE DESCRIPTIONS

SIGNAL	TYPE	DESCRIPTION
ADDR[1..0]	I	**Address Bus**. Host processor address bus.
DATA[15..0]	I	**Data Bus**. Host processor data bus.
CSn	I	**Chip Select**. Enables host processor writes to this device.
WRn	I	**Write**. Host processor write command.
CLK	I	**Clock In**. Master clock for processing logic.
RESETn	I	**Reset**. Master asynchronous reset for processing logic.
FREQ STROBE	I	**Frequency Strobe**. Transfers tune word into phase accumulator. (active high)
PHASE STROBE	I	**Phase Offset Strobe**. Transfers phase offset word to CORDIC engine. (active high)
FORMAT	I	**Format**. Controls output data format. (0=two's complement / 1= offset binary)
SIN	O	**Data Clock**. Receive baseband data clock.
COS	O	**Data Output**. Processed receive data. Synchronous to data clock.

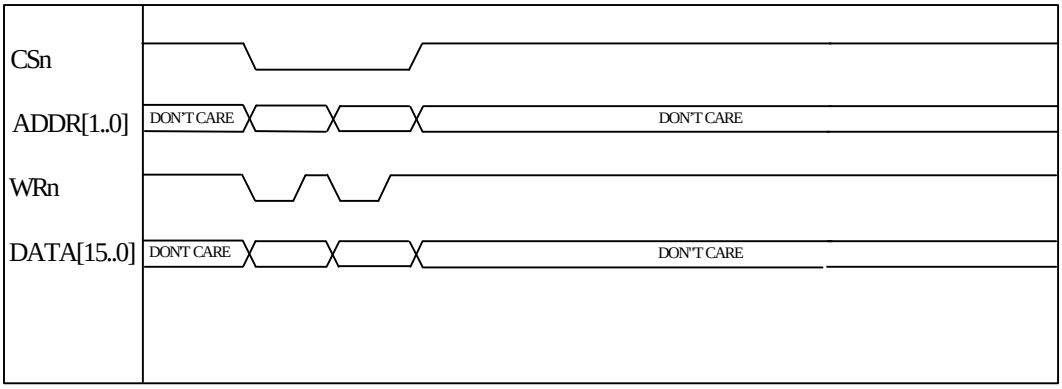
2.1 Processor Interface

The parallel processor interface permits the host processor to write control information to the NCO. The NCO provides a standard 16-bit interface to most microprocessors or DSP's, however the processor interface can be easily customized to accommodate any processor, since the PLD is software programmable.

2.1.1 Bus Interface

The standard bus interface includes a 16-bit, input data bus, an active low chip select, write control line, and an address bus. The NCO data bus is tri-stated when CSn=1 and the device is not selected. During a write cycle, data from the host processor data bus is latched into the register indicated by the address bus. Figure 2.1.1-1 illustrates a typical write bus cycle.

FIGURE 2.1.1-1 Typical Bus Cycles



2.1.2 Frequency Tune Register

The NCO provides a Frequency Tune Register to hold frequency tune data transferred form the host processor. The register allows the host processor to transfer the data in 16-bit wide words. The Frequency Strobe signal is used to enable the transfer of the Frequency Tune Register contents into the phase accumulator.

The twos complement format of the Frequency Tune Word supports both positive and negative frequencies. The output frequency of the NCO is determined by the NCO clock frequency and the Frequency Tune Word in accordance with the following equation:

$$Fout = Fclk * Freq[31..0] / 2^{32} \quad ; Fout \text{ in Hz.}$$

1.1.3 Phase Offset Register

The NCO provides a Phase Offset Register to hold offset data transferred form the host processor. The register allows the host processor to transfer the data in a single 16-bit wide word. The Phase Strobe signal is used to enable the transfer of the Phase Offset Register contents into the phase accumulator/offset summer. The 16-bit Phase Offset Word, input to the NCO, is left justified to create 32-bits, by zero filling the lower 16-bits.

The twos complement format of the Phase Offset Word supports both positive and negative phase offsets. The phase offset of the NCO outputs are determined by the Phase Offset Word in accordance with the following equation:

$$Phase[15..0] = Phase\ Offset / 180 * 2^{31} \quad ; Phase\ Offset \text{ in degrees.}$$

1.1.4 Address Decode Logic

The NCO contains the address decode logic necessary to decode four 16-bit internal registers. The address decode logic can be easily modified to accommodate a variety of addressing schemes. For example, the address decoder can be configured to decode more or less than the standard four registers. It can also be configured to support registers of different widths. In fact, the processor interface can include custom address decode logic and other miscellaneous glue logic, required for the host processor, further increasing system integration and flexibility.

TABLE 2.1.3-1 Address Decoding

Address	CSn	WRn	Function
00	0	Rising Edge	Writes the Frequency Tune Register[15..0]
01	0	Rising Edge	Writes the Frequency Tune Register[31..16]
10	0	Rising Edge	Writes the Phase Offset Register[15..0]
11	0	Rising Edge	Reserved

1.2 Control Signals

The CORDIC NCO provides four control signals that permit user control without using the microprocessor interface. These control lines allow the user to select the output number format, synchronize tuning and phase modulation, as well as initialize the internal logic.

1.2.1 Resetn

The CORDIC NCO provides an asynchronous reset signal that is active low. When this line is low all logic, including the microprocessor registers, are cleared.

1.2.2 Format

The Format control signal determines the numeric format of the output data. When the Format control line is held low, the NCO outputs data in the two's complement format. When the Format line is held high, NCO data is output in the binary offset format. Input data is ALWAYS two's complement format. The table below illustrates the relationship between these formats and a typical DAC Full Scale.

DAC Level	Two's Complement Format	Offset Binary Format
+FS -1 LSB	32767 (7FFFh)	65535 (FFFFh)
+FS/2	16384 (4000h)	49152 (C000h)
+1 LSB	1 (0001h)	32769 (8001h)
0	0 (0000h)	32768 (8000h)
-1 LSB	65535 (FFFFh)	32767 (7FFFh)
-FS/2	49152 (C000h)	16384 (4000h)
-FS	32768 (8000h)	0 (0000h)

To convert Offset Binary outputs to fractional representation use the following equation:

Fractional Representation = (Output value -32768) / 32767.

To convert Two's Complement output to fractional representation use the following equation:

$$\text{Fractional Representation} = \begin{cases} (\text{Output Value} - 65536) / 32767 & ; \text{when (Output Value} > 32767) \\ (\text{Output Value} / 32767) & \text{otherwise} \end{cases}$$

1.2.3 Frequency Strobe

The Frequency Strobe control line transfers the contents of the Frequency Tune Register to the phase accumulator, on the first rising edge of the clock, after the control line is asserted.

1.2.4 Phase Strobe

The Phase Strobe control line transfers the contents of the Phase Offset Register to the accumulator/offset summer, on the first rising edge of the clock, after the control line is asserted.

3.0 Spectral Analysis

The CORDIC based NCO provides excellent spectral purity. The superior spurious performance is due to the use of 18-bits of phase information by the CORDIC routine. In a typical Look-Up-Table based NCO this would require nearly 500Kbytes of equivalent ROM storage. The requirement for ROM space doubles if simultaneous sin and cosine outputs are desired using the Look-Up-Table approach. The CORDIC based NCO automatically provides both sine and cosine outputs simultaneously.

Figure 3.0-1 shows a spectral analysis of the sine wave output for Fs/4 + 500kHz. This particular frequency represents the worst case, close-in, ¼ cross-over spurs. Figure 3.0-2 shows the spectral analysis of the sine wave output for Fs/4 + 1kHz. This frequency displays more bandwidth and consequently a larger number of spurs.

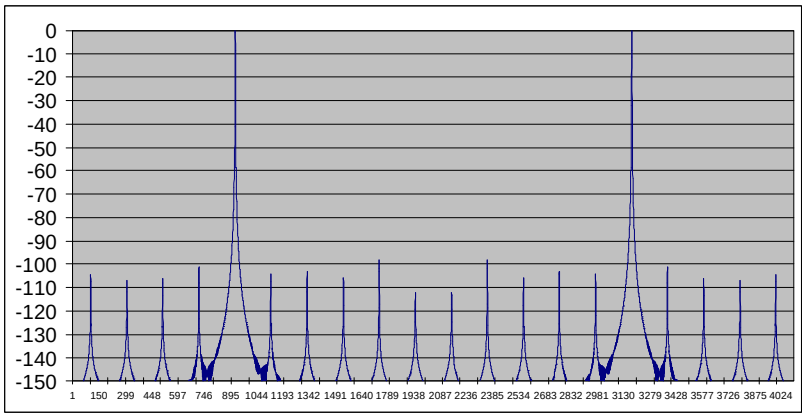


Figure 3.0-1 Spectral Analysis of NCO Output (Fs/4 + 500kHz)

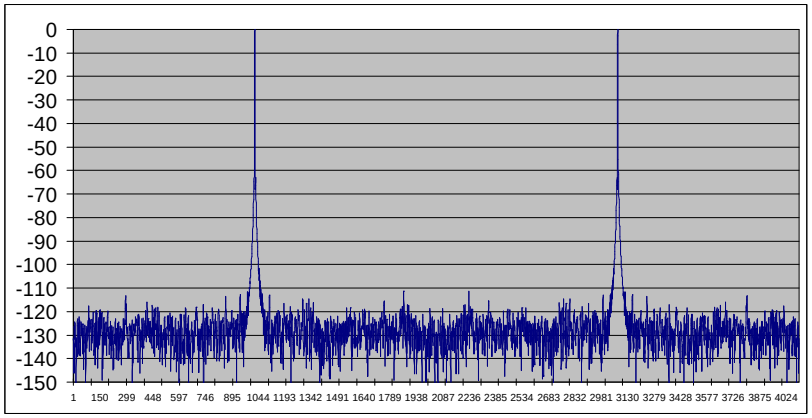


Figure 3.0-2 Spectral Analysis of NCO Output (Fs/4 + 1kHz)