



COMPARATOR

- Programmable Hysteresis and Response Time
- Configurable as Wake-up or Reset Source
- Low Current (0.4uA)

ON-CHIP DEBUG

- On-Chip Debug Circuitry Facilitates Full Speed, Non-Intrusive In-System Debug (No Emulator Required!)
- Provides Breakpoints, Single Stepping, Watchpoints
- Inspect/Modify Memory, Registers, and Stack
- Superior Performance to Emulation Systems Using ICE-Chips, Target Pods, and Sockets
- Low Cost, **Complete** Development Kit

SUPPLY VOLTAGE2.7V to 3.6V

- Typical Operating Current: 5.8mA @ 25MHz
11uA @ 32kHz
- Typical Stop Mode Current: <0.1uA

Temperature Range: -40°C to +85°C

HIGH SPEED 8051 μ C Core

- Pipe-lined Instruction Architecture; Executes 70% of Instructions in 1 or 2 System Clocks
- Up to 25MIPS Throughput with 25MHz Clock
- Expanded Interrupt Handler

MEMORY

- 256 Bytes Internal Data RAM
- 8k Bytes FLASH; In-System Programmable in 512 byte Sectors

DIGITAL PERIPHERALS

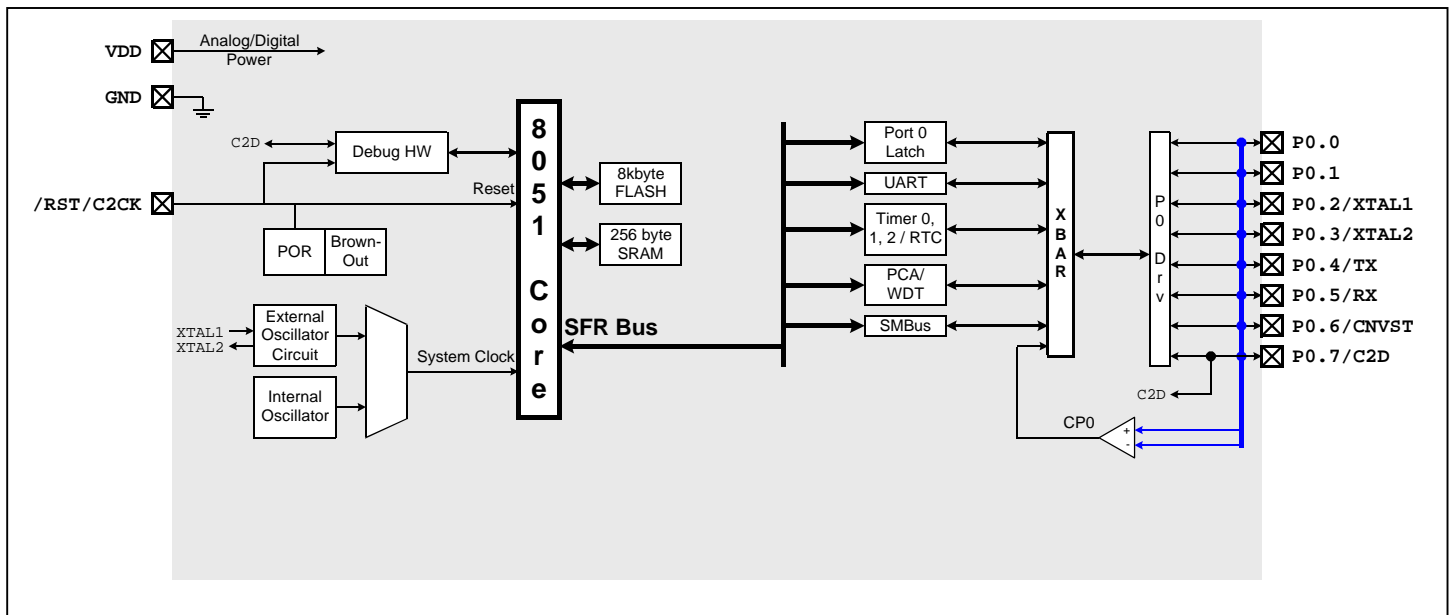
- 8 Port I/O; All 5V tolerant with High Sink Current
- Enhanced Hardware UART and SMBus™ Serial Ports
- Three General Purpose 16-Bit Counter/Timers
- 16-bit Programmable Counter Array with Three Capture/Compare Modules, WDT
- Real Time Clock Mode using PCA or Timer and External Clock Source

CLOCK SOURCES

- Internal Oscillator: 20MHz Nominal
- External Oscillator: Crystal, RC, C, or Clock (1 or 2 Pin Modes)
- Can Switch Between Clock Sources on-the-fly; Useful in Power Saving Modes

11-Pin Micro Lead Package

- 3 x 3mm PCB Footprint; Actual MLP Size 
- SMBus is a trademark of Intel Corp.





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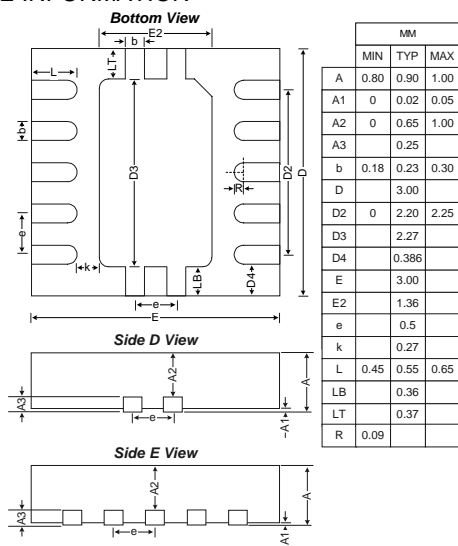
8KB Flash, 256 RAM, 11-Pin MCU

PRELIMINARY

SELECTED ELECTRICAL SPECIFICATIONS $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 2.7\text{V}$ unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL CHARACTERISTICS					
Supply Voltage		2.7		3.6	V
Supply Current with CPU active	Clock=25MHz		5.8		mA
	Clock=1MHz		0.34		mA
	Clock=32kHz; VDD Monitor Disabled		11		μA
Supply Current (shutdown)	Oscillator off; VDD Monitor Enabled		10		μA
	Oscillator off; VDD Monitor Disabled		<0.1		μA
CPU & DIGITAL I/O PORTS					
Clock Frequency Range		DC		25	MHz
Port Output High Voltage	$I_{OH} = -3\text{mA}$, Port I/O push-pull	$V_{DD} - 0.7$			V
Port Output Low Voltage	$I_{OL} = 8.5\text{mA}$			0.6	V
Input High Voltage		$0.7 \times V_{DD}$			V
Input Low Voltage				$0.3 \times V_{DD}$	V
INTERNAL OSCILLATOR					
Frequency		15.0	20.0	25.0	MHz
COMPARATOR					
Response Time Mode0	$(CP+) - (CP-) = 100\text{mV}$		0.1		μs
Current Consumption Mode0			7.6		μA
Response Time Mode1	$(CP+) - (CP-) = 100\text{mV}$		0.18		μs
Current Consumption Mode1			3.2		μA
Response Time Mode2	$(CP+) - (CP-) = 100\text{mV}$		0.32		μs
Current Consumption Mode2			1.3		μA
Response Time Mode3	$(CP+) - (CP-) = 100\text{mV}$		1		μs
Current Consumption Mode3			0.4		μA

PACKAGE INFORMATION



C8051F300DK DEVELOPMENT KIT

