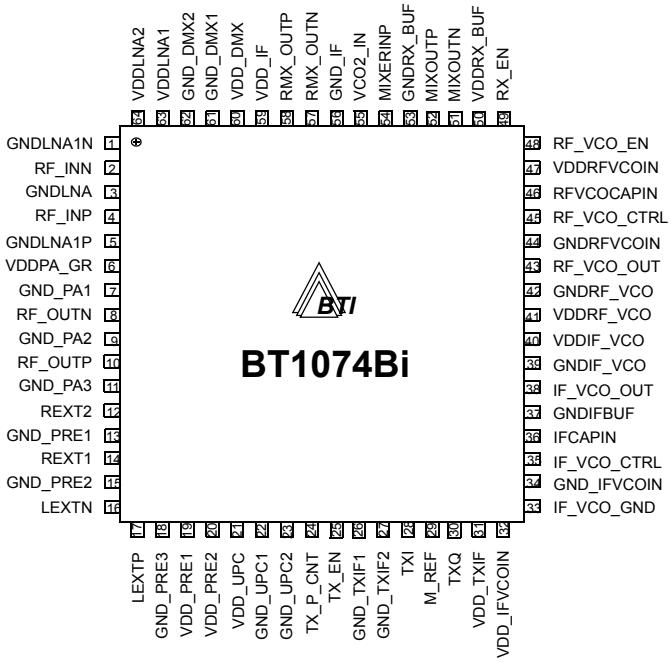
SINGLE CHIP 850-950MHz RF TRANSCEIVER

Features

- Complete single chip RF transceiver
- Two on-chip local oscillators
- I/Q or FM* input interface
- Single power supply 2.7 - 3.6 V
- Low power consumption BiCMOS technology
- On-chip LNA and RF Mixer
- RF Power selectivity (-4dBm or +17dBm)
- Wide operating temp range (-40°C to +85°C)



Applications

- 902-928 MHz ISM Band
- 868-870MHz Band (Europe)
- Direct Sequence Spread Spectrum (DSS)
- Frequency Hopping Spread Spectrum
- Wireless LAN
- Wireless Communication Products

Description

The BT1074Bi is a BiCMOS monolithic integrated RF transceiver. In addition to the input I/Q interface, the IC contains all of the required components to implement a complete RF-IF transceiver. This includes two on-chip local oscillators, a low noise amplifier with an overall noise figure of less than 5dB over temperature and power supply variations, two highly linear down-conversion mixers, an IF amplifier, an upconversion mixer and an on-chip power amplifier capable of delivering -4dBm to +17dBm. The unit operates with a power supply voltage range of 2.7 - 3.6 volts.

* *See Single-ended RFM input application example on page 15.*

TRFIC® RFICs for 850 - 2400MHz

Ordering Information

BT1074Bi 850-950MHz RF Transceiver

BTI, 13825 Cerritos Corporate Dr., Cerritos CA. 90703, U.S.A.
Tel (562) 407-0500 Fax (562) 407-0510 sales@betheltronix.com www.betheltronix.com

Specifications

Parameters	Min.	Typ.	Max.	Units
Overall				
Power supply	2.7	3.0	3.6	V
Operating Frequency ranges	890	915	940	MHz
	860		875	MHz
Receiver				
Gain	28	35	44	dB
Noise Figure	3.6	4	5	dB
Input IP3	-11	-12	-13	dBm
Current consumption (w/ RF VCO)	-	60	-	mA
Transmitter				
Gain	-	17	-	dB
TX current consumption @	-	89*	-	mA
High power mode (with RF & IF VCOs)				
*with RF PA @ +15 dBm output				
IFVCO current consumption	-	27	-	mA
RFVCO current consumption	-	32	-	mA
Receiver Section				
LNA + RF Downconversion Mixer				
Gain	16	20	22	dB
Input IP3	-13	-12	-11	dBm
Input 1dB compression point	-22	-21	-20	dBm
Noise figure (LNA only)	2.4	2.8	3.3	dB
S11	-44	-	-22	dB
Input impedance[1]	-	50	-	Ω
Output Impedance	-	300	-	Ω
Image Rejection (at typical center freq.):				
915MHz	27	29	31	dB
881.49MHz	26	28	30	dB
IF Downconversion Mixer & IF Amp				
Gain	12	15	20	dB
Input IP3	-10	-10	-9	dBm
Input 1dB compression point	-20	-20	-19	dBm
Noise figure	-	-	-	
Input Impedance	-	300	-	Ω
Output Impedance	-	330	-	Ω
Transmitter Section				
I&Q Modulator & Filter				
Input impedance	-	>20	-	kΩ
I/Q input frequency	-	<4	-	MHz
I/Q input swing	-	0.5	-	Vp-p
I/Q input DC level	-	VDD/2	-	V
M_REF DC level	-	VDD/2	-	V

Parameters	Min.	Typ.	Max.	Units
RF Upconversion Mixer				
Conversion gain (internal)	-	0	-	dB
Input IP3	-	-10	-	dBm
Input 1dB compression point	-	-20	-	dBm
Power Amplifier*				
Output power into 50Ω load, high power mode (TX_P_CNT=0V)	+13	+15	+17	dBm
Output power into 50Ω load, low power mode (TX_P_CNT=VDD)	-	-4	-	dBm
Voltage Gain (internal)	-	25	-	dB
Output impedance (after combiner)	-	50	-	Ω
Output 1dB compression point	-	7	-	dBm
Output spurious suppression	-	-40	-30	dBm
RF VCO Section*				
Frequency range (at output to PLL)	780	805	830	MHz
VCO phase noise at 100KHz offset (closed-loop)	-	-100	-	dBc/Hz
VCO phase noise at 1MHz offset	-	-118	-	dBc/Hz
VCO output level (50Ω)	-14	-12	-6	dBm
IF VCO Section*				
Frequency range (at output to PLL)	205	220	235	MHz
VCO phase noise at 100KHz offset (closed-loop)	-	-112	-	dBc/Hz
VCO phase noise at 1MHz offset	-	-120	-	dBc/Hz
VCO output level	-14	-8	-2	dBm

** The values in these sections refer to the 902-928MHz application. To use the BT1074B in the 868-870MHz band, only the RF VCO, IF VCO, power combiner and LNA RF matching component values need to be changed.*

Absolute Maximum Ratings

Parameters	Value	Unit
Supply Voltage	7	V
Power Control Voltage	V_{DD}+0.5	V
Storage Temperature	+150	^oC

Pin Table

Pin	Parameter	I/O	Description
Power and Ground Pins			
63/64	VDDLNA1-2	-	Power supply to LNA
60	VDD_DMX	-	Power supply to downconverters
59	VDD_IF	-	Power supply to RX differential-to-single buffers
32	VDD_IFVCOIN	-	Power supply to IF VCO first stage

Pin	Parameter	I/O	Description
21	VDD_UPC	-	Power supply to TX upconverters
6	VDDPA_GR	-	Power supply to guard ring
19/20	VDD_PRE1-2	-	Power supply to pre-amplifier
31	VDD_TXIF	-	Power supply to transmitter
40	VDDIF_VCO	-	Power supply to IF VCO
41	VDDRF_VCO	-	Power supply to RF VCO
47	VDDRFVCOIN	-	Power supply to RF VCO input stage
50	VDDRX_BUF	-	Power supply to receiver IF buffer
3	GNDLNA	-	Ground to LNA
61/62	GND_DMX1-2	-	Ground to downconverters
56	GND_IF	-	Ground to RX differential-to-single buffers
34	GND_IFVCOIN	-	Ground to IF VCO first stage
22/23	GND_UPC1-2	-	Ground to TX upconverters
13/15/18	GND_PRE1-3	-	Ground to pre-amplifier
7/9/11	GND_PA1-3	-	Ground to power amplifier
26/27	GND_TXIF1-2	-	Ground to transmitter
5	GNDLNA1P	-	Ground to RX LNA differential first stage
1	GNDLNA1N	-	Ground to RX LNA differential first stage
37	GNDIFBUF	-	Ground to IF VCO buffer
39	GNDIF_VCO	-	Ground to IF VCO
42	GNDRF_VCO	-	Ground to RF VCO
44	GNDRFVCOIN	-	Ground to RF VCO input stage
53	GNDRX_BUF	-	Ground to receiver IF buffer
33	IF_VCO_GND	-	Ground to IF VCO buffer
Local Oscillator Pins			
38	IF_VCO_OUT	O	IF VCO output
36	IFCAPIN	I	IF VCO feedback capacitors input
35	IF_VCO_CTRL	I	IF VCO control input
43	RF_VCO_OUT	O	RF VCO output
45	RF_VCO_CTRL	I	RF VCO control input
46	RFVCOCAPIN	I	RF VCO resistor bias input
Transmitter Pins			
8	RF_OUTN	O	Power amplifier output
10	RF_OUTP	O	Power amplifier output
24	TX_P_CNT	I	Transmission output power control: Hi - low power mode Low - high power mode
12	REXT2	I	Bias for power amplifier
14	REXT1	I	Bias for power amplifier

Pin	Parameter	I/O	Description
16	LEXTN	O	Output to external inductors
17	LEXTP	O	Output to external inductors
28	TXI	I	Baseband quadrature input to the transmitter
29	M_REF	I	I/Q input DC reference
30	TXQ	I	Baseband in-phase input to the transmitter
Receiver Pins			
4	RF_INP	I	RF Differential Input to the receiver
2	RF_INN	I	RF Differential Input to the receiver
55	VCO2_IN	I	Second Mixer's input
54	MIXERINP	I	RF input to the second mixer
51	MIXOUTN	O	Differential output of second downconverter mixer
52	MIXOUTP	O	Differential output of second downconverter mixer
58	RMX_OUTP	O	Differential output of downconverter mixer
57	RMX_OUTN	O	Differential output of downconverter mixer
Power Down Pins			
25	TX_EN	I	Transmitter power down control
49	RX_EN	I	Receiver power down control
48	RF_VCO_EN	I	RF VCO power down control

Detailed Pin Description:

RECEIVER

RF_INP and RF_INN (Pin 4 and Pin 2)
RF Differential Inputs
RF_INP and RF_INN are the differential inputs of the LNA. An AC coupling capacitor of 100pF is required. RF differential inputs are generated by an external phase-splitter circuit, but for a single RF input, the LNA can be biased, as shown in the **Application Circuit**. For optimum performance, the component lead length of the external phase-splitter circuit and PCB traces to the LNA input pins should be minimized. Also, the ground plane must surround the phase -splitter circuit to prevent noise coupling from other circuits. The frequency range is from 890MHz to 940MHz.

RMX_OUTP and RMX_OUTN (Pin 58 and Pin 57)
First IF Differential Outputs
These are the differential outputs of the internal IF buffers. With the external IF combiner circuit as shown in the **Application Circuit,** the differential outputs become a single-ended output to drive a 110.592MHz Bandpass SAW filter. These internal IF buffers have open-drain outputs to drive an input impedance of a 300Ω BPF through the external combiner circuit.

MIXERINP (Pin 54)
Second IF Amplifier Input
The output of a 110.592MHz BPF SAW filter is connected to this pin for the second stage downconversion. No AC coupling is required.

MIXOUTP and MIXOUTN (Pin 52 and Pin 51)
Second IF Differential Outputs
These are the second IF Amp differential outputs. The gain of the IF Amp can be controlled by connecting MIXOUTP through a resistor to ground. A 470Ω resistor to ground gives a 0dB gain. The other Amp output, MIXOUTN, is fed to a 10.7MHz BPF through an AC coupling (0.1uF) capacitor.

VCO2_IN (Pin 55)
External Clock Input
A clock of 99.892MHz is fed to this pin to downconvert the first IF at 110.592MHz to 10.7MHz. No AC coupling is required.

VDDLNA1, VDDLNA2 (Pin 63 and Pin 64)
LNA power
VDDLNA supplies power to the first and second stage of the LNA. Since the LNA input signal level is small and high frequency, the VDDLNA should be decoupled very close to the chip (for example, within 0.25 inches of the package).

GNDLNA1P, GNDLNA1N and GNDLNA (Pin 5, Pin 1 and Pin 3)
LNA Ground
GNDLNA1P and GNDLNA1N pins are the ground for the first stage of the LNA and GNDLNA is the ground for the second stage of the LNA. GNDLNA1P and GNDLNA1N are internally separated. For stability and optimum performance, the GNDLNA1P and GNDLNA1N should be physically short.

VDD_DMX (Pin 60)
Downconverter Power
VDD_DMX supplies power to the downconversion mixers.

GND_DMX1, GND_DMX2 (Pin 61 and Pin 62)
Downconverter Ground
GND_DMX is the ground for the downconversion mixers. This ground connection is recommended to be shorted via holes to the ground plane below.

VDD_IF and VDDRX_BUF (Pin 59 and Pin 50)
IF Buffers and Second Downconversion Mixers Power
Both power supplies require 0.1uF bypass capacitors to ground.

GND_IF and GNDRX_BUF (Pin 56 and Pin 53)
IF Buffers and Second Down-Conversion Mixers Ground
GND_IF is the ground for the internal IF buffers, and GNDRX_BUF is the ground for the second downconversion mixers and IF amplifiers.

TRANSMITTER

RF_OUTN and RF_OUTP (Pin 8 and Pin 10)
Power Amplifier Outputs
These are the differential outputs of the power amplifier which requires a combining network as shown in the **Application Circuit**. The combiner converts the differential signals to a single-ended signal and provides a matching impedance to 50Ω as well. DC bias to VDD is required since these are open-collector outputs, and AC coupling is needed after the combiner as shown.

LEXTN and LEXTP (Pin 16 and Pin 17)
Preamplifier Amplifier Outputs
These are the differential outputs of the preamplifier, which are open-collector types. Two inductors to the VDD are required for tuning the preamplifier to the desired frequency band. Recommended values for 900MHz are shown in the **Application Circuit**. Since these are also inputs to the power amplifier, the inductors should be close to the pins and isolated from the power amplifier output to avoid output feedback to these two pins, which may cause instability for the power amplifier.

REXT1 and REXT2 (Pin 14 and Pin 12)
Preamplifier/Power Amplifier Bias/Gain Adjust
Rext1 is the biasing resistor for the preamplifier, and REXT2 is the biasing resistor for the power amplifier. For an output power of +15dBm, recommended values are 1kΩ for REXT1 and 2.8kΩ for REXT2. Increasing REXT1 and lowering REXT2 will lower output power, and vice versa.

TXI, M_REF and TXQ (Pin 28, Pin 29 and Pin 30)
Baseband Data Inputs
These are the inputs which interface with the data signals from the digital signal processor (DSP) or microprocessor (μP). TXI and TXQ are inphase (I) and quadrature (Q) signals, respectively. M_REF is the DC signal coming from the DSP/μP. All of these pins require a DC level of VDD/2, and a voltage swing of 500mVp-p is required for TXI and TXQ. The **Application Circuit** shows a technique to interface with 1Vp-p I and Q signals with a 6dB voltage attenuator with DC reference to M_REF pin. A low pass filter may also be required to reject sampling noise from the DSP/μP. For DSS applications, the base band data input signal can be modulated at the IFVCO tank circuit using a Gaussian filter, prior to the PLL frequency synthesizer. For that, the M_REF pin has to be biased to half of +VDD supply and both the TXQ & TXI input have to connect to the M_REF pin through a resistor in order to adjust the TX output gain.

VDDPA_GR (Pin 6)
Power Supply for Guard Ring of Power Amplifier
This power supply pin is only for the output stage of power amplifier. It should be decoupled right at the pin before sharing with other power supplies.

VDD_PRE1, VDD_PRE2 (Pin 19 and Pin 20)
Power Supply for Preamplifier
These are the power supply pins dedicated to the preamplifier. Decoupling should be done right at these pins to a ground plane, if possible.

VDD_UPC (Pin 21)
Power Supply for RF Upconversion Mixers
This is a dedicated power supply pin for the RF upconversion mixers. Decoupling should be done right at this pin to a ground plane, if possible.

VDD_TXIF (Pin 31)
Power Supply for Input Buffers and IF Upconversion Mixers
The input buffers and IF upconversion mixers share this power supply on-chip. Besides the usual high frequency decoupling, it should be decoupled for low frequency, up to 10MHz.

These are the dedicated ground pins that can share the same ground as long as a good ground plane is available:

GND_PA1, GND_PA2, GND_PA3 (Pin 7, Pin 9 and Pin 11)
Ground Pins for the Power Amplifier

GND_PRE1, GND_PRE2, GND_PRE3 (Pin 13, Pin 15 and Pin 18)
Ground Pins for the Preamplifier

GND_UPC1, GND_UPC2 (Pin 22 and Pin 23)
Ground Pins for the RF Upconversion Mixers

GND_TXIF1, GND_TXIF2 (Pin 26 and Pin 27)
Ground Pin for the Input Buffers and IF Upconversion Mixers

RFVCO

RF_VCO_CTRL (Pin 45)
RFVCO Input Control
An external tank circuit is connected to the RFVCO Input Control pin (see **Application Circuit**). The tank circuit generates the overall oscillation frequency for the RFVCO and therefore must be optimized to avoid any interference from other components. The RF_VCO_CTRL pin and the external PLL completes the RF-PLL loop that generates a fixed oscillation frequency for the RFVCO.

RF_VCO_OUT (Pin 43)
RF_VCO Output
The RF_VCO_OUT pin is connected to the external PLL to complete the RF-PLL loop. The PLL applies a DC voltage to the input tank circuit based on the detected RF_VCO_OUT signal. This DC voltage produces the negative bias voltage required by the Varactor to generate the necessary capacitance for the tank circuit network.

VDDRFVCOIN and GNDRFVCOIN (Pin 47 and Pins 44)
RFVCO Input Stage Power Supply and Ground
VDDRFVCOIN is the power supply for the input stage of the RFVCO. For optimum performance, VDDRFVCOIN should be bypassed to GNDRFVCOIN using a low-inductance / high frequency coupling capacitor. The input stage of the RFVCO is very critical in generating the overall frequency of the RFVCO; therefore isolating these power supply pins will enhance the overall performance of the RFVCO.

VDDRF_VCO and GNDRF_VCO (Pin 41 and Pin 42)
RFVCO Power Supply and Ground
VDDRF_VCO and GNDRF_VCO provide the power supply source for the other stages of the RFVCO.

RFVCOCAPIN (Pin 46)
RFVCO Resistor Bias Input
This pin provides an off-chip resistor bias to the RF VCO.

IF VCO

IF_VCO_CTRL (Pin 35)
IF VCO Input
This pin is connected to the external tank circuit as the VCO input. Its frequency is tuned to 221.184MHz (according to the RF module application) and can vary up to 500MHz.

IFCAPIN (Pin 36)
VCO Feedback Capacitors Input
This pin provides an off-chip capacitive feedback loop to the VCO oscillator.

IF_VCO_OUT (Pin 38)
IF VCO Differential Outputs
The VCO's oscillation frequency can be controlled by connecting its output to a PLL as shown in the **Application Circuit**.

VDD_IFVCOIN (Pin 32)
VCO Input Power Supply
The IF VCO has two power supplies, VDD_IFVCOIN (Pin 32) and VDDIF_VCO (Pin 40). VDD_IFVCOIN is the first stage VCO power. A large capacitor of at least 100pF is recommended to connect this pin and ground for filtering out noise.

VDDIF_VCO (Pin 40)
VCO Buffer Power Supply
This pin provides power to the internal VCO buffer circuitry.

GND_IFVCOIN (Pin 34)
VCO Input Ground
This pin is the first stage VCO ground.

GNDIFBUF (Pin 37)
VCO Buffer Ground
This pin is ground for the internal VCO buffer circuitry.

IF_VCO_GND (Pin 33)
Ground to IF VCO Buffer
This pin is ground for the IF VCO buffer, which is used by the transmitter section during transmission.

GNDIF_VCO (Pin 39)
VCO Ground
This pin is ground for the internal VCO circuitry.

POWER SAVING/POWER DOWN PINS

The following pins are all CMOS digital interface.

TX_P_CNT (Pin 24)
Transmission Output Power Control
This pin controls the power amplifier output with two levels. A HIGH signal puts the power amplifier in low power mode with -4dBm output power. A LOW signal puts the power amplifier in high power mode with +17dBm output power. These power levels are based upon the resistor values shown for REXT1 & REXT2.

TX_EN (Pin 25)
Transmitter Power Down Control
This pin controls the power down function of the entire transmitter, including the power amplifier and preamplifier. A HIGH signal turns the circuit on while a LOW signal turns the circuit off.

RF_VCO_EN (Pin 48)
RF VCO Power Down Control
This pin controls the power-down function of the RF VCO, which is used by the transmitter and the receiver. A HIGH signal turns the circuit off while a LOW signal turns the circuit on.

RX_EN (Pin 49)
Receiver Power Down Control
This pin controls the power down function of the entire receiver. A HIGH signal turns the circuit off while a LOW signal turns the circuit on.

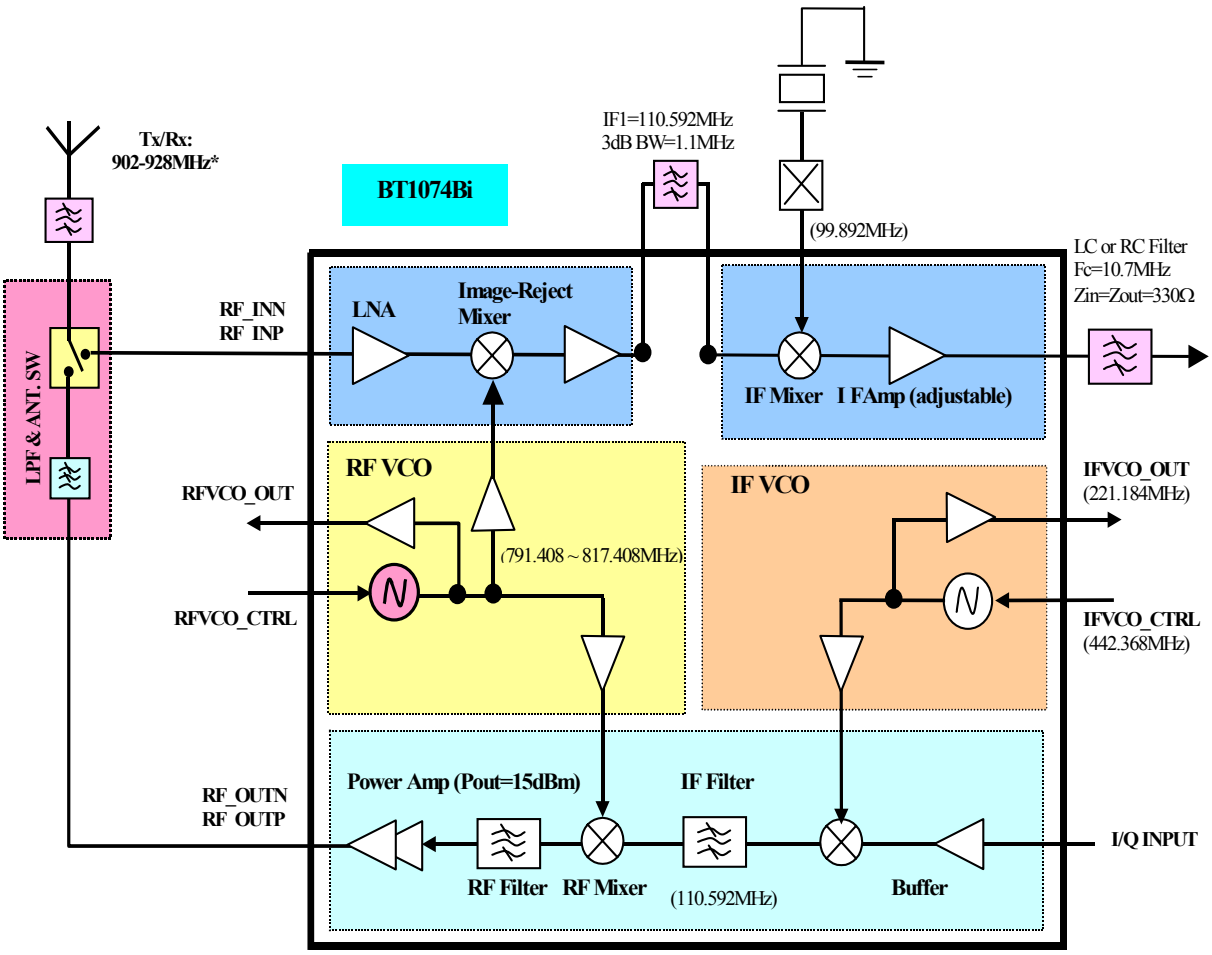
TYPICAL PERFORMANCE CHARACTERISTICS

The recommended TDD mode as well as power saving mode usage of all of these control pins are as follows:

Pins	Communication Mode		Power Save Mode*
	TX	RX	
TX_EN	HI	LO	LO
RX_EN	HI	LO	HI
RF_VCO_EN	LO	LO	HI
TX_P_CNT	LO	LO	HI

Note: Control level for minimum power consumption.

Block Diagram



*: ISM Band

TRFIC® RFICs for 850 - 2400MHz

RECEIVER:

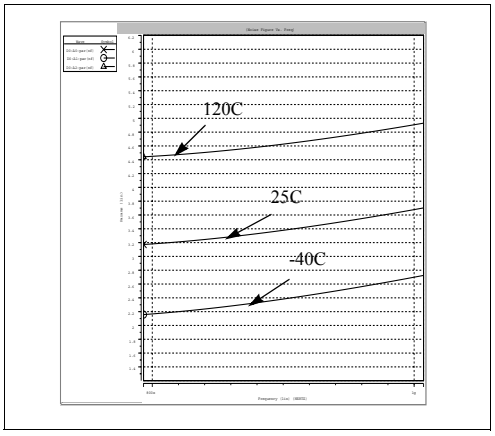


Figure 1. NF vs. Freq, varying temp.

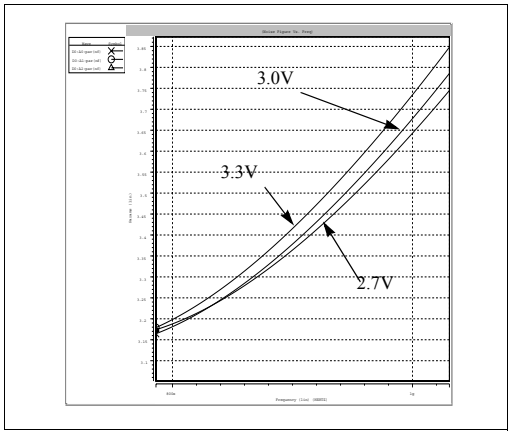


Figure 2. NF vs. Freq, varying Vdd

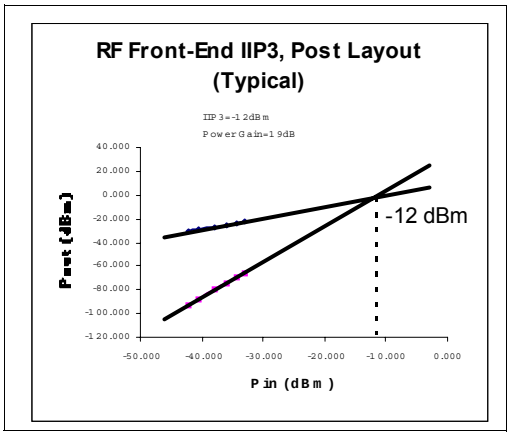


Figure 3. IP3 (LNA + RF Mixer)

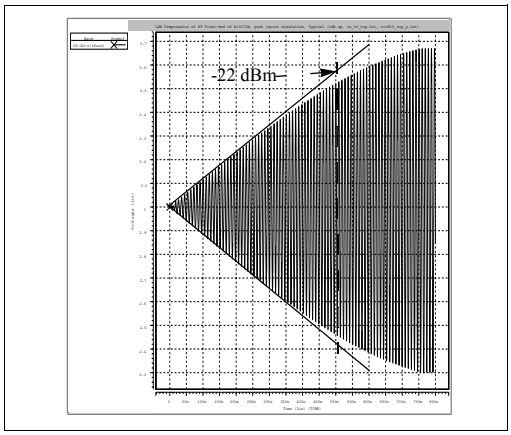


Figure 4. P1dB (LNA + RF Mixer)

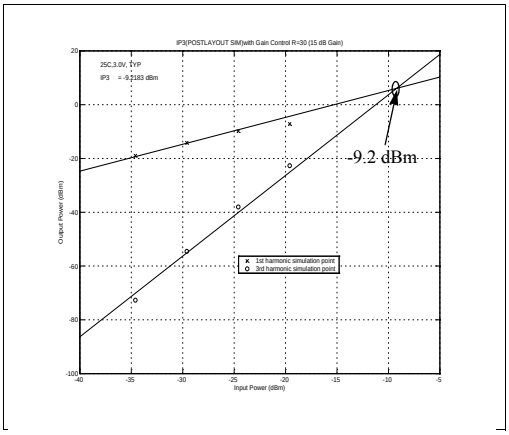


Figure 5. IP3 (IF Mixer + IF Amp)

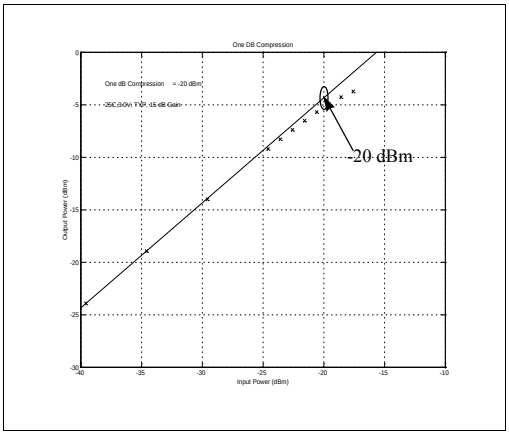


Figure 6. P1dB (IF Mixer + IF Amp)

TRANSMITTER:

RFVCO:

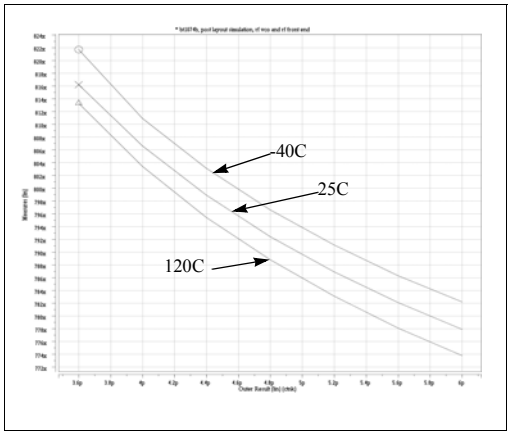


Figure 7. Freq vs. Cap., varying temp.

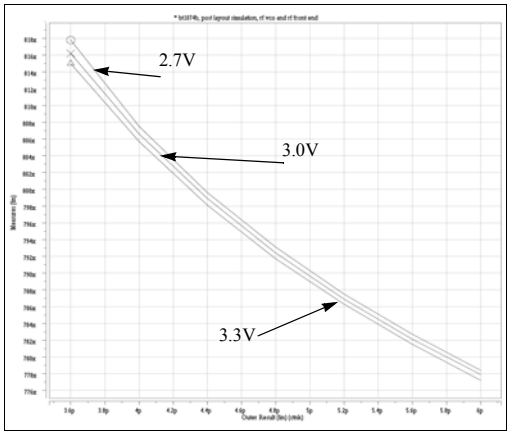


Figure 8. Freq vs. Cap., varying vdd

IFVCO:

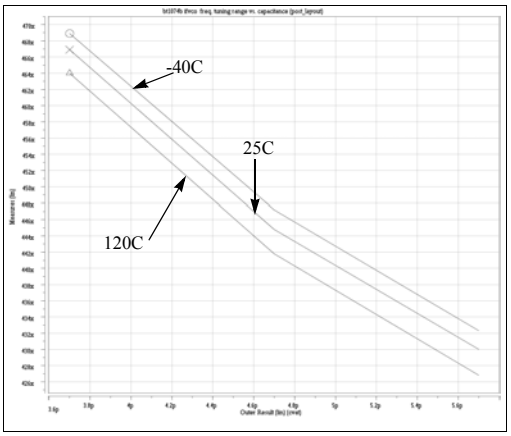


Figure 9. Freq vs. Cap., varying temp.

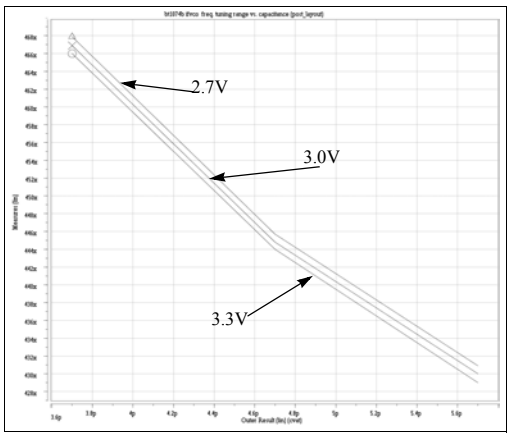


Figure 10. Freq vs. Cap., varying vdd

APPLICATION INFORMATION:

The BT1074Bi is a complete RF transceiver which integrates the receiver, transmitter and local oscillator functions into one chip. Designed to operate in TDD mode, the chip supports ISM band applications, including DSS.

The example described here (and shown in the **Application Circuit**) shows the BT1074Bi used in a 902-928MHz product. Only the RF VCO, IF VCO and power combiner impedance component matching values need to be changed to use the BT1074Bi for other frequency bands (i.e. 868-870MHz).

902-928MHz Example

The transmitter accepts I&Q inputs from the system interface which also provides the DC reference level to M_REF pin. An on-chip RF filter removes spurious signals before going to the on-chip power amplifier. RF outputs are differential and a power combining network is required for converting to a single-ended interface with an output load (see *Application Circuit on page 15*). A power control pin selects between high or low transmission power mode, which ranges from -4dBm to +17dBm. The power level can also be set with resistors at REXT2 and REXT1 pins.

In the receiver section, an on-chip bandpass filter is provided between the LNA output and downconverter mixer input for optimum noise performance. The first IF outputs at 110.592MHz are differential and require a power combiner. The second IF mixer downconverts the first IF signal from 110.592MHz to 10.7MHz by an external crystal clock input at 99.892MHz. A gain-adjustable IF amplifier provides additional gain up to 20dB.

The RF local oscillator and the transmitter IF oscillator are conveniently provided on-chip and can be used with an external dual PLL frequency synthesizer. Both the RF and IF local oscillators require external tuning elements, as shown in the *Application Circuit on page 15*.

The receiver, transmitter, and the two oscillators can each be put into sleep mode with on-chip power-down control pins. These functions can be turned on or off by a microcontroller. For example, in the receiving mode, the microcontroller will turn on the receiver and will turn off the transmit function. The RF and IF VCOs will always be on during the TX and RX mode. In the transmitting mode, the microcontroller will turn on the transmitter and will turn off the receiver function.

The recommended usage of the BT1074Bi is shown in the digital spread spectrum system block diagram on the next page in **Figure A**:

Digital Spread Spectrum System Block Diagram

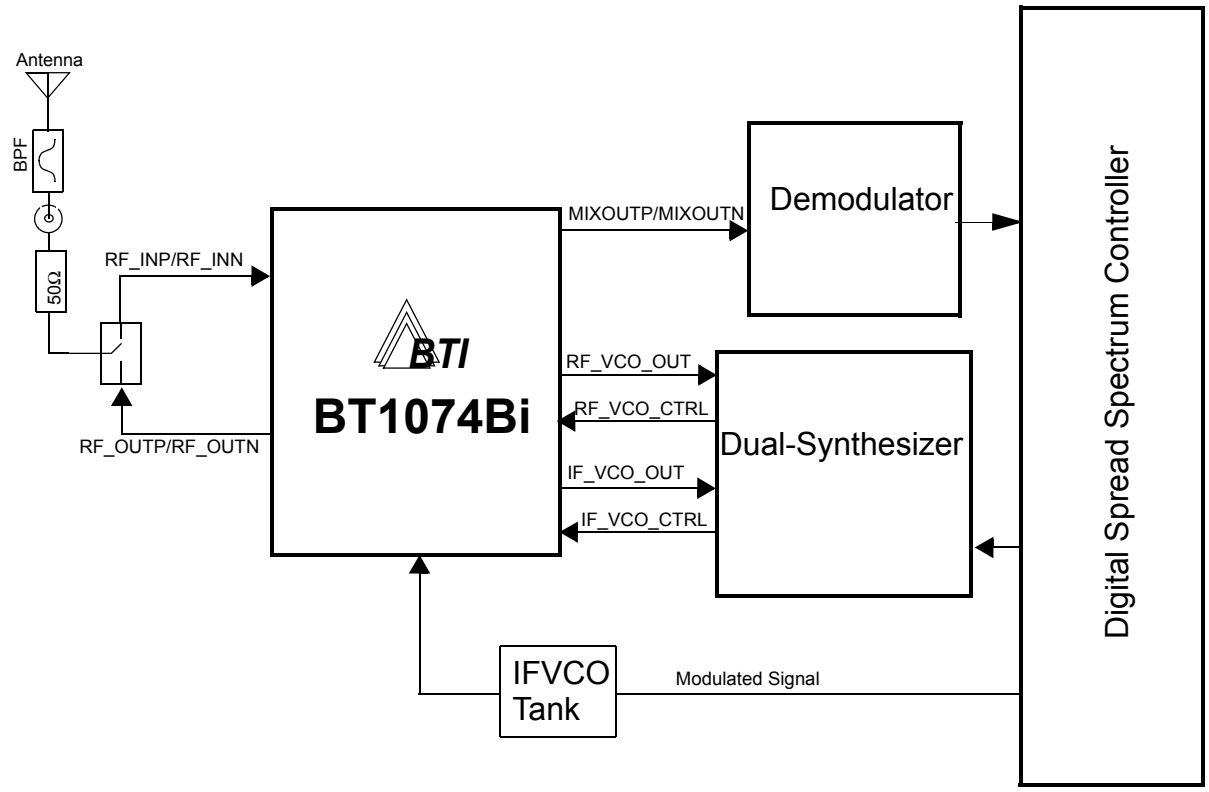


Figure A

APPLICATION CIRCUIT: I & Q INPUT MODULATION

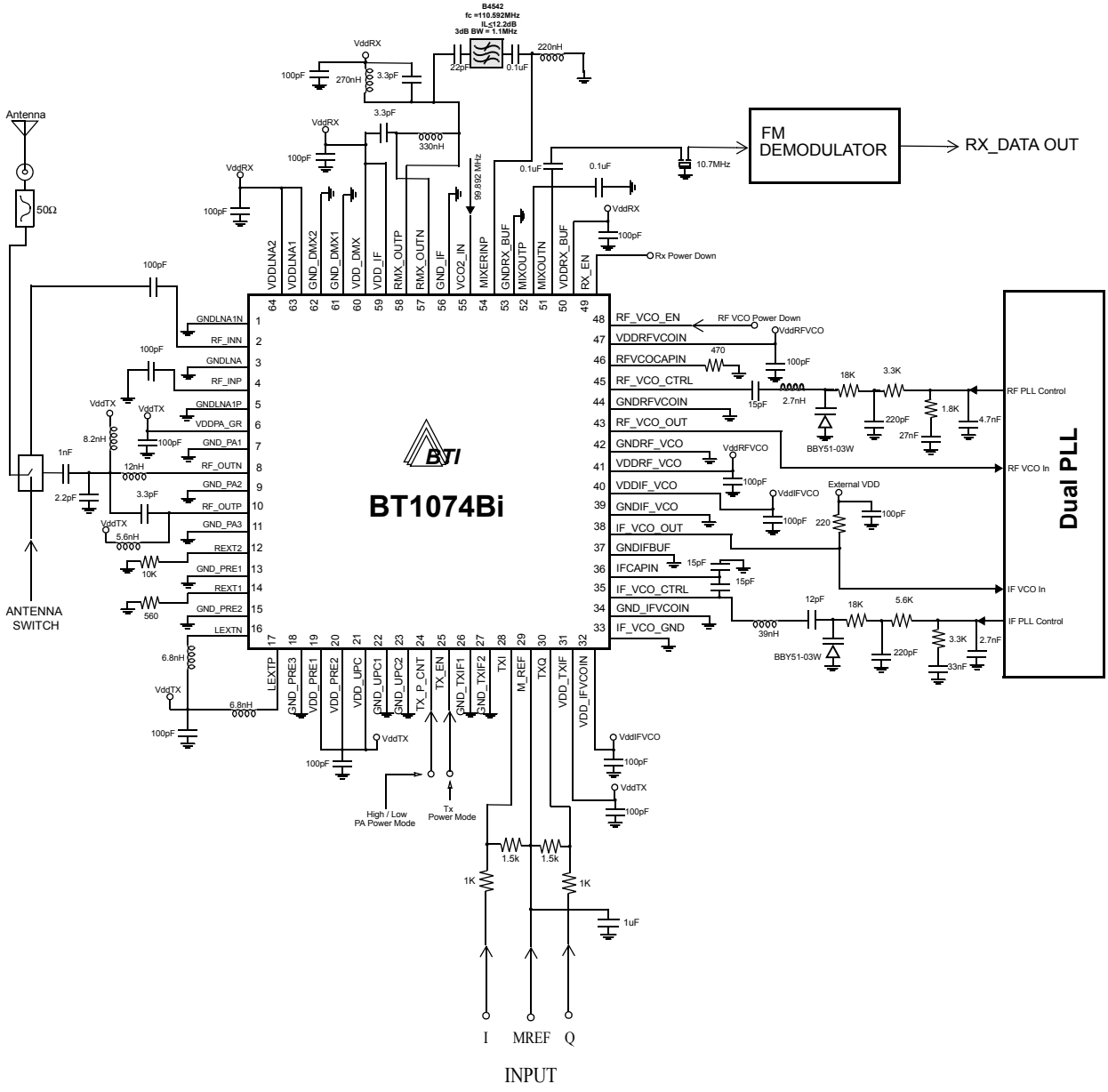


Figure C

APPLICATION CIRCUIT: DIRECT INPUT MODULATION AT IFVCO

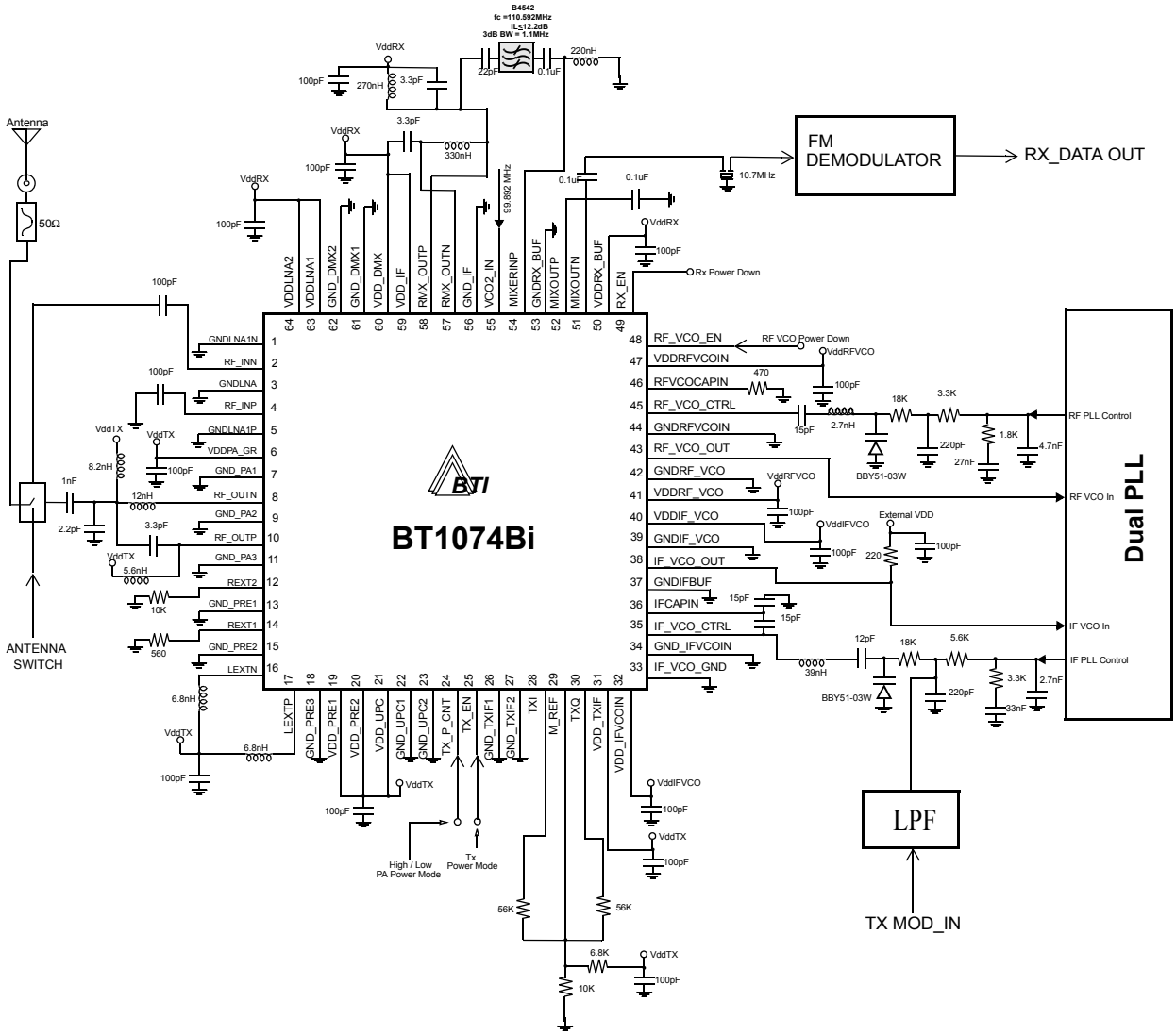
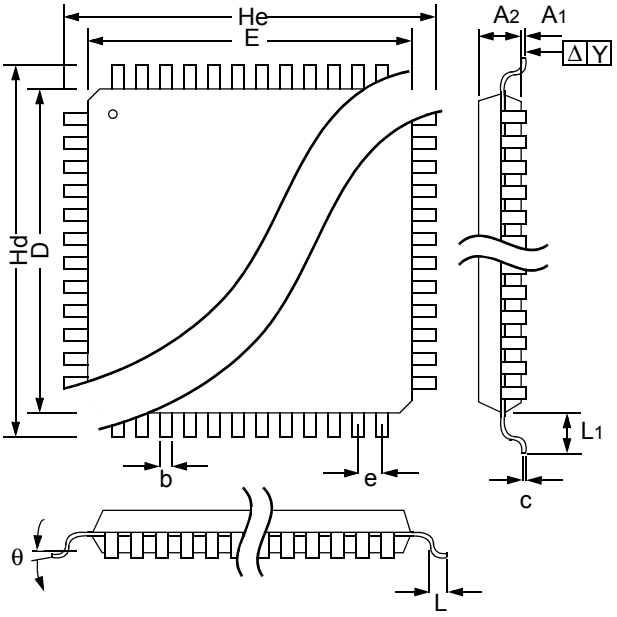


Figure B

Package Dimensions



10x10x1.0 64 LD TQFP PACKAGE:

Sym-bol	Millimeter			Inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A1		0.10			.004	
A2		1.00			.039	
b		0.2			.008	
c		0.127			.005	
D	9.90	10.00	10.10	0.390	0.394	0.398
E	9.90	10.00	10.10	0.390	0.394	0.398
e		0.50			0.020	
Hd	11.90	12.00	12.10	0.468	0.472	0.476
He	11.90	12.00	12.10	0.468	0.472	0.476
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Y			0.08			0.003
θ	0		7	0		7

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