Articia Sa

PRODUCT HIGHLIGHTS

High Integration

64-bit-Wide PCIX/PCI Bus

Low Cost

Triple DES

DMA

iMemory

Multi-Platform Capability

Highly Integrated
Articia Sa is a highly-integrated PowerPC companion chipset. Harnessing the industry-leading CPU bus speed of 166 MHz, the cutting-edge 333 MHz DDR SDRAM, the stunning graphic capability from AGP4X, and the extended data throughput of 64-bit PCI, the multi-missioned Articia Sa brings down system cost while offering phenomenal performance.

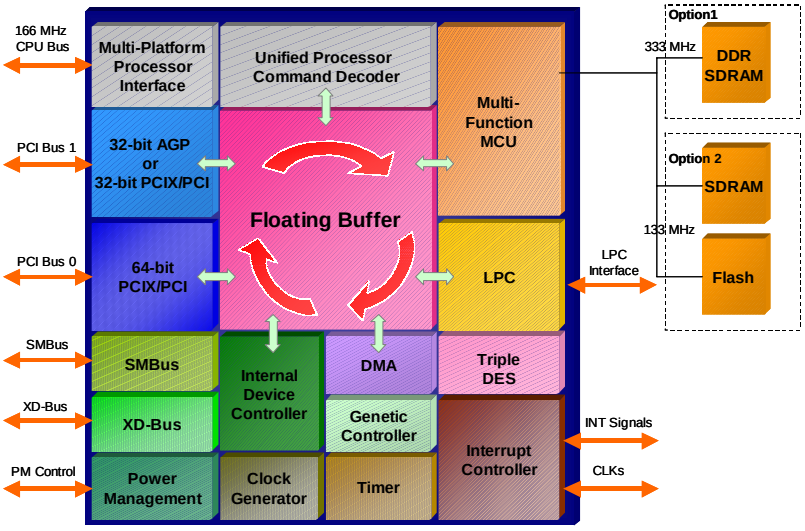
Highly Affordable
Articia Sa offers a most powerful and yet affordable solution for the innovative pervasive computing markets. By incorporating all critical functionalities such as the programmable Interrupt Controller, the enhanced DMA engine, the integrated Clock Generator, and the Global Timers in one single package, Articia Sa truly realizes “total solution.”

Triple DES for Guaranteed Security
Armed with the hardware-based Triple DES, Articia Sa guarantees a secure processing environment and eliminates overhead in data execution through software encryption and decryption cycles.

Unique DMA Capabilities
Articia Sa integrates a DMA Controller, which supports 4 independent channels with direct mode and chain mode. This DMA engine enables extremely fast, massive data transfer among Peripheral-to-Memory, Memory-to-Peripheral, Peripheral-to-Peripheral, and Memory-to-Memory-- a tremendous performance booster.

iMemory
With the choice of 333 MHz DDR SDRAM or 133 MHz SDRAM, Articia Sa delivers a flexible, high-bandwidth design environment. Its iMemory technology facilitates run-time fault detection and in-field fault recovery. The rapid re-mapping table ensures real-time memory error protection.

Multi-Platform Support
Articia Sa supports PowerPC processors at up to 166MHz CPU bus frequency. Its Symmetric Multiprocessing (SMP) architecture ensures smooth operation of dual processors based systems. The Unified Processor Command Decoder enables multi-platform support, including support for MIPS and x86.



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Mai Logic

ARTICIA Sa

Articia Sa

PRODUCT FEATURES

Processor Support

- Support leading PowerPC CPUs including IBM 750CX/CXe, 750FX, and Motorola MPC74XX series processors
- Both 60x and MPX bus protocols compliant
- Full SMP support for dual processors
- Handle four outstanding requests
- 64-bit 166MHz CPU bus interface with data parity (2.5V/3.3V I/O tolerance)

Multi-Function Memory Controller

- Support 64/128/256/512/1024 Mb SDRAM

333MHz DDR SDRAM Interface

- 72-bit DRAM Data Path (full ECC support) with over 2 GB/sec bandwidth
- Support up to 8 physical banks in 4 DDR DIMMs; 8 DRAM pages can be opened simultaneously
- Addressable memory space from 16MB up to 4GB

133MHz SDRAM Interface

- 72-bit DRAM Data Path (full ECC support) with over 1GB/sec bandwidth
- Support up to 8 physical banks in 4 DIMMs; 8 DRAM pages can be opened simultaneously
- Addressable memory space from 16MB up to 4GB

PROM/Flash ROM Support

- Up to 512MB Progammable ROM supported on memory bus
- Up to 512MB Flash ROM supported on memory bus

Floating Buffer

- The smart thread cache engine with optimal read/write buffer allocation
- Achieve zero initial wait state for PCI devices access such as 3-1-1-1-…-1 in Read Hit Cycles
- Support multiple data transfer protocols including page reordering, page merge write, and cache line merge write
- Prefetch/Read Ahead and Merge Write features for CPU, PCI bus 0, and AGP/PCI bus 1
- Four-port concurrency control among CPU, Memory, PCI 0 and AGP/PCI bus 1 interfaces
- Hidden Snoop/Snoop Ahead features with no interference to CPU normal data cycles

PCIX/PCI Bus 0

64-bit PCIX/PCI

- Configurable 64-bit 133MHz PCIX or 64/32-bit 66/33MHz PCI interfaces
- XD-Bus decoding and NVRAM support
- Bus arbitration unit supports up to 5 external PCI masters
- 8MB of addressable memory space for PROM/Flash memory on XD-Bus
- Up to 4 split transactions supported

AGP2X/PCIX/PCI Bus 1

32-bit AGP 2X

- 16 pipelined requests with reordering capability
- Software transparent one-level TLB translation
- 16-entry GART table cache
- 32-Qword read return queue and 20-Qword write data queue
- AGP 4X and sideband address protocol support

32-bit PCIX/PCI

- Bus arbitration unit supports up to 3 external PCI masters
- Configurable 32-bit PCIX or 32-bit 66/33MHz PCI interfaces
- Up to 4 split transactions supported

Integrated DMA Controller

- Support 4 DMA channels
- Two PCI buses accessible (PCI bus 0 and PCI bus 1)
- Direct/chain mode support with self-looping capability
- Triple DES encryption engine supported
- Misaligned transfer supported
- Run-time memory fault detection

Integrated Interrupt Controller

- Fully compatible with OpenPIC/8259 standard
- Up to 5 external interrupt sources in direct mode
- Up to 16 serial interrupts supported

Articia Sa

PRODUCT FEATURES

Patented iMemory Technology

- Run-time memory fault detection
- In-field memory fault recovery

Low Pin Count (LPC) Interface

- Allow connection to legacy ISA and X-Bus devices such as Super I/O
- DMA transfer supported

Power Management Controller (PMC)

- Global timers/counters
- Dynamic PowerPC power management compliant
- 4 levels of power-saving modes supported: Full-on, Doze, Nap, Sleep

Add-on Features

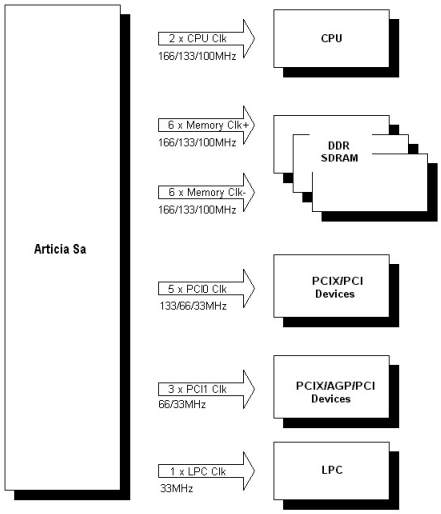
- Triple DES encryption engine
- Patented Genetic Computing
- Configurable general purpose I/O signals
- Programmable I/O driving current control
- Adjustable timing delay capability

Technology

- 0.25µm, 2.5V core, 3.3V I/O
- PBGA package (35mmX35mm substrate)
- Tri-Tier Bonding technology
- 824 pin count

Integrated Clock Generator

- 2 x CPU bus clock outputs at 166/133/100MHz
- 6 pairs x memory clock outputs at 166/133/100MHz
- PCIX/PCI/AGP clock outputs at 133/66/33MHz
- LPC clock output at 33MHz
- Clock timing delay control
- Reduced clock skew and jitter for higher signal quality



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