ChromaCast

82C205

LCD Monitor Controller

Advance Information

CONFIDENTIAL

Revision 1.0

912-1000-024

7/8/99

OPTi Inc.

1440 McCarthy Blvd.

Milpitas, CA 95035

Tel: (408) 486-8000

Fax: (408) 486-8001

WWW: http://www.opti.com

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1. Features

Digital Input Support

- 24-bit digital input
- 300 Mb/sec data rate

Full Screen Image Scaling At All Resolutions

- Incoming video scaled via high quality interpolation/decimation filters to full panel screen size

Multiple LCD Panel Type Support

- 9, 12, 18, 24, 36 bit TFT panel resolution from 640x480 up to 1280x1024
- Drives Single/Multiple Pixels per Clock
- 90 Hz panel refresh rate for TFT

Super OSD Support

- 16-color OSD support
- Transparent, translucent, inverted video, and blinking color attribute support

Multi-sync support

- Supports incoming video with resolutions from 640x480 up to 1280x1024
- Automatic incoming resolution detection
- Horizontal frequency from 15 to 70 kHz
- Vertical frequency from 40 to 85 Hz

Host Interface

- Direct 8-bit micro-controller interface (8051-compatible)

LCD TV Support

- Direct video decoder interface support for LCD TV applications
- High quality scale up algorithm for TV input

VESA Compliant

- DPMS for Display Power Management
- FPDI-1 Flat Panel Display Interface
- LVDS and PanelLink transceiver interface for FPDI-2 (24 bpp mode)

Electrical/Physical Specification

- 0.35 mm process
- 3.3 Volt power supply
- 5V-tolerant I/O
- 208 PQF package

2. Overview

This data book describes the ChromaCast 82C205 LCD monitor controller, a cost reduced solution for LCD (liquid crystal display) monitor control from OPTi Inc. The ChromaCast solution supports a 64-bit DRAM interface for data buffering, an 8051-compatible micro-controller interface, a 24-bit digital interface that can be used with an RGB A/D converter, a PanelLink™ receiver, or an NTSC/PAL decoder, and direct drive control for TFT panels.

ChromaCast 82C205 is packaged in a 208-pin PQF package. 82C205 is a cost-effective, high-performance universal panel controller. Figure 1 shows a system configuration using the 82C205.

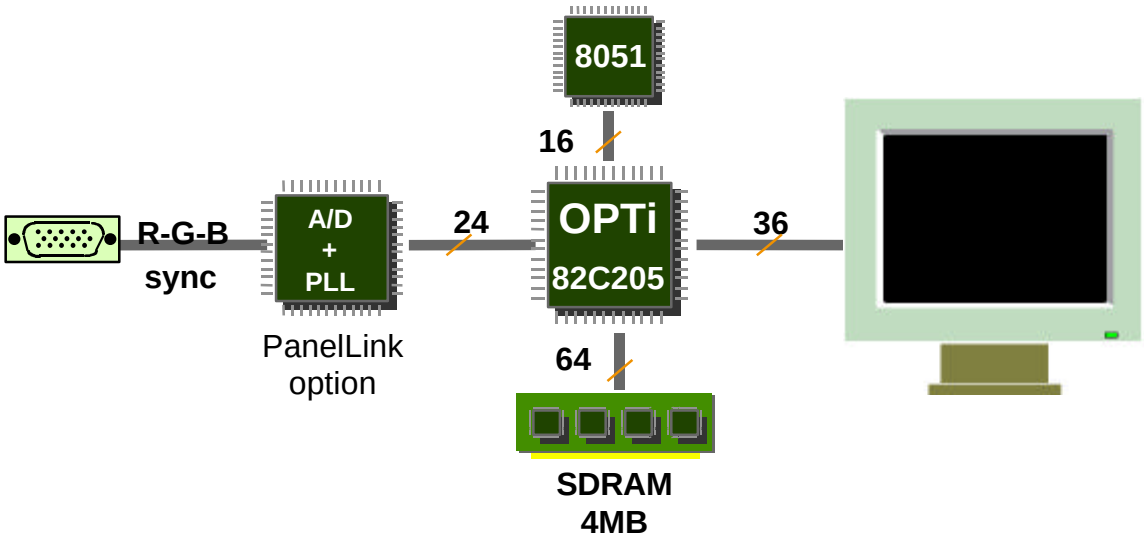
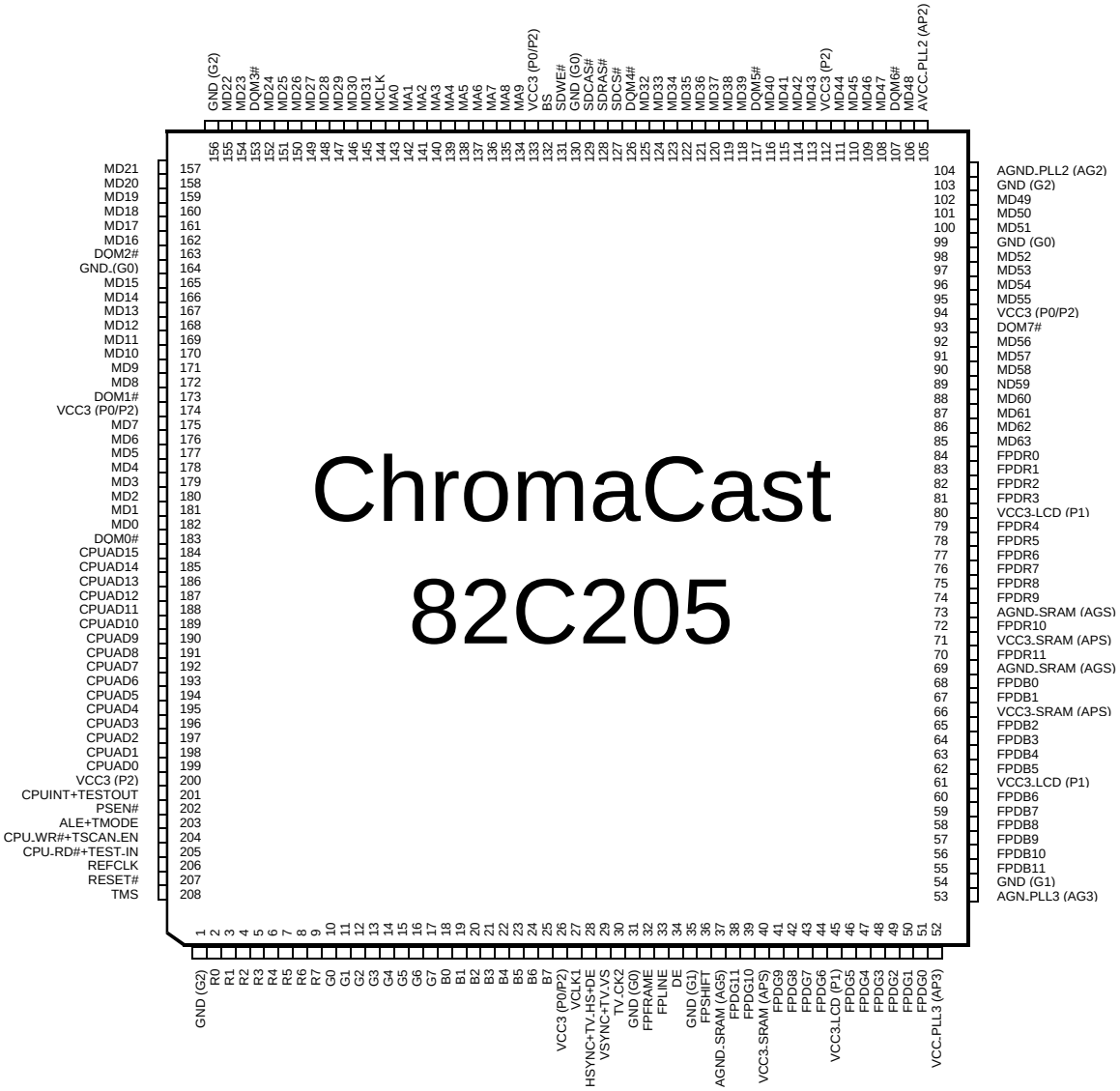


Figure 1. ChromaCast 82C205 System Diagram

3. Signal Definitions

3.1. Pin Diagram



3.2. Pin Listing

Pin No.	Signal Name
1	GND (G2)
2	R0
3	R1
4	R2
5	R3
6	R4
7	R5
8	R6
9	R7
10	G0
11	G1
12	G2
13	G3
14	G4
15	G5
16	G6
17	G7
18	B0
19	B1
20	B2
21	B3
22	B4
23	B5
24	B6
25	B7
26	VCC3 (P0/P2)
27	VCLK1
28	HSYNC+TV_HS
29	VSYNC+TV_VS
30	TV_CK2
31	GND (G0)
32	FPFRAME
33	FPLINE
34	DE

Pin No.	Signal Name
35	GND (G1)
36	FPSHIFT
37	AGND_SRAM (AGS)
38	FPDG11
39	FPDG10
40	VCC3_SRAM (APS)
41	FPDG9
42	FPDG8
43	FPDG7
44	FPDG6
45	VCC3_LCD (P1)
46	FPDG5
47	FPDG4
48	FPDG3
49	FPDG2
50	FPDG1
51	FPDG0
52	VCC3_PLL3 (AP3)
53	AGND_PLL3 (AG3)
54	GND (G1)
55	FPDB11
56	FPDB10
57	FPDB9
58	FPDB8
59	FPDB7
60	FPDB6
61	VCC3_LCD (P1)
62	FPDB5
63	FPDB4
64	FPDB3
65	FPDB2
66	VCC3_SRAM (APS)
67	FPDB1
68	FPDB0

Pin No.	Signal Name
69	AGND_SRAM (AGS)
70	FPDR11
71	VCC3_SRAM (APS)
72	FPDR10
73	AGND_SRAM (AGS)
74	FPDR9
75	FPDR8
76	FPDR7
77	FPDR6
78	FPDR5
79	FPDR4
80	VCC3_LCD (P1)
81	FPDR3
82	FPDR2
83	FPDR1
84	FPDR0
85	MD63
86	MD62
87	MD61
88	MD60
89	MD59
90	MD58
91	MD57
92	MD56
93	DQM7#
94	VCC3 (P0/P2)
95	MD55
96	MD54
97	MD53
98	MD52
99	GND (G0)
100	MD51

Pin No.	Signal Name
101	MD50
102	MD49
103	GND (G2)
104	AGND_PLL2 (AG2)
105	AVCC_PLL2 (AP2)
106	MD48
107	DQM6#
108	MD47
109	MD46
110	MD45
111	MD44
112	VCC3 (P2)
113	MD43
114	MD42
115	MD41
116	MD40
117	DQM5#
118	MD39
119	MD38
120	MD37
121	MD36
122	MD35
123	MD34
124	MD33
125	MD32
126	DQM4#
127	SDCS#
128	SDRAS#
129	SDCAS#
130	GND (G0)
131	SDWE#
132	BS
133	VCC3 (P0/P2)
134	MA9
135	MA8
136	MA7

Pin No.	Signal Name
137	MA6
138	MA5
139	MA4
140	MA3
141	MA2
142	MA1
143	MA0
144	MCLK
145	MD31
146	MD30
147	MD29
148	MD28
149	MD27
150	MD26
151	MD25
152	MD24
153	DQM3#
154	MD23
155	MD22
156	GND (G2)
157	MD21
158	MD20
159	MD19
160	MD18
161	MD17
162	MD16
163	DQM2#
164	GND (G0)
165	MD15
166	MD14
167	MD13
168	MD12
169	MD11
170	MD10
171	MD9
172	MD8

Pin No.	Signal Name
173	DQM1#
174	VCC3 (P0/P2)
175	MD7
176	MD6
177	MD5
178	MD4
179	MD3
180	MD2
181	MD1
182	MD0
183	DQM0#
184	CPUAD15
185	CPUAD14
186	CPUAD13
187	CPUAD12
188	CPUAD11
189	CPUAD10
190	CPUAD9
191	CPUAD8
192	CPUAD7
193	CPUAD6
194	CPUAD5
195	CPUAD4
196	CPUAD3
197	CPUAD2
198	CPUAD1
199	CPUAD0
200	VCC3 (P2)
201	CPUINT+TESTOUT
202	PSEN#
203	ALE+TMODE
204	CPU_WR#+TSCAN_EN
205	CPU_RD#+TEST_IN
206	REFCLK
207	RESET#
208	TMS

3.3. Signal Descriptions

3.3.1. Terminology/Nomenclature Conventions

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms "assertion" and "negation" are used extensively. This is done to avoid confusion when working with a mixture of "active low" and "active high" signals. The term "assert", or "assertion", indicates that a signal is active, independent of whether that level is represented by a high or low voltage. The term "negate", or "negation", indicates that a signal is inactive.

3.3.2. CPU and System Interface

Signal Name	Pin No.	Signal Type	Signal Description
CPU_RD# TEST_IN	205	I	CPU active low read strobe when TMS=0. Test Input for Nand Tree and Tri-state tests when TMS=1
CPU_WR# TSCAN_EN	204	I	CPU active low write strobe when TMS=0. Reserved Input for tests when TMS=1
ALE+TMODE	203	I	CPU Address latch enable. ChromaCast latches address from CPU address/data bus at negative edge of ALE. When TMS=1, TMODE selects between NAND tree and tri-state testing (see Section 3.4, "Test Mode Signals").
CPUAD_[15:5] CPUAD_[7:0]	190 - 199	I I/O	CPU address/data bus bits [15:0] Low Byte ([7:0]) is multiplexed data and the lower address byte. Upper Byte (15:8) is upper address byte.
CPUINT + TESTOUT	201	O	CPU active low interrupt when TMS=0. Test Output for Nand Tree and Tri-state Tests when TMS=1
RESET#	207	I	ChromaCast System Reset (active low). The minimum RESET time is 1ms, i.e. the RESET signal should stays active for at least 1ms after power is stabilized.
REFCK	206	I	Reference Clock. 14.318 MHz reference clock driven externally. This same 14MHz clock must be used to drive the external microcontroller.
PSEN#	202	I	Program strobe enable. Active low signal indicates that the CPU needs to fetch a progarm instruction.
TMS	208	I	Test Mode Select – Sets test mode at power-up (see Secton 3.4, "Test Mode Signals"). TMS=0: Normal operation TMS=1: Test mode

3.3.3. NTSC/PAL Decoder Interface

Signal Name	Pin No.	Signal Type	Signal Description
R[7:0]	2-9	I	Digital Red Input
G[7:0]	10-17	I	Digital Green Input – OR – Digital Luminance Data input for 16-bit NTSC/PAL Decoder Interface or Digital Luminance and Chrominance Data input for 8-bit NTSC/PAL Decoder Interface.
B[7:0]	18-25	I	Digital Blue Input – OR – Digital Chrominance Data input for 16-bit NTSC/PAL Decoder Interface.
VCLK1	27	I	Video Capture Clock from external line-locked PLL
TV_CK2	30	I	Clock from the NTSC/PAL Decoder.
HSYNC TV_HS	28	I	Horizontal Sync signal from VGA – OR – HREF signal from NTSC/PAL Decoder
VSYNC TV_VS	29	I	Vertical Sync signal from VGA – OR – Odd/Even flag from NTSC/PAL Decoder.

3.3.4. DRAM Interface

Signal Name	Pin No.	Signal Type	Signal Description
DQM#[7:0]	93, 107, 117, 126, 153, 163, 173, 183	O	Data Mask (DQM) for SDRAM.
BS	132	O	SDRAM Bank Select (Active low)
MCLK	144	I/O	Memory clock for Memory Controller and SDRAM. Internal MCK PLL or External oscillator provides this clock.
MD[63:0]	See Sec 3.1	I/O	Memory data bus (64-bit).
MA[9:0]	134 - 143	O	Memory address bus signals.
SDRAS#	128	O	SDRAM RAS (Active Low)
SDCAS#	129	O	SDRAM CAS (Active Low)

Signal Name	Pin No.	Signal Type	Signal Description
SDCS#	127	O	SDRAM Chip Select (Active Low) EDO RAS (Active Low)
SDWE#	131	O	Write Enable (Active Low)

3.3.5. Panel Interface Signals

Signal Name	Pin No.	Signal Type	Signal Description
FPFRAME	32	O	Flat panel FRAME signal. Analogous to vertical sync. Programmable polarity.
FPLINE	33	O	Flat panel line signal. Analogous to horizontal sync. Programmable polarity.
FPSHIFT	36	O	Shift clock. Analogous to pixel clock. Shift Clock can be programmed to be gated by DE.
DE	34	O	Panel enable (data ready) signal for display. Also known as DRDY.
FPDR[11:0]	70-83	O	Flat Panel Red Display Data for TFT Mode (See Section 3.3.6.1 below for complete mapping)
FPDG[11:0]	39-57	O	Flat Panel Green Display Data (See Section 3.3.6.1 below for complete mapping)
FPDB[11:0]	55-68	O	Flat Panel Blue Display Data (See Section 3.3.6.1 below for complete mapping)

3.3.6. Power and Ground Signals

Signal Name	Pin No.	Signal Type	Signal Description
VCC3 (P0/P2)	26, 94, 112, 133, 174, 200	P	Core power plane. Also supplies I/O power for CPU, YUV and DRAM.
VCC_SRAM (APS)	40, 66, 71	P	SRAM power plane
VCC_PLL2 (AP2)	105	P	PLL2 power plane
VCC3_PLL3 (AP3)	52	P	PLL3 power plane
VCC3_LCD (P1)	45, 61, 80	P	Power plane for LCD

Signal Name	Pin No.	Signal Type	Signal Description
AGND_SRAM (AGS)	37, 69, 73	P	Analog ground for SRAM
AGND_PLL2 (AG2)	104	P	Analog ground for PLL2
AGND_PLL3 (AG3)	53	P	Analog ground for PLL3
GND (G0)	31, 99, 130, 164	G	Digital ground for core plane
GND (G1 and G2)	1, 35, 54, 103, 156,	G	Digital ground for all I/O planes

3.3.6.1. TFT Panel Data Pin Mapping

(O: pixel#1,3,5…; E: pixel#2,4,6…)

Mode	Red (O)	Red (E)	Green (O)	Green (E)	Blue (O)	Blue (E)
A-333-S09	FPDR[7:5]		FPDG[7:5]		FPDB[7:5]	
A-333-S18	FPDR[7:5]	FPDR[15:13]	FPDG[7:5]	FPDG[15:13]	FPDB[7:5]	FPDB[15:13]
A-444-S12	FPDR[7:4]		FPDG[7:4]		FPDB[7:4]	
A-444-S24	FPDR[7:4]	FPDR[15:12]	FPDG[7:4]	FPDG[15:12]	FPDB[7:4]	FPDB[15:12]
A-666-S18	FPDR[7:2]		FPDG[7:2]		FPDB[7:2]	
A-666-S36	FPDR[7:2]	FPDR[15:10]	FPDG[7:2]	FPDG[15:10]	FPDB[7:2]	FPDB[15:10]
A-888-S24	FPDR[7:0]		FPDG[7:0]		FPDB[7:0]	

3.4. Test Mode Signals

Signal Name	Pin No.	Signal Type	Signal Description
TMS	208	I	Test Mode Select – Sets mode at power-up **TMS TMODE Operation Mode** 0 0 Normal 0 1 Reserved 1 0 NAND-tree operation 1 1 Tri-state operation
TESTIN	205	I	Test Input for Nand Tree and Tri-state tests
TESTOUT	201	O	Test Output for Nand Tree and Tri-state Tests

3.5. Power and Ground Pins

Signal Name	Pin No.	Signal Type
GND (G0)	31	G
GND (G0)	99	G
GND (G0)	130	G
GND (G0)	164	G
GND (G1)	35	G
GND (G1)	54	G
GND (G2)	1	G
GND (G2)	103	G
GND (G2)	156	G
AGND_SRAM (AGS)	37, 69, 73	G

Signal Name	Pin No.	Signal Type
AGND_PLL2 (AG2)	104	G
AGND_PLL3 (AG3)	53	G
VCC3 (P0/P2)	26	P
VCC3 (P0/P2)	94	P
VCC3 (P0/P2)	133	P
VCC3 (P0/P2)	174	P
VCC3 (P2)	112	P
VCC3 (P2)	200	P
VCC3_LCD (P1)	45	P
VCC3_LCD (P1)	61	P

Signal Name	Pin No.	Signal Type
VCC3_LCD (P1)	80	P
AVCC_PLL2 (AP2)	105	P
VCC3_PLL3 (AP3)	52	P
VCC3_SRAM (APS)	40	P
VCC3_SRAM (APS)	66	P
VCC3_SRAM (APS)	71	P

3.6. Power Up Strapping Assignments

3.6.1. Panel Type

Signal Name	Signal Description
MD[9:6]	At power-up, these pins strap the panel type. A 4.7KΩ resistor to ground represents 0. 0000 = Reserved 0001 = Reserved 0010 = Reserved 0100 = A333-S09 0101 = A444-S12 0110 = A666-S18 0111 = A888-S24 1000 = A333-S18 1001 = A444-S24 1010 = A666-S36 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved

3.6.2. Register Base Address Strapping

Signal Name	Signal Description
MD[5:0]	At power-up, these pins strap a portion of the register base address for ChromaCast's register file, which corresponds to address bits [13:8] of the micro-controller bus. The setting 01h is not allowed due to a conflict with the CLUT BASE default. **Bit 5 4 3 2 1 0 Operation** 0 0 0 0 0 0 Fixed address at 8000h 0 0 0 0 0 1 Relocate Address to 8100h --- --- 1 1 1 1 1 1 Relocate Address to BF00h

4. Functional Description

4.1. Internal Block Diagram

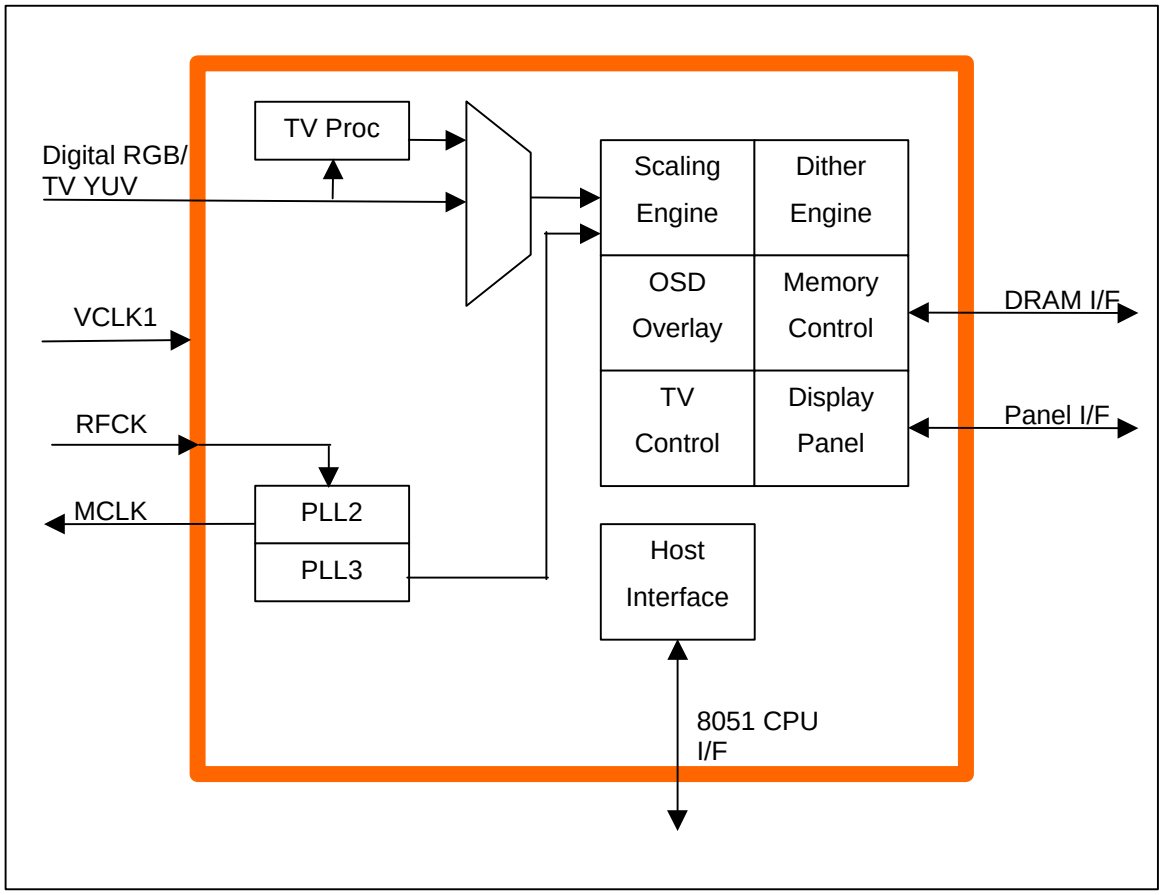


Figure 2. ChromaCast Internal Block Diagram

4.2. Micro-Controller Interface

The 82C205 interfaces to the popular 8051-compatible micro-controller with a shared 16-bit address and data bus (8-bit). The 82C205 provides the micro-controller with one interrupt source, which can be used by the programmer to monitor the status of the 82C205.

The micro-controller can access the registers of the 82C205, the Color Look-Up Table (CLUT), and the DRAM frame buffer. Since the internal address of the frame buffer is 22 bits wide, the 82C205 uses a bank switching technique in order to allow the micro-controller access to the entire memory address space.

4.3. Input Source

The 82C205 supports 24-bit digital input. This 24-bit digital input port can be connected to a TV decoder, external ADC and PanelLink™ receiver. The 82C205 can also generate its own internal test patterns and syncs that can be used for system integration tests.

4.4. Automatic Resolution Detection

The 82C205 monitors the horizontal and vertical syncs from the VGA and performs automatic polarity detection, as well as determination of the horizontal sync frequency and the incoming image resolution. Changes in the horizontal sync frequency and the input image resolution can be configured to prompt an interrupt when these changes occur. The micro-controller can then read the system status and then re-program the 82C205 appropriately.

A fully programmable capture CRTC can be adjusted by the programmer to align with incoming data, based upon the status information that the 82C205 provides.

4.5. TV Mode

The 82C205 chip can be used to turn the LCD monitor into a TV monitor. If the system design for the monitor includes a TV input and NTSC/PAL decoder, then the 82C205 can enable the flat panel to display television signals. Both 16- and 8-bit interfaces to TV decoders are supported, which offers the designer the flexibility of using a less expensive decoder. The 82C205 requires an ODD/EVEN flag as its vertical sync, and the HREF signal as its horizontal sync.

4.6. Full Scale and Centering Options

Scaling is always an important issue for multi-sync monitors, so the 82C205 uses high quality filters to perform image scaling, both horizontally and vertically. Even low resolution images, such as the output from a TV decoder, can be displayed at the full panel resolution. A “centering” option also allows for a smaller resolution image to be displayed on a larger panel with its original resolution surrounded by a black border.

4.7. Contrast/Brightness Control

Contrast and brightness are adjusted digitally on the 82C205, with built in clamping to prevent overflow and underflow. The contrast and brightness controls exist for each color component separately (R-G-B), so color weighting can also be performed by adjusting the contrast of each component to give a component a certain weight relative to the other color components.

$$R_o = R_i * Contrast_R + Brightness_R$$
$$G_o = G_i * Contrast_G + Brightness_G$$
$$B_o = B_i * Contrast_B + Brightness_B$$

4.8. On Screen Display

The 82C205 supports 8 color OSD. Using the attribute control of the 82C205, the programmer is able to build on-screen menus with transparency, translucency, video inversion, and blinking special effects.

The OSD region on the display is defined as a rectangular region. The rectangular region’s size and location on the display are controlled by programmable registers, so the OSD can be of any size, and be located at any coordinate on the display.

The micro-controller writes the bitmap data for the rectangular OSD region to a DRAM buffer. The OSD data in the DRAM buffer contains a 4-bit index into a Color Look Up Table (CLUT) register which is internal to the 82C205 and is also programmable by the micro-controller.

The CLUT contains 16 entries each using 6 bits to describe a 3-bit RGB color value, a 2-bit attribute value to control the overlay graphics, and a 1-bit alpha blend value to control the global alpha value or translucency of the of the overlay graphics. Figure 3 illustrates the organization of the CLUT.

Bit[5]	Bit[4]	Bit[3]	Bits[2:1]	Bit[0]
Red	Green	Blue	Overlay	α

Figure 3. CLUT contents

A global alpha is defined for the entire table, and each entry is tagged with an alpha-blend flag. Inverted video, transparent and blinking attributes are also supported in this mode.

Using the alpha blend value, the OSD graphics can be composited with the video stream controlled by a blend factor in order to create a translucent effect. Pixels in the defined rectangular OSD region that the programmer wishes to be "blank" graphics, i.e. the underlying video is clearly visible, can attach the "transparent" attribute to the OSD pixel. The formula used to control alpha blending is as follows:

$$\text{Output} = \text{Video} * (1-\alpha) + \text{OSD} * (\alpha)$$

Attributes further expand the OSD effects, with an invert attribute (which inverts the video data) and a blink attribute, which performs a hardware controlled blink using a programmable blink rate.

4.9. Dithering

Some flat panels do not provide a 24-bit "true color" interface, so the challenge is to achieve the effect of true color when the panel itself supports less than a full color display. OPTi uses an advanced dithering technique which delivers a true color effect on all display types.

4.10. Versatile Panel Support

The 82C205 is configurable to support a wide range of active matrix displays with resolutions of 640 x 480, 800 x 600, 1024 x 768, and 1280 x 1024 pixels. TFT displays with 9-, 12-, 18-, and 24-bits per pixel are supported. 82C205 also supports multiple pixels per clock and provides a 36-bit interface for panel support.

The synchronization signals to the flat panel are controlled by a fully programmable display CRTC. Positive and negative polarity syncs are supported. In addition to the horizontal and vertical syncs, and the pixel clock for the panel, a data ready (DE) signal is also provided for TFT displays

4.11. Clock Generation

82C205 contains two internal PLLs that are used to generate the clocks necessary for operation. In addition to these two clocks, which control the video processing unit and the memory subsystem, the 14.318 Mhz reference clock is also used internally. This 14.319Mhz same as the system clock for the micro-controller interface.

- PLL2 (MCK) uses the 14.318 MHz reference clock to generate the clock for the memory controller. This clock frequency should match the speed of the DRAM. For SDRAM, a 100 MHz clock is recommended.
- PLL3 (VCLK2) uses the 14.318 MHz reference clock to generate the display clock for the video processing unit. This is also the clock that will be used to drive the panel and its frequency is closely linked to the panel specifications.

4.12. DRAM Interface

82C205 contains an integrated memory controller that supports 64-bit SDRAM. There is also a bypass mode available for some TFT panels that can be used to eliminate the need for a frame buffer, but at the cost of reduced functionality, such as loss of the TV support option.

5. Register Descriptions

5.1. Revision Register

7	6	5	4	3	2	1	0
Index 00h			**Chip Revision (R)**				**Default = 00h**
Chip Revision							

5.2. System Control Register

7	6	5	4	3	2	1	0
Index 01h				**System Enable (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Add one clock for CPU read/write: 0: Enable 1: Disable	CPU DRAM Access: 0: Enable 1: Disable	Video Display Control 0: Disable 1: Enable	Video Capture Control 0: Disable 1: Enable
Index 02h				**Software Reset (R/W)**			**Default = 00h**
These software resets allow the CPU flexibility for debug and power down functions. The default value is zero and software reset is unnecessary at startup							
Reserved	Reserved	Capture Reset: 0: Normal 1: Reset	Display Reset: 0: Normal 1: Reset	Reserved	Memory Controller Reset: 0: Normal 1: Reset	Reserved	Timer Reset: 0: Normal 1: Reset the timer

5.3. Memory Control Registers

7	6	5	4	3	2	1	0
Index 04h				**Capture Start Address - Field 1 (R/W)**			**Default = 00h**
Starting address for Video Capture Field 1 -- Low Byte							
Index 05h							**Default = 00h**
Starting address for Video Capture Field 1 -- Middle Byte							
Index 06h							**Default = 00h**
Reserved	Reserved	Starting address for Video Capture Field 1 -- High Byte					
Index 07h				**Capture Start Address - Field 2 (R/W)**			**Default = 00h**
Starting address for Video Capture Field 2 -- Low Byte							
Index 08h							**Default = 00h**
Starting address for Video Capture Field 2 -- Middle Byte							
Index 09h							**Default = 00h**
Reserved	Reserved	Starting address for Video Capture Field 2 -- High Byte					

7	6	5	4	3	2	1	0
Index 0Ah -0Ch			**Reserved**				**Default = 00h**
Index 0Dh			**OSD Start Address (R/W)**				**Default = 00h**
Starting address of OSD Index Buffer Low Byte							
Index 0Eh							**Default = 00h**
Starting address of OSD Index Buffer Middle Byte							
Index 0Fh							**Default = 00h**
Reserved	Reserved	Starting address of OSD Index Buffer High Byte					
Index 10h			**Display Panel Start Address – Field 1 (R/W)**				**Default = 00h**
Starting address for Display buffer. This is the starting address for field 1 of the TV or VGA data. Low Byte							
Index 11h							**Default = 00h**
Middle Byte							
Index 12h							**Default = 00h**
Reserved	Reserved	High Byte					
Index 13h			**Display Panel Start Address – Field 2 (R/W)**				**Default = 00h**
Starting address for Display buffer. This is the starting address for field 2 of the TV data. Low Byte							
Index 14h							**Default = 00h**
Middle Byte							
Index 15h							**Default = 00h**
Reserved	Reserved	High Byte					
Index 16h			**Video Pitch (R/W)**				**Default = 00h**
Pitch of the Frame Buffer. Low Byte							
Index 17h							**Default = 00h**
Reserved	Reserved	Reserved	High Byte				
Index 18h - 19h			**Reserved**				**Default = 00h**
Index 1Ah			**OSD Pitch (R/W)**				**Default = 00h**
Pitch of the OSD Index Buffer Low Byte							
Index 1Bh							**Default = 00h**
Reserved	Reserved	Reserved	High Byte				
Index 1Ch			**Memory Bank (R/W)**				**Default = 00h**
Bank Address for DRAM access by CPU. The CPU address is structured so that the resultant memory address is: bank[7:0], cpu_addr[21:14] Hence, each bank is 16Kbytes, with 256 available banks.							

7	6	5	4	3	2	1	0
Index 1Dh			**Sequencer Control (R/W)**				**Default = 20h**
Reserved	Reserved	Arbiter Client Acknowledge Overlap: This bit should be set to 1 (default) for optimal memory performance. It allows for greater throughput for internal client requests.	Reserved	Reserved	Reserved	Reserved	Reserved
Index 1Eh			**Refresh Rate Control (R/W)**				**Default = FFh**
Number of reference clock cycles between refresh requests (f = 14.318Mhz, T = 70ns). The duration between refresh requests should be 1/3 of the maximum refresh interval for a row. Low Byte							
Index 1Fh							**Default = FFh**
High Byte							
Index 20h - 21h			**Reserved**				**Default = 00h**
Index 22h			**SDRAM Control 0 (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	CAS Latency = 3: 0: Disable 1: Enable	SDRAM Burst Type: 0: Sequential 1: Interleave	SDRAM Burst Length: 00: Burst Length = 1 01: Burst Length = 2 10: Burst Length = 4 11: Burst Length = 8	
Index 23h			**Reserved**				**Default = 00h**
Index 24h			**CLUT Base Address (R/W)**				**Default = 01h**
Reserved	Reserved	Color Look Up Table Base Address. This 6-bit value corresponds to bits [13:8] of the micro-controller address. Default = 1 (REGBASE should NOT be strapped to '1'.)					
Index 25h			**TV Weave Mode (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	TV Weave Mode Capture Pitch Adjust: 0: Enable 1: Disable (See note below.)
Note: If set to '1', adjusts the Capture Pitch to twice the Video Pitch if selected in order to accommodate TV Weave mode. TV Weave mode captures both fields of the TV image in an interleaved manner. (Sets Capture Pitch = 2 * Video Pitch.)							
Index 26h			**CPU Memory Read Buffer (R)**				**Default = 00h**
CPU Memory Read Buffer Status This register latches the CPU read data from memory and can be used by the microcontroller to perform a "double read".							

7	6	5	4	3	2	1	0
Index 27h			**Arbiter State (R)**				**Default = 00h**
This register can be used to detect a lock-up of the arbiter. For debug purposes only.							
Reserved	Reserved	Reserved	Arbiter State Status				
Index 28h			**Sequencer State (R)**				**Default = 00h**
This register can be used to detect a lock-up of the memory sequencer. For debug purposes only.							
Reserved	Reserved	Reserved	Sequencer State Status				

5.4. OSD Registers

7	6	5	4	3	2	1	0
Index 29h				**OSD Configuration (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	OSD Blink Background Select: 0: Blink to Video Background 1: Blink to CLUT Index0 Background	OSD function: 0: Disable (default) 1: Enable	Reserved
Index 2Ah				**OSD Window Horizontal Offset (R/W)**			**Default = 00h**
Horizontal Offset for the rectangular OSD region referenced from the far left of the display and in units of display pixels. Low Byte							
Index 2Bh				**OSD Window Horizontal Offset (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 2Ch				**OSD Horizontal Size (R/W)**			**Default = 00h**
Width of rectangular OSD region in units of display pixels. Low Byte							
Index 2Dh				**OSD Horizontal Size (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 2Eh				**OSD Window Vertical Offset (R/W)**			**Default = 00h**
Vertical Offset for the rectangular OSD region referenced from the top of the display and in units of display lines. Low Byte							
Index 2Fh				**OSD Window Vertical Offset (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 30h				**OSD Vertical Size (R/W)**			**Default = 00h**
Height of rectangular OSD region in units of display lines. Low Byte							
Index 31h				**OSD Vertical Size (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		

7	6	5	4	3	2	1	0
Index 32h			**Blink Rate for OSD (R/W)**				**Default = 00h**
Blink Rate for On Screen Display. Blink Rate is in units of frames. Setting the blink rate to 30 means that the OSD will appear for 30 frames, then disappear for 30 frames. The OSD will blink only if the blink attribute is selected							
Index 33h - 37h			**Reserved**				**Default = 00h**

5.5. Dither Register Settings

7	6	5	4	3	2	1	0
Index 38h				**Primary Bits (R/W)**			**Default = 00h**
Capture Data Bits: Bits per pixel color component for dither capture data.				Reserved (set to 0)		Dither Line Depth Select: For TFT: Dither Line Depth = (8 - Primary Bits) / 2	
Index 39h				**Dither Control (R/W)**			**Default = FAh**
Reserved (set to 1)	Reserved (set to 1)	Reserved (set to 1)	Reserved (set to 1)	Reserved (set to 2)		Reserved (set to 2)	
Index 3Ah				**Dither Threshold (R/W)**			**Default = 00h**
Adjustment of this value can reduce Moire pattern effects.							
Index 3Bh				**Dither Algorithm Initializations (R/W)**			**Default = 03h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved (set to 1)	Reserved (set to 1)
Index 3Ch				**Dither Frame and Line Offset (R/W)**			**Default = 00h**
Reserved				Dither Line Offset Function Control: This register setting depends on the values in Register 38h, the Primary Bits, and the Dither Line Depth. 8 - Primary Bits - Dither Line Depth			
Index 3Dh				**Dither Mode (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Index 3Eh - 3Fh				**Reserved**			**Default = 00h**

5.6. Capture CRTC Registers

7	6	5	4	3	2	1	0
Index 40h				**Capture Horizontal Sync Width (R/W)**			**Default = 00h**
Capture Horizontal Sync Width (in units of VCLK1 cycles). Low Byte							
Index 41h				**Capture Horizontal Sync Width (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			

7	6	5	4	3	2	1	0
Index 42h			**Capture Horizontal Display Start (R/W)**				**Default = 00h**
Counter Value that corresponds to the horizontal start location of active video during video capture (in units of VCLK1 cycles). Low Byte							
Index 43h			**Capture Horizontal Display Start (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 44h			**Capture Horizontal Display End (R/W)**				**Default = 00h**
Counter Value that corresponds to the horizontal end location of active video during video capture (in units of VCLK1 cycles). Low Byte							
Index 45h			**Capture Horizontal Display End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 46h			**Capture Horizontal Total (R/W)**				**Default = 00h**
Period of the Horizontal Sync in units of VCLK1. Used when free running the internal capture horizontal sync. Low Byte							
Index 47h			**Capture Horizontal Total (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	High Byte				
Index 48h			**Capture Vertical Sync Start (R/W)**				**Default = 00h**
Starting Location for Vertical Sync Pulse, i.e. counter value in units of capture video lines specifying the delay from the start of the VGA vertical sync going active to when the internal capture vertical sync goes active.							
Index 4Ah			**Capture Vertical Sync End (R/W)**				**Default = 00h**
Ending Location for Vertical Sync Pulse, i.e. counter value in units of capture video lines specifying the delay from the start of the VGA vertical sync going active to when the internal capture vertical sync goes inactive. Low Byte							
Index 4Bh			**Capture Vertical Sync End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 4Ch			**Capture Vertical Display Start (R/W)**				**Default = 00h**
Counter Value that corresponds to the vertical start location of active video in units of capture video lines. Low Byte							
Index 4Dh			**Capture Vertical Display Start (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 4Eh			**Capture Vertical Display End (R/W)**				**Default = 00h**
Counter Value that corresponds to the vertical end location of active video in units of capture video lines. Low Byte							
Index 4Fh			**Capture Vertical Display End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 50h			**Capture Vertical Total (R/W)**				**Default = 00h**
Period of Vertical Sync in units of capture video lines. Used when free running the internal capture vertical sync. Low Byte							
Index 51h			**Capture Vertical Total (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			

7	6	5	4	3	2	1	0
Index 52h			**Synchronization Control (R/W)**				**Default = 03h**
Reserved	Reserved	VGA Vertical Sync: 0: Sync present 1: Sync lost (Read only)	VGA Horizontal Sync 0: Sync present 1: Sync lost (Read only)	VGA Vertical Sync Input Polarity: 0: Positive 1: Negative (Read only)	VGA Horizontal Sync Input Polarity: 0: Positive 1: Negative (Read only)	Synchronize to Vertical Sync: 0: Free run the internal vertical sync: 1: Synchronize to external vertical sync.	Synchronize to Horizontal Sync: 0: Free run the internal horizontal sync: 1: Synchronize to external horizontal sync.
Index 53h			**Reserved**				**Default = 00h**

5.7. Scaling Registers

7	6	5	4	3	2	1	0
Index 54h			**Vertical Scale Ratio (R/W)**				**Default = 00h**
Vertical Scale Ratio for Vertical Decimation: This value is determined by the following formula, where Capture Ysize is the number of lines in the incoming video frame and Display Ysize is the number of lines in the panel: If Capture Ysize < Display Ysize, then Yratio = (Capture Ysize * 1024) / Display Ysize. Otherwise, Yratio = (((Display Ysize * 2048) / Capture Ysize) + 1) / 2. Low Byte							
Index 55h			**Vertical Scale Ratio (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 56h			**Input Y Size (R/W)**				**Default = 00h**
Number of lines per frame in the incoming image Low Byte							
Index 57h			**Input Y Size (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 58h			**Output Y Size (R/W)**				**Default = 00h**
Number of lines per frame in the displayed image (after scaling) Low Byte							
Index 59h			**Output Y Size (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 5Ah			**Vertical Scale-Down Random DDA Initialization (R/W)**				**Default = 00h**
Maximum random initialization value for Vertical scale down DDA (Disable with 01h) Low Byte							
Index 5Bh			**Vertical Scale-Down Random DDA Initialization (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		

7	6	5	4	3	2	1	0
Index 5Ch			**Vertical Scale-Up Random DDA Initialization (R/W)**				**Default = 00h**
Maximum random initialization value for Vertical scale up DDA Low Byte							
Index 5Dh			**Vertical Scale-Up Random DDA Initialization (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Seed Sign Bit: (Adds randomness to vertical scale up.) 0: DDA init value is an unsigned number. 1: DDA init value is a signed number.	High Byte (for Maximum random initialization for Vertical scale up DDA)		
Index 5Eh			**Vertical Scale-Up Mid Point Selection (R/W)**				**Default = 02h**
Reserved	Reserved	Reserved	Reserved	Reserved	TV Mode Even Field: 0: Reverse 1: Normal	DDA Field Compensation: 0: Disable 1: Enable	0: Select DDA Reference 1: Select Mid-Point Reference
Index 5Fh			**Reserved**				**Default = 00h**
Index 60h			**Horizontal Scale Ratio (R/W)**				**Default = 00h**
Horizontal Scale Ratio for Decimation This value is determined by the following formula, where Capture Xsize is the number of pixels per line in the incoming video frame and Display Xsize is the number of pixels per line in the panel: If Capture Xsize > Display Xsize then Xratio = (((Display Xsize * 8192) / Capture Xsize) + 1) / 2 Otherwise, Xratio = 4096 Low Byte							
Index 61h			**Horizontal Scale Ratio (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	High Byte				
Index 62h			**Output X Size (R/W)**				**Default = 00h**
Number of Pixels in a line of the displayed image (after scaling). Low Byte							
Index 63h			**Output X Size (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 64h			**Input X Size (R/W)**				**Default = 00h**
Number of Pixels per line in incoming image (before scaling). Low Byte							
Index 65h			**Input X Size (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		
Index 66h			**Horizontal Scale-Down Random DDA Initialization (R/W)**				**Default = 00h**

7	6	5	4	3	2	1	0
Maximum Random Initialization Value for Horizontal Scale Down DDA Low Byte							
Index 67h			**Horizontal Scale-Down Random DDA Initialization (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte		

5.8. Contrast and Brightness Control Registers

7	6	5	4	3	2	1	0
Index 68h			**Red Contrast Control (R/W)**				**Default = 80h**
Red contrast level (0 to 255) Note: 128 is unity							
Index 69h			**Green Contrast Control (R/W)**				**Default = 80h**
Green contrast level (0 to 255) Note: 128 is unity							
Index 6Ah			**Blue Contrast Control (R/W)**				**Default = 80h**
Blue contrast level (0 to 255) Note: 128 is unity							
Index 6Bh			**Red Brightness Control (R/W)**				**Default = 00h**
Red brightness level (-128 to 127)							
Index 6Ch			**Green Brightness Control (R/W)**				**Default = 00h**
Green brightness level (-128 to 127)							
Index 6Dh			**Blue Brightness Control (R/W)**				**Default = 00h**
Blue brightness level (-128 to 127)							

5.9. Video Input Source Selection Registers

7	6	5	4	3	2	1	0
Index 6Eh				**Anti-Alias Pre-Filter (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Anti-Alias Pre-Filter Operation: 0: Enable 1: Disable **NOTE**: Enable for VGA scale down only.

7	6	5	4	3	2	1	0
Index 6Fh			**Video Input Source Selection (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Overlay grid dots on input pattern: 0: disable (default) 1: enable	Video Input Source Select. Video sources can be from the A/D converters or a test pattern generator: 0000: Reserved 0001: Black color pattern 0010: White color pattern 0011: Grey color pattern 0100: Red color pattern 0101: Green color pattern 0110: Blue color pattern 0111: Horizontal ramp pattern 1000: Horizontal line pattern 1001: Vertical ramp pattern 1010: Vertical line pattern 1011: Alternating block scan patterns 1100: B/W checker board pattern 1101: G&P checker board pattern 1110: Color bar pattern 1111: 4 corner blend pattern			

5.10. Resolution Detection Registers

7	6	5	4	3	2	1	0
Index 70h			**Resolution Counter (R)**				**Default = 00h**
Counter for number of VGA horizontal syncs in a frame (in units of capture video lines). Low Byte							
Index 71h			**Resolution Counter (R)**				**Default = 00h**
High Byte							
Index 72h			**Horizontal Frequency Counter (R)**				**Default = 00h**
Counter for period of VGA horizontal sync (in units of reference clock). Reference clock frequency is 14.318 MHz Low Byte							
Index 73h			**Horizontal Frequency Counter (R)**				**Default = 00h**
High Byte							
Index 74h			**Active Video Top Edge (R)**				**Default = 00h**
The line number of the first line which contains active VGA data after Vertical Sync. Low Byte							
Index 75h			**Active Video Top Edge (R)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			

7	6	5	4	3	2	1	0
Index 76h			**Active Video Bottom Edge (R)**				**Default = 00h**
The line number of the last line which contains active VGA data after Vertical Sync. Low Byte							
Index 77h			**Active Video Bottom Edge (R)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 78h			**Active Video Left Edge (R)**				**Default = 00h**
The first horizontal position that contains active VGA data after Horizontal Sync. Low Byte							
Index 79h			**Active Video Left Edge (R)**				**Default = 00h**
Reserved	Reserved	Reserved	High Byte				
Index 7Ah			**Active Video Right Edge (R)**				**Default = 00h**
The last horizontal position that contains active VGA data after Horizontal Sync. Low Byte							
Index 7Bh			**Active Video Right Edge (R)**				**Default = 00h**
Reserved	Reserved	Reserved	High Byte				

5.11. TV Decoder Interface Registers

7	6	5	4	3	2	1	0
Index 7Ch			**TV Mode (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Phase Counter Offset: These bits are used to adjust the lumninance and chrominance phase offset.		NTSC Decoder data bus width: 0: 16-bit (default) 1: 8-bit	Input Mode: 0: VGA or test pattern input (default) 1: TV input
Index 7Dh			**TV Sync Polarity Adjustment (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Odd/Even Flag Polarity: 0: Positive (typical) 1: Negative	HREF polarity: 0: Positive 1: Negative (typical)

5.12. Display Horizontal Scaling

7	6	5	4	3	2	1	0
Index 7Eh			**Horizontal Scale X Ratio 1 (R/W)**				**Default = 00h**
Horizontal Scale x Ratio 1							
Index 7Fh			**Horizontal Scale X Ratio 2 (R/W)**				**Default = 00h**
Horizontal Scale-Up: 0: Enable 1: Disable	Reserved	Horizontal Scale x Ratio 2					

5.13. Display CRTC Registers

7	6	5	4	3	2	1	0
Index 80h			**Display Horizontal Total (R/W)**				**Default = 00h**
Horizontal Total (in units of VCLK2) Low Byte							
Index 81h			**Display Horizontal Total (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 82h			**Display Horizontal Sync Width (R/W)**				**Default = 00h**
Horizontal Sync Width (in units of VCLK2) Low Byte							
Index 83h			**Display Horizontal Sync Width (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 84h			**Display Horizontal Display Start (R/W)**				**Default = 00h**
Horizontal Display Start Location (in units of VCLK2) Low Byte							
Index 85h			**Display Horizontal Display Start (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 86h			**Display Horizontal Display End (R/W)**				**Default = 00h**
Horizontal Display End Location (in units of VCLK2) Low Byte							
Index 87h			**Display Horizontal Display End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 88h			**Display Vertical Total - Odd Frame (R/W)**				**Default = 00h**
Vertical Total for Odd Frame (in units of display video lines). Low Byte							
Index 89h			**Display Vertical Total - Odd Frame (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			

7	6	5	4	3	2	1	0
Index 8Ah			**Display Vertical Total - Even Frame (R/W)**				**Default = 00h**
Vertical Total for Even Frame (in units of display video lines). If odd and even frames have the same vertical total, this register still needs to be programmed. Low Byte							
Index 8Bh			**Display Vertical Total - Even Frame (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 8Ch			**Display Vertical Sync Width (R/W)**				**Default = 00h**
Vertical Sync Width (in units of display video lines) Low Byte							
Index 8Dh			**Display Vertical Sync Width (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 8Eh			**Display Vertical Display Start (R/W)**				**Default = 00h**
Vertical Display Start (in units of display video lines) Low Byte							
Index 8Fh			**Display Vertical Display Start (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 90h			**Display Vertical Display End (R/W)**				**Default = 00h**
Vertical Display End (in units of display video lines) Low Byte							
Index 91h			**Display Vertical Display End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 92h			**Vertical Sync Signal Offset Control (R/W)**				**Default = 05h**
Defines the delay in units of capture video lines, from the rising edge of the capture vertical sync to the rising edge of the display vertical sync Low Byte							
Index 93h			**Vertical Sync Signal Offset Control (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	High Byte			
Index 94h				**Bypass Mode HSYNC Offset (R/W)**			**Default = 06h**
Reserved				High Byte			
Index 95h				**Bypass Mode HSYNC Offset (R/W)**			**Default = 0Ah**
Defines the delay in units of VCLK2 display HSYNC to capture HSYNC in bypass mode. Low Byte							
Index 96h				**Reserved**			**Default = 00h**

7	6	5	4	3	2	1	0
Index 97h			**Synchronization Control (R/W)**				**Default = 03h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0: Free run display vertical sync. 1: Synchronize display vertical sync to capture vertical sync.	0: Free run display horizontal sync. 1: Synchronize display horizontal sync to capture horizontal sync.
Index 98h			**Panel Display Window Horizontal Start (R/W)**				**Default = 00h**
Horizontal Start of Panel Display Window (in units of VCLK2) Low Byte							
Index 99h			**Panel Display Window Horizontal Start (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Horizontal Start of Panel Display Window (in units of VCLK2) High Byte			
Index 9Ah			**Panel Display Window Horizontal End (R/W)**				**Default = 00h**
Horizontal End of Panel Display Window (in units of VCLK2) Low Byte							
Index 9Bh			**Panel Display Window Horizontal End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Horizontal End of Panel Display Window (in units of VCLK2) High Byte			
Index 9Ch			**Panel Display Window Vertical Start (R/W)**				**Default = 00h**
Vertical Start of Panel Display Window (in units of display video lines) Low Byte							
Index 9Dh			**Panel Display Window Vertical Start (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Vertical Start of Panel Display Window (in units of display display video lines) High Byte			
Index 9Eh			**Panel Display Window Vertical End (R/W)**				**Default = 00h**
Vertical End of Panel Display Window (in units of display video lines) Low Byte							
Index 9Fh			**Panel Display Window Vertical End (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Vertical End of Panel Display Window (in units of display video lines) High Byte			

5.14. Panel Registers

7	6	5	4	3	2	1	0
Index A0h			**Panel Type (R)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Panel Type. Nomenclature according to FPDI standards: 0000: Reserved 0001: Reserved 0010: Reserved 0011: Reserved 0100: A333-S09 0101: A444-S12 0110: A666-S18 0111: A888-S24 1000: A333-S18 1001: A444-S24 1010: A666-S36 1011: Reserved			
Index A1h			**Panel Sync Signal Control (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Selects where data changes relative to FPSHIFT: 0: Data changes at rising edge of FPSHIFT 1: Data changes at falling edge of FPSHIFT	Selects an FPS Gated by the valid data region. 0: Continuous FPS (TFT) 1: Gate FPS by Valid Data Region (not used)	Flat Panel Frame signal polarity: 0: Active high (default) 1: Active low	Flat Panel Line signal polarity: 0: Active high (default) 1: Active low
Index A2h - A3h			**Reserved**				**Default = 00h**
Index A4h			**Memory Bypass Mode (R/W)**				**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Memory Bypass: 0: Use external DRAM (Default) 1: Bypass DRAM

5.15. Bandwidth Conservation Registers

7	6	5	4	3	2	1	0
Index B0h			**OSD FIFO Word Count (R/W)**				**Default = 00h**
Special register for OSD FIFO control, indicating the number of 64-bit words that will be fetched in one line for OSD.							
Index B1h			**Reserved**				**Default = 00h**
Index B2h			**Panel Display FIFO Word Count (R/W)**				**Default = 00h**
Special register for upper display FIFO control, indicating the number of words that will be fetched for the whole panel.							
Index B3h			**Reserved**				**Default = 00h**

5.16. Interrupt Control Registers

7	6	5	4	3	2	1	0
Index B4h				**Interrupt Enable (R/W)**			**Default = 00h**
VGA Horizontal Frequency Change interrupt: 0: Disable (default) 1: Enable	Display VBI start interrupt: 0: Disable (default) 1: Enable	Display VBI end interrupt: 0: Disable (default) 1: Enable	Capture VBI start interrupt: 0: Disable (default) 1: Enable	Capture VBI end interrupt; 0: Disable (default) 1: Enable	VGA Vertical Frequency Change interrupt: 0: Disable (default) 1: Enable	Timer interrupt: 0: Disable (default) 1: Enable	Reserved
Index B5h				**Interrupt Clear (W)**			**Default = 00h**
VGA Horizontal Frequency Change interrupt clear: Write 1 to clear	Display VBI start interrupt clear: Write 1 to clear	Display VBI end interrupt clear: Write 1 to clear	Capture VBI start interrupt clear: Write 1 to clear	Capture VBI end interrupt clear: Write 1 to clear	VGA Vertical Frequency Change interrupt clear: Write 1 to clear	Timer interrupt clear: Write 1 to clear	Reserved
Index B5h				**Interrupt Status (R)**			**Default = 00h**
VGA Horizontal Frequency Change event status	Display VBI start event status: Occurs at beginning of display vertical sync pulse.	Display VBI end event status: Occurs at end of display vertical sync pulse.	Capture VBI start event status: Occurs at beginning of capture vertical sync pulse.	Capture VBI end event status: Occurs at end of capture vertical sync pulse.	VGA Vertical Frequency Change event status	Timer event status: Occurs when count-down timer reaches zero.	Reserved

5.17. CLUT Access Control

7	6	5	4	3	2	1	0
Index B6h -B7h			**Reserved**				**Default = 00h**

5.18. ADC and PLL Control Registers

7	6	5	4	3	2	1	0
Index B8h C2h			**Reserved**				**Default = 00h**
Index C3h			**VCLK1 Phase Offset (R/W)**				**Default = 09h**
Reserved			Phase offset for VCLK1				
Index C4h			**MCLK PLL Control (R/W)**				**Default = 02h**
14.318 Mhz reference clock * N/M = MCLK frequency							
Divide MCLK PLL output frequency by 2 (If enabled, the output of the MCLK PLL will be divided by 2): 0: Disable 1: Enable	MCLK PLL M Factor (M[5:0])						
Index C5h			**MCLK PLL Control (R/W)**				**Default = 09h**
Reserved	MCLK PLL N Factor (N[6:0])						
Index C6h			**VCLK2 PLL Control (R/W)**				**Default = 02h**
14.318 Mhz reference clock * N/M = VCLK2 frequency							
Divide VCLK2 PLL output frequency by 2: 0: Disable 1: Enable	VCLK2 PLL M Factor (M[5:0])						
Index C7h			**VCLK2 PLL Control (R/W)**				**Default = 03h**
VCLK2 PLL N Factor (N[6:0])							

5.19. Power Management Registers

7	6	5	4	3	2	1	0
Index C8h			**Power Enables for Panel Voltages (R/W)**				**Default = 00h**
This power up/down sequencing is very important. **Improper sequencing can cause panel damage!** These signals default to zero at reset, i.e. inactive.							
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

7	6	5	4	3	2	1	0
Index C9h			**Hardware Enables (R/W)**				**Default = 00h**
Control of Wake-up and Power Down for Power Conservation in the 82C200.							
Master Bias 0: Disable 1: Enable	Reserved (set to 0)	Reserved	Line Buffer Power 0: Disable 1: Enable	VCLK2 PLL Power 0: Disable 1: Enable	MCK PLL Power 0: Disable 1: Enable	Reserved (set to 0)	Reserved
Index CAh			**Timer (R/W)**				**Default = FFh**
General Purpose Count Down Timer (in units of 10 us) to assist the software power sequencing. Generates a timer event whenever it reaches zero. Range from 0~5s. The low byte should be written last, i.e. write the high and mid bytes before the low byte. Low Byte							
Index CBh			**Timer (R/W)**				**Default = FFh**
Mid Byte							
Index CCh			**Timer (R/W)**				**Default = 07h**
Reserved	Reserved	Reserved	Reserved	Reserved	High Byte The high byte should be written first, before writing the mid and low bytes		
Index CDh - CEh			**Reserved**				**Default = 00h**

5.20. CLUT Registers

This is the Color Look Up Table used for the OSD, providing 8 colors available to 16 entries. A global alpha blend value is defined for all blending in this mode, and a 1-bit value for each entry selects whether or not the blend will occur.

Transparent, inverted video, and blinking attributes are also supported.

In the CLUT registers D0h - DFh, the Global Blend Enable and attribute bits (bits 5, 1:0) work together as follows:

000: Normal	X01: Inverted Video
010: Blink, no blend	X11: Transparent
100: Blend	110: Blink, blend

7	6	5	4	3	2	1	0
Index CFh			**CLUT Register Control (R/W)**				**Default = 00h**
Reserved	Reserved	Enable CLUT registers	Global blend value Can be used in place of the Attribute to define a global value for pixel translucency.				
Index D0h			**CLUT0 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	

7	6	5	4	3	2	1	0
Index D1h			**CLUT1 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D2h			**CLUT2 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D3h			**CLUT3 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D4h			**CLUT4 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D5h			**CLUT5 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D6h			**CLUT6 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D7h			**CLUT7 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D8h			**CLUT8 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index D9h			**CLUT9 (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index DAh			**CLUTA (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	

7	6	5	4	3	2	1	0
Index DBh			**CLUTB (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index DCh			**CLUTC (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index DDh			**CLUTD (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index DEh			**CLUTE (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index DFh			**CLUTF (R/W)**				**Default = 00h**
Reserved	Reserved	Global Blend: 0: Disable 1: Enable	Red	Green	Blue	Attribute	
Index E0h - E8h			**Reserved**				**Default = 00h**

5.21. Status Registers

7	6	5	4	3	2	1	0
Index E9h				**Clear FIFO Error (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Writes 1 to clear all the error flags. Write 0 to resume normal operation.
Index EAh				**FIFO Status – Byte 1 (R)**			**Default = 00h**
Reserved	Reserved	OSD FIFO overflow: 0: Normal operation 1: Overflow	OSD FIFO underflow: 0: Normal operation 1: Underflow	Reserved	Reserved	Reserved	Reserved
Index EBh				**FIFO Status – Byte 2 (R)**			**Default = 00h**
Reserved	Reserved	Capture FIFO overflow	Capture FIFO underflow	Display upper FIFO overflow	Display upper FIFO underflow	Reserved	Reserved

7	6	5	4	3	2	1	0
Index Ech			**Capture Signature – Byte 1 (R)**				**Default = 00h**
Capture Signature Signature analyzer output on video capture data stream (used for testing). Low Byte							
Index EDh			**Capture Signature – Byte 2 (R)**				**Default = 00h**
High Byte							
Index EEh			**Display Signature – Byte 1 (R)**				**Default = 00h**
Display Signature Signature analyzer output on video display data stream (used for testing). Low Byte							
Index EFh			**Display Signature – Byte 2 (R)**				**Default = 00h**
High Byte							
Index F0-FBh			**Reserved**				**Default = 00h**

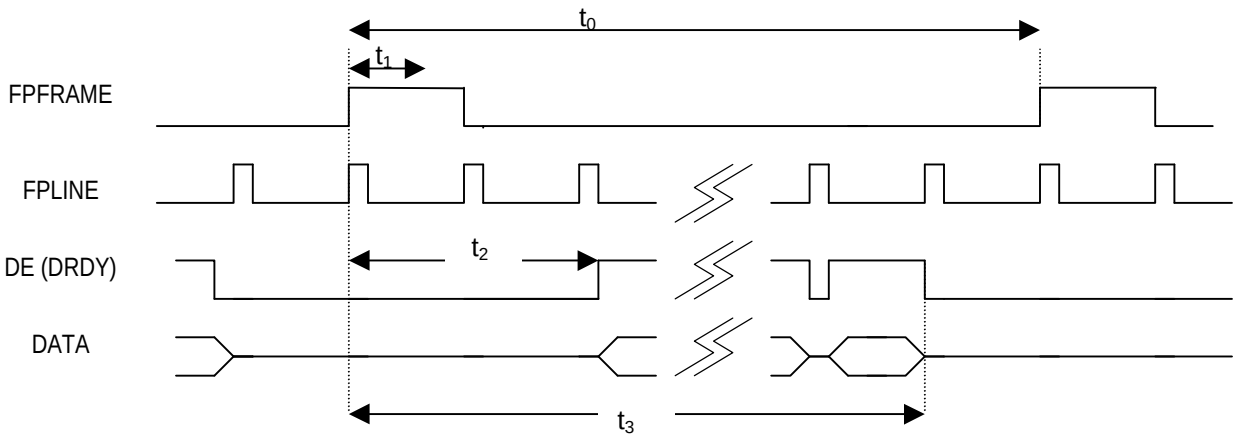
5.22. I/O Control Registers

7	6	5	4	3	2	1	0
Index FCh				**Clock Control (R/W)**			**Default = 00h**
Display Sync Bi-direction control: 0: Input 1: Output	Capture Sync Bi-direction control: 0: Input 1: Output	Reserved	Reserved	Memory Clock Source Selection: 0: External oscillator (default) 1: Internal PLL	Reserved	VCLK1 External Clock Input Invert Selection: 0: No invertion (default) 1: Invert VCLK1	Reserved
Index FDh				**RGB Data Input Selection (R/W)**			**Default = 00h**
Reserved	Reserved	Reserved	Reserved	Reserved	Pull Down Function for Bi-directional Buffer: 0: Disable 1: Enable	Reserved (set to 1**)**	Reserved (set to 1**)**

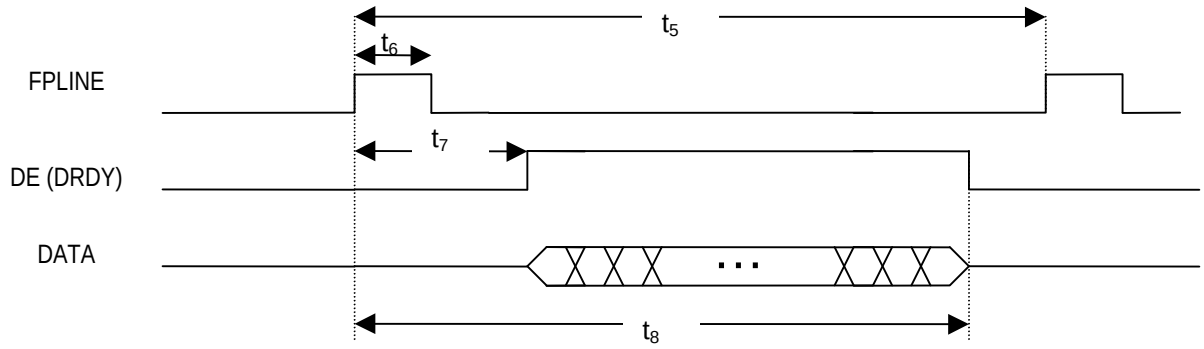
6. Timing Information and Waveforms

Signal	Description	Symbol	Min	Typical	Max	Unit
FPFRAME	Vertical Total	t_0	0		4095	Lines
	Sync Width	t_1	0		4095	Lines
	Vertical Display Start	t_2	0		4095	Lines
	Vertical Display End	t_3	0		4095	Lines
FPLINE	Horizontal Total	t_5	0		4095	Pixel Clock
	Sync Width	t_6	0		4095	Pixel Clock
	Horizontal Display Start	t_7	0		4095	Pixel Clock
	Horizontal Display End	t_8	0		4095	Pixel Clock
DE	Data Valid	t_{10}	0		4095	Pixel Clock
FPSHIFT	Pixel Clock Frequency	t_{11}	10		120	MHz

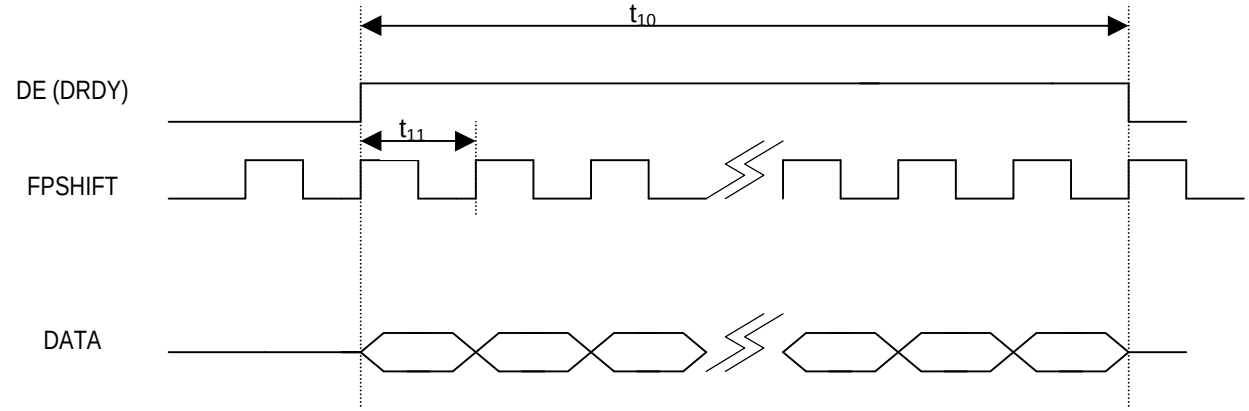
6.1. Vertical Timing for TFT Panel



6.2. Horizontal Timing for TFT Panel



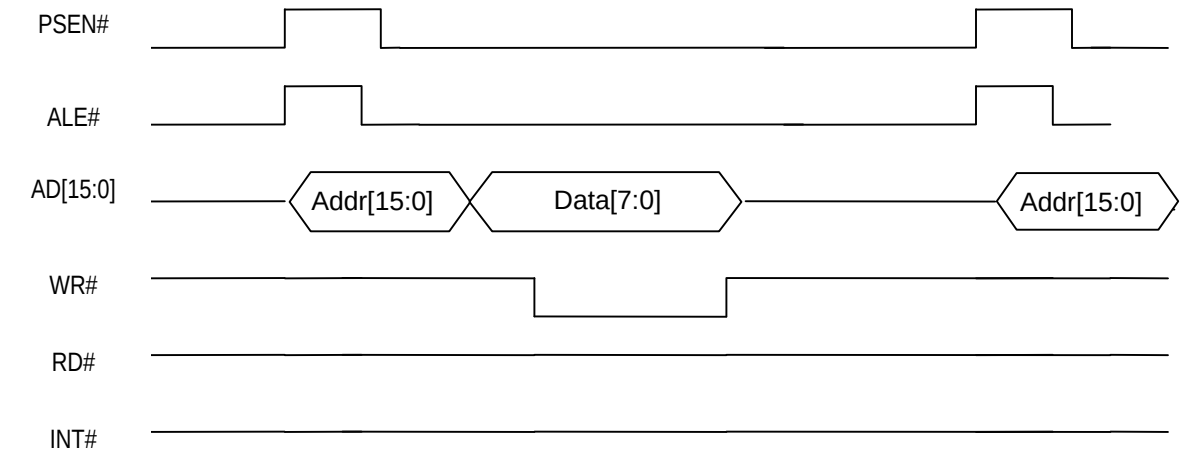
6.3. Detail of Pixel Clock Timing



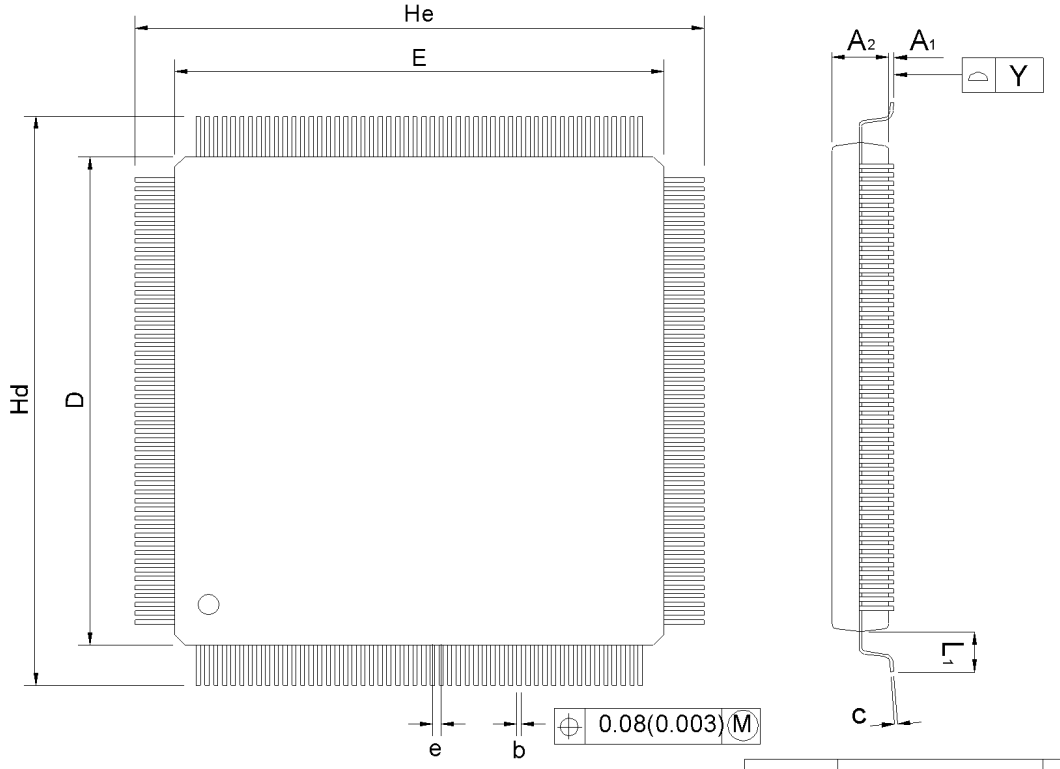
*** Polarity of FPFRAME, FPLINE, & FPSHIFT is programmable.**

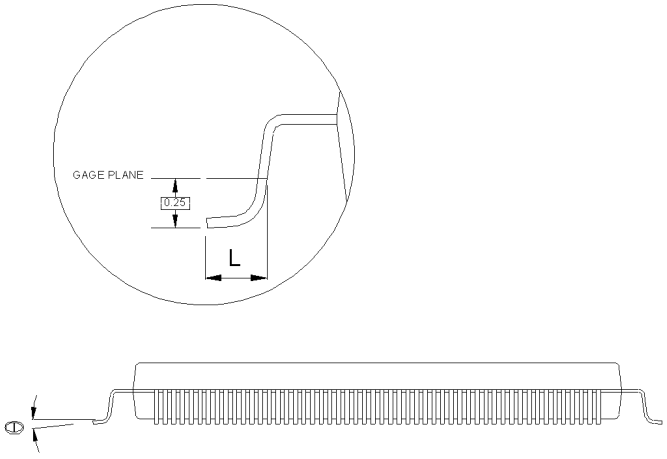
*** One and Two Pixels Per Clock are supported.**

6.4. Micro-Controller Interface



7. 208-Pin PQFP Mechanical Drawing





SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A_1	0.05	0.25	0.50	0.002	0.010	0.020
A_2	3.17	3.32	3.47	0.125	0.131	0.137
b	0.10	0.20	0.30	0.004	0.008	0.012
c	0.10	0.15	0.20	0.004	0.006	0.008
D	27.90	28.00	28.10	1.098	1.102	1.106
E	27.90	28.00	28.10	1.098	1.102	1.106
e		0.50			0.020	
Hd	30.35	30.60	30.85	1.195	1.205	1.215
He	30.35	30.60	30.85	1.195	1.205	1.215
L	0.50	0.60	0.75	0.020	0.024	0.030
L_1		1.30			0.051	
Y			0.08			0.003
θ	0		7	0		7

Dwg. No.:	AS208PQFP-001	
Dwg. Rev.:	A1	Unit: MM / INCH