ESS Technology, Inc.

ES2842
PCI Integrated LAN V.90/V.92 Modem Solution
Product Brief

DESCRIPTION

The ES2842, ESS Technology's first LAN plus host-based *Tele***Drive**® modem chip for the PCI bus, provides desktop and notebook computers with greater connectivity to both packet networks and telephone networks. The ES2842 maximizes integration and reduces the external component BOM cost to a minimum.

The ES2842 device combines into a single-chip a host-based V.90/V.92 modem, modem control buffers, a modem codec, and an IEEE 802.3-compatible Ethernet media access controller (MAC) with an analog phoneline interface and a PCI bus interface. This advanced high-level device integration allows the ES2842 to be used as a host-based modem and LAN solution for desktop and notebook systems requiring either a modem connection or a 10/100 Ethernet connection. The ES2842 is also capable of providing a home network connection that complies with the Home Phoneline Networking Alliance (HomePNA) 1-Mb/s (HPNA1.0) specification.

The ES2842 LAN feature supports 100BASE-TX (100-Mb/s mode) and 10BASE-T (10-Mb/s mode) full-duplex operations. The ES2842 includes a media-independent interface (MII) and reduced MII (RMII), enabling it to interface with an external PHY transceiver used for either a LAN or HPNA-based chipset.

The ES2842 modem sends and receives data and fax information and supports the telephone answering machine (TAM) feature. With its built-in ACPI $D3_{cold}$ wake-on-LAN and wake-on-ring support, the ES2842 is an ideal modem solution for notebooks and battery-operated devices. The ES2842 modem provides the interface and control logic needed to transfer data between its serial I/O terminals and the PCI interface.

The ES2842 delivers a high modem connectivity rate, as well as high throughput without the need of a dedicated DSP. The ES2842 supports worldwide homologation and is capable of data/fax/voice call discrimination. With the addition of an external transformer DAA, the ES2842 provides a very cost-effective modem/LAN solution for add-on card, motherboard, and mini-PCI card implementations.

The ES2842 is available in a 128-pin low-profile quad flat pack (LQFP) package.

FEATURES

- V.90/V.92 analog data/fax/TAM modem
- Data mode capabilities:
  - V.90/V.92: 56 Kbps
  - ITU-T V.34: 33.6 Kbps and fallbacks
- Fax mode capabilities:
  - ITU-T V.17, V.29, V.27ter, and V.21ch2
  - Group 3 (TIA/EIA-578 Class 1 and Class 2)
- Requires minimum 166-MHz Pentium with MMX technology
- Integrated modem codec and analog front end
- 16-bit ADC and DAC with built-in anti-aliasing and reconstruction filters
- Supports external transformer DAA
- 10/100-Mb/s LAN or 1-Mb/s HPNA networking capability
- Integrated on-chip 1/10/100-Mbps MAC controller capable of interfacing with 10Base-T PHY transceiver and with 100Base-TX PHY transceiver
- MII for connecting to external 10/100-Mbps PHY transceiver
- RMII for connecting to external 10/100-Mbps PHY transceiver
- Full-duplex operation supported in MII and RMII ports with independent transmit (TX) and receive (RX) channels
- Support for IEEE 802.3x flow control and IEEE 802.3u auto-negotiation for 10Base-T and 100Base-TX
- EEPROM interface for subsystem ID and subsystem vendor ID
- ACPI and PCI power management standard-compliant
- Wake-on-ring and wake-on-LAN capability
- On-chip FIFOs for PCI bus and both RX and TX state machines
- Supports both RJ-11 tip and ring connection and RJ-45 LAN/Ethernet connection
- PC99/PC2001-compliant with support for V.250, V.251, and V.253 commands
- Worldwide homologation

MODEM DRIVER SUPPORT

- Microsoft Windows 98/SE/ME/2000
- Microsoft Windows NT 4.0

LAN DRIVER SUPPORT

- NIC drivers for Netware 3.x and 4.x networks (16-bit and 32-bit ODI)
- Microsoft Windows networks (NDIS 2.0, 4.0, and 5.0)
- Packet driver

PINOUT

Figure 1 shows the ES2842 pinout diagram.

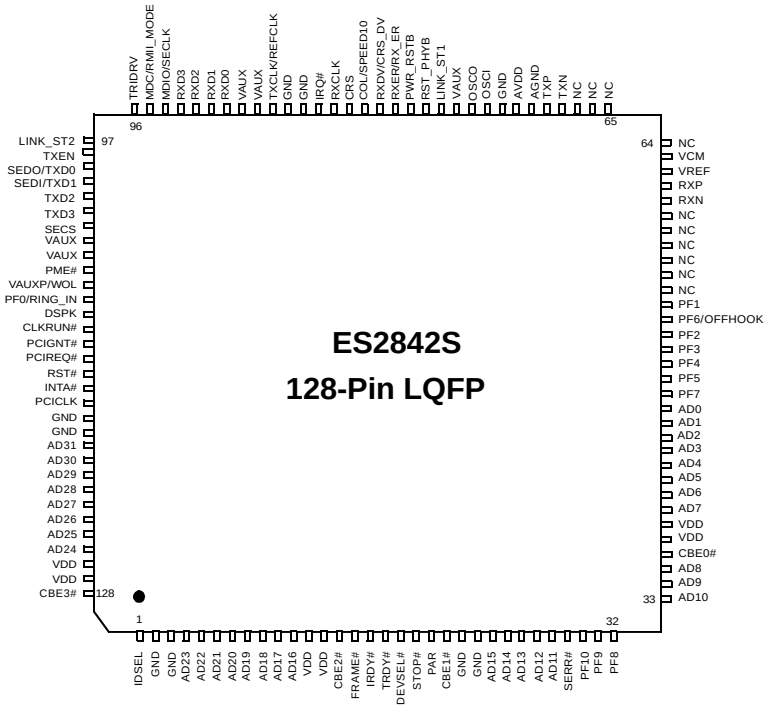

Figure 1 ES2842 Pinout Diagram

PIN DESCRIPTIONS

Table 1 lists the ES2842 pin descriptions.

Table 1 ES2842 Pin Descriptions

Names	Pin Numbers	I/O	Definitions
IDSEL	1	I	ID select.
GND	2, 3, 22, 23, 52, 53, 72, 85, 86, 116, 117	G	Digital ground.
VDD	12, 13, 37, 38, 126, 127	P	3.3V digital power supply.
AD[31:0]	4:11, 24:28, 33:35, 39:46, 118:125	I/O	Address and data lines from the PCI bus.
C/BE[3:0]#	14, 21, 36, 128	I/O	PCI command/byte enable. During address phase of a transaction, these pins define the bus command. During data phase, these pins define the bus enable.
FRAME#	15	I/O	Cycle frame.
IRDY#	16	I/O	Initiator ready.
TRDY#	17	I/O	Target ready.
DEVSEL#	18	I/O	Device select.
STOP#	19	I/O	Stop transaction.
PAR	20	I/O	Parity.
SERR#	29	OD	System bus error.
PF[5:2] and PF1	30:32, 47:51, 55	I/O	General-purpose programmable bidirectional flag. These pins can be used for interfacing with a telephone or other device, performing such functions as caller ID, etc. Refer to pin descriptions of pins 54 and 108 for preprogrammed telephone interface pins.

Table 1 ES2842 Pin Descriptions (continued)

Names	Pin Numbers	I/O	Definitions
PF6	54	O	General purpose programmable flag.
OFFHOOK		O	Offhook output
NC	56:59, 64:67	—	No connect.
RXN	60	I	Codec analog differential receive negative input. The DC level is VCM, and the full-scale input is either 2.2Vp-p±5% or 1.1Vp-p±5%, depending on the gain setting.
RXP	61	I	Codec analog differential receive positive input. The DC level is VCM, and the full-scale input is either 2.2Vp-p±5% or 1.1Vp-p±5%, depending on the gain setting.
VREF	62	O	Voltage reference bypass. Has a range of 1.235V±5%. Bypass to AGND with 0.1-µF ceramic chip capacitor parallel with 10-µF tantalum capacitor.
VCM	63	O	Common mode voltage bypass. Has a range of 2.16V±5%. Bypass to AGND with 0.1-µF ceramic chip capacitor parallel with 10-µF tantalum capacitor.
TXN	68	O	Codec analog differential transmit negative output. The DC level is VCM, and the full-scale input is either 2.8Vp-p±5% or 1.4Vp-p±5%, depending on the gain setting.The maximum loading is 1.2k Ω, in parallel with 20 pF for modem applications.
TXP	69	O	Codec analog differential transmit positive output. The DC level is VCM, and the full-scale input is either 2.8Vp-p±5% or 1.4Vp-p±5%, depending on the gain setting.The maximum loading is 1.2k Ω, in parallel with 20 pF for modem applications.
AGND	70	G	Analog ground.
AVDD	71	P	5V analog power supply.
OSCI	73	I	Crystal clock input.
OSCO	74	O	Crystal clock output.
VAUX	75, 88, 89, 104, 105	P	3.3V V_{AUX} power supply for wake-on-ring and wake-on-LAN.
LINK_ST1	76	I	Link status interface input from PHY.
PHY_RSTB	77	O	Reset output to PHY; will follow PWR_RSTB and remain active for 1.3 msec after PWR_RSTB. Can be toggled by bit 7 of LAN_IO register [4Ah].
PWR_RSTB	78	I	Power-on reset. This is an active-low input signal when a power-on reset event occurs.
RXER	79	I	Receive error input for MII mode. Indicates that the external PHY transceiver has detected coding errors in the receive data frame now being transmitted to RXD[3:0]. RXER is ignored while RX_DV is deasserted.
RX_ER		I	Receive error input for RMII mode. Indicates that the external PHY transceiver has detected coding errors in the receive data frame now being transmitted to RXD[1:0]. RX_ER is ignored while RX_DV is deasserted.
RXDV	80	I	Receive data valid.
CRS_DV		I	Carrier sense/receive data valid. Asserted asynchronously by the PHY when the receive medium is nonidle. In 10Base-T mode, carrier is detected when squelch is passed in RMII mode.
COL	81	I	Collision. When selected as COL, asserted output whenever a collision is detected.
SPEED10		I	Speed select. Acts as toggle for 10-Mb/s and 100-Mb/s operation for external PHY transceiver in RMII mode.
CRS	82	I	Carrier sense input.
RXCLK	83	I	Receive clock input. Provides the nibble rate clock timing reference for the output transfer of RXDV, RXD[3:0], and RXER/RX_ER signals and operates at 25/2.5 MHz.
IRQ#	84	I	Interrupt request.
TXCLK	87	I	Transmit clock input. When selected as TXCLK, provides timing reference for transfer of the transmitted data and operates at 25/2.5 MHz.
REFCLK		I	Reference clock input. When selected as REFCLK, provides continuous clock timing reference for CRS_DV, RXD[1:0], TXEN, TXD[1:0], and RX_ER. Operates at 50 MHz ±50 ppm with a duty cycle between 35% and 65% in RMII mode.
RXD[3:0]	90:93	I	Receive data. When in RMII mode, only RXD[1:0] are defined.
MDIO	94	I/O	When the MDIO function is selected, this pin functions as the MII management data I/O pin. It acts as an output during the header portion of management frame transfers and during the data portion of write operations. It also acts as an input during the data portion of read operations.
SECLK		O	Serial EEPROM data clock input.

Table 1 ES2842 Pin Descriptions (continued)

Names	Pin Numbers	I/O	Definitions
MDC	95	O	When the MDC function is selected, this pin functions as the MII management data clock pin. It runs up to 2.5 MHz.
RMII_MODE		I	RMII_MODE enable. The ES2842 supports both MII and RMII modes. When the RMII_MODE signal is high, RMII mode is supported. When the RMII_MODE signal is low, MII mode is supported. Strap option pin latched at power-on reset.
TRIDRV	96	O	Tri-state output pin connected to the input pin of HPNA PHY to tri-state output of HPNA PHY. When asserted high, this pin tri-states all outputs except open-drain outputs.
LINK_ST2	97	I	Link status Interface input from (second) HPNA PHY.
TXEN	98	O	Transmit enable. This pin indicates that the MAC is presenting valid data on TXD[3:0]. TXEN transitions are latched on the falling edge of REFCLK.
SEDO	99	O	Serial EEPROM data input.
TXD[0]		O	Transmit data output 0.
SEDI	100	I	Serial EEPROM data output with an internal pullup.
TXD[1]		O	Transmit data output 1.
TXD[3:2]	101, 102	O	Transmit data 2 and 3 in MII mode. Not defined in RMII mode.
SECS	103	O	Serial EEPROM port chip select output using 10k Ω pulldown resistor.
PME#	106	OD	Power management enable interrupt output to wake up the system.
VAUXP	107	I	V_{AUX} support detection. V_{AUXP} is driven high at reset to indicate that ACPI is supported with ***D3$_{cold}$*** state. No support when driven low. Strap option pin latched at power-on reset.
WOL		O	Wake-on-LAN signal output. The ES2842 asserts this signal if a change is detected in link status, Magic Packet , or sample frame events.
PF0	108	O	general purpose programmable flag.
RING_IN		I	Ring-in-detection input.
DSPK	109	O	Modem speaker digital output.
CLKRUN#	110	I/O	CLKRUN# is an input/output pin for PCI clock status and an output to start or accelerate clock function.
PCIGNT#	111	I	PCI grant input.
PCIREQ#	112	O	PCI request output.
RST#	113	I	PCI bus reset.
INTA#	114	OD	Interrupt A request output, active-low. INTA# is the level triggered interrupt pin dedicated to servicing internal device interrupt requests.
PCICLK	115	I	PCI bus clock input.

ORDERING INFORMATION

Part Number	Description	Package
ES2842S	PCI V.90/V.92 HSP Modem LAN	128-pin LQFP

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