

## DRAM

## 1M x 16 DRAM EDO PAGE MODE

### FEATURES

- X16 organization
- EDO (Extended Data-Out) access mode
- 2  $\overline{\text{CAS}}$  Byte/Word Read/Write operation
- Single power supply :  
5V  $\pm$  10% Vcc for 5V product  
3.3V  $\pm$  10% Vcc for 3.3V product
- Interface for inputs and outputs  
TTL-compatible for 5V products  
LVTTTL-compatible for 3.3V products
- 1024-cycle refresh in 16ms
- Refresh modes :  $\overline{\text{RAS}}$  only,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  (CBR) and HIDDEN capabilities,
- Optional self-Refresh capabilities(S-ver. Only)
- JEDEC standard pinout
- Key AC Parameter

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>
-45	45	11	77	16
-50	50	13	84	20
-60	60	15	104	25

### ORDERING INFORMATION - PACKAGE

42-pin 400mil SOJ  
44 / 50-pin 400mil TSOP (Typell)

PRODUCT NO.	Refresh	Vcc	PACKING TYPE
M11B16161A-45J/50J/60J	Normal	5V	SOJ
M11B16161SA-45J/50J/60J	*Self-Refresh		
M11L16161A-45J/50J/60J	Normal	3.3V	
M11L16161SA-45J/50J/60J	Self-Refresh		
M11B16161A-45T/50T/60T	Normal	5V	TSOPII
M11B16161SA-45T/50T/60T	*Self-Refresh		
M11L16161A-45T/50T/60T	Normal	3.3V	
M11L16161SA-45T/50T/60T	Self-Refresh		

\* Ordered by special request

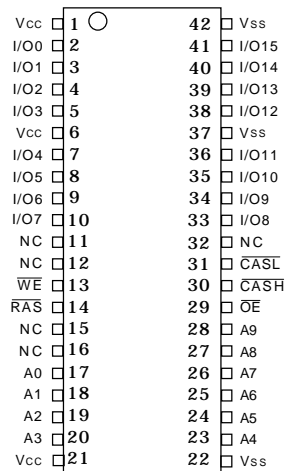
### GENERAL DESCRIPTION

The M11B16161/M11L16161 series is a randomly accessed solid state memory, organized as 1,048,576 x 16 bits device. It offers Extended Data-Output access mode. Single power supply (5V  $\pm$  10%, 3.3V  $\pm$  10%), access time (-45,-50,-60), self-refresh function and package type (SOJ, TSOP II) are optional features of this family. All these family have  $\overline{\text{CAS}}$  - before -  $\overline{\text{RAS}}$ ,  $\overline{\text{RAS}}$  -only refresh and Hidden refresh.

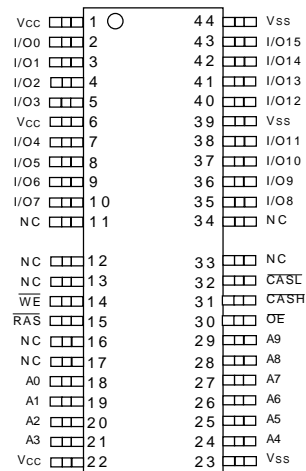
Two access modes are supported by this device : Byte access and Word access. Use only one of the two  $\overline{\text{CAS}}$  and leave the other staying high will result in a BYTE access. WORD access happens when two  $\overline{\text{CAS}}$  ( $\overline{\text{CASL}}$ ,  $\overline{\text{CASH}}$ ) are used.  $\overline{\text{CASL}}$  transiting low during READ or WRITE cycle will output or input data into the lower byte (IO0~IO7), and  $\overline{\text{CASH}}$  transiting low will output or input data into the upper byte (IO8~15).

### PIN ASSIGNMENT

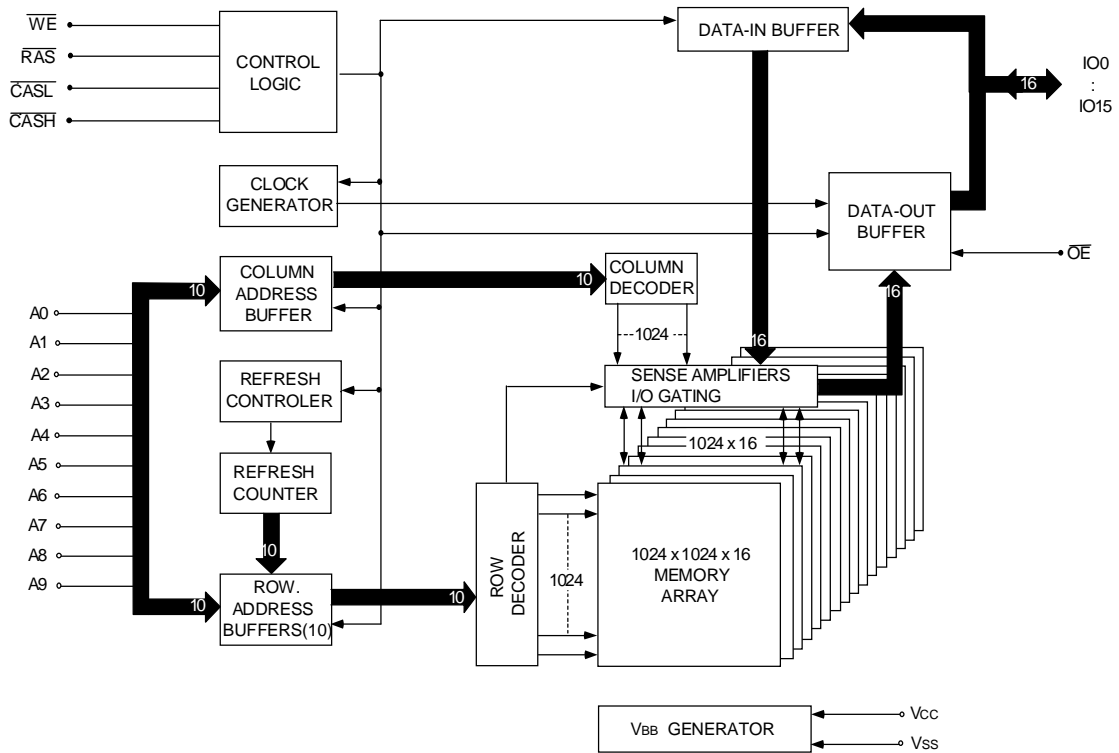
SOJ Top View



TSOP (Typell) Top View



## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTIONS

PIN NO. (SOJ Package)	PIN NAME	TYPE	DESCRIPTION
17~20, 23~28	A0~A9	Input	Address Input Row Address : A0~A9 Column Address : A0~A9
14	RAS	Input	Row Address Strobe
30	CASH	Input	Column Address Strobe / Upper Byte Control
31	CASL	Input	Column Address Strobe / Lower Byte Control
13	WE	Input	Write Enable
29	OE	Input	Output Enable
2~5, 7~10, 33~36, 38~41	I/O0 ~ I/O15	Input / Output	Data Input / Output
1, 6, 21	V <sub>cc</sub>	Supply	Power, (5V or 3.3V)
22, 37, 42	V <sub>ss</sub>	Ground	Ground
11, 12, 15, 16, 32	NC	-	No Connect

## ABSOLUTE MAXIMUM RATINGS

Voltage on Any pin Relative to V<sub>ss</sub>  
 5V Product                   ... -1V to +7V  
 3.3V Product                 ... -0.5V to +4.6V  
 Operating Temperature, T<sub>A</sub> (ambient)   ... 0 °C to +70 °C  
 Storage Temperature (plastic)           ... -55 °C to +150 °C  
 Power Dissipation                         ... 1.0W  
 Short Circuit Output Current             ... 50mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded. This is a stress rating only, and functional operation of the device above those conditions indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED

### OPERATING CONDITIONS (0 °C ≤ T<sub>A</sub> ≤ 70 °C)

PARAMETER	CONDITIONS	SYMBOL	3.3V		5V		UNITS	NOTES
			MIN	MAX	MIN	MAX		
Supply Voltage		V <sub>CC</sub>	3.0	3.6	4.5	5.5	V	1
Supply Voltage		V <sub>SS</sub>	0	0	0	0	V	
Input High Voltage		V <sub>IH</sub>	2.0	V <sub>CC</sub> +0.3	2.4	V <sub>CC</sub> +0.3	V	1
Input Low Voltage		V <sub>IL</sub>	-1.0	0.8	-1.0	0.8	V	1
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IH(max)</sub>	I <sub>LI</sub>	-10	10	-10	10	μA	
Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> Output(s) disable	I <sub>LO</sub>	-10	10	-10	10	μA	
Output High Voltage	5V   I <sub>OH</sub> = -5 mA	V <sub>OH</sub>	2.4	-	2.4	-	V	
	3.3V   I <sub>OH</sub> = -2 mA							
Output Low Voltage	5V   I <sub>OL</sub> = 4.2 mA	V <sub>OL</sub>	-	0.4	-	0.4	V	
	3.3V   I <sub>OL</sub> = 2 mA							

Note : 1.All Voltages referenced to V<sub>ss</sub>

PARAMETER	CONDITIONS	SYMBOL	MAX			UNITS	NOTES
			-45	-50	-60		
Operating Current	$\overline{RAS}$ , $\overline{CAS}$ cycling , t <sub>RC</sub> = min	I <sub>CC1</sub>	150	140	130	mA	1,2
Standby Current	TTL interface , $\overline{RAS}$ , $\overline{CAS}$ = V <sub>IH</sub> , D <sub>OUT</sub> =High-Z	I <sub>CC2</sub>	4	4	4	mA	
	CMOS interface, $\overline{RAS}$ , $\overline{CAS}$ ≥ V <sub>CC</sub> -0.2V		2	2	2	mA	
$\overline{RAS}$ only refresh Current	t <sub>RC</sub> = min	I <sub>CC3</sub>	150	140	130	mA	2
EDO Page Mode Current	t <sub>PC</sub> = min	I <sub>CC4</sub>	150	140	130	mA	1,3
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current	t <sub>RC</sub> = min	I <sub>CC6</sub>	150	140	130	mA	
Battery Backup Current (S-ver. Only)	Standby with CBR refresh, t <sub>RC</sub> = 62.4us t <sub>RAS</sub> ≤ 300ns, D <sub>OUT</sub> =Hi-Z, CMOS interface	I <sub>CC7</sub>	500	500	500	μA	
Self Refresh Current (S-ver. Only)	$\overline{RAS}$ , $\overline{CAS}$ ≤ 0.2V, D <sub>OUT</sub> =Hi-Z, CMOS interface	I <sub>CC8</sub>	500	500	500	μA	

Note : 1. I<sub>CC</sub> max is specified at the output open condition.  
 2. Address can be changed twice or less while  $\overline{RAS}$  =V<sub>IL</sub> .  
 3. Address can be changed once or less while  $\overline{CAS}$  =V<sub>IH</sub> .

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$  or  $3.3V \pm 10\%$ )

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input Capacitance (address)	C <sub>i1</sub>	-	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	C <sub>i2</sub>	-	7	pF
Output capacitance (I/O0~I/O15)	C <sub>i/o</sub>	-	10	pF

**AC ELECTRICAL CHARACTERISTICS** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$  or  $3.3V \pm 10\%$ ,  $V_{SS} = 0V$ ) (note 14)

Test Conditions

Input timing reference levels : 0.8V, 2.4V (for 5V power supply), 0.8V, 2.0V (for 3.3V power supply)

Output reference level :  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$

Output Load : 2TTL gate + CL (50pF)

Assumed  $t_r = 2ns$

PARAMETER	SYMBOL	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	t <sub>RC</sub>	77		84		104		ns	
Read Write Cycle Time	t <sub>RWC</sub>	97		110		135		ns	
EDO-Page-Mode Read or Write Cycle Time	t <sub>PC</sub>	16		20		25		ns	22
EDO-Page-Mode Read-Write Cycle Time	t <sub>PCM</sub>	53		58		68		ns	22
Access Time From $\overline{\text{RAS}}$	t <sub>RAC</sub>		45		50		60	ns	4
Access Time From $\overline{\text{CAS}}$	t <sub>CAC</sub>		11		13		15	ns	5,20
Access Time From $\overline{\text{OE}}$	t <sub>OAC</sub>		11		13		15	ns	13,20
Access Time From Column Address	t <sub>AA</sub>		22		25		30	ns	
Access Time From $\overline{\text{CAS}}$ Precharge	t <sub>ACP</sub>		25		28		33	ns	20
$\overline{\text{RAS}}$ Pulse Width	t <sub>RAS</sub>	45	10,000	50	10,000	60	10,000	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode)	t <sub>RASC</sub>	45	100,000	50	100,000	60	100,000	ns	
$\overline{\text{RAS}}$ Hold Time	t <sub>RSH</sub>	6		7		10		ns	25
$\overline{\text{RAS}}$ Precharge Time	t <sub>RP</sub>	28		30		40		ns	
$\overline{\text{CAS}}$ Pulse Width	t <sub>CAS</sub>	6	10,000	7	10,000	10	10,000	ns	24
$\overline{\text{CAS}}$ Hold Time	t <sub>CSH</sub>	35		37		40		ns	19
$\overline{\text{CAS}}$ Precharge Time	t <sub>CP</sub>	6		7		10		ns	6,23
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t <sub>RCD</sub>	10	34	11	37	14	45	ns	7,18
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t <sub>CRP</sub>	5		5		5		ns	19
Row Address Setup Time	t <sub>ASR</sub>	0		0		0		ns	
Row Address Hold Time	t <sub>RAH</sub>	6		7		10		ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	t <sub>RAD</sub>	8	23	9	25	12	30	ns	8
Column Address Setup Time	t <sub>ASC</sub>	0		0		0		ns	18
Column Address Hold Time	t <sub>CAH</sub>	6		7		10		ns	18
Column Address Hold Time (Reference to $\overline{\text{RAS}}$ )	t <sub>AR</sub>	40		44		55		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	t <sub>RAL</sub>	23		25		30		ns	
Column Address setup to $\overline{\text{CAS}}$ precharge	t <sub>ACH</sub>	10		11		13		ns	

(Continued)

PARAMETER	SYMBOL	-45		-50		-60		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	tRCS	0		0		0		ns	15,18
Read Command Hold Time Reference to $\overline{\text{CAS}}$	tRCH	0		0		0		ns	9,15,19
Read Command Hold Time Reference to $\overline{\text{RAS}}$	tRRH	0		0		0		ns	9
$\overline{\text{CAS}}$ to Output in Low-Z	tCLZ	0		0		0		ns	20
Output Buffer Turn-off Delay From $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	tOFF1	0	11	0	13	0	15	ns	10,17,20
Output Buffer Turn-off to $\overline{\text{OE}}$	tOFF2	0	11	0	13	0	15	ns	17,26
Write Command Setup Time	tWCS	0		0		0		ns	11,15,18
Write Command Hold Time	tWCH	6		7		10		ns	15,25
Write Command Hold Time(Reference to $\overline{\text{RAS}}$ )	tWCR	40		44		55		ns	15
Write Command Pulse Width	tWP	6		7		10		ns	15
Write Command to $\overline{\text{RAS}}$ Lead Time	tRWL	11		13		15		ns	15
Write Command to $\overline{\text{CAS}}$ Lead Time	tCWL	6		7		10		ns	15,19
Data-in Setup Time	tDS	0		0		0		ns	12,20
Data-in Hold Time	tDH	6		7		10		ns	12,20
Data-in Hold Time (Reference to $\overline{\text{RAS}}$ )	tDHR	40		44		55		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	tRWD	57		67		79		ns	11
Column Address to $\overline{\text{WE}}$ Delay Time	tAWD	34		42		49		ns	11
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tCWD	23		30		34		ns	11,18
Transition Time (rise or fall)	tT	1	50	1	50	1	50	ns	2,3
Refresh Period (1024 cycles)	tREF		16		16		16	ms	
Refresh Period (1024 cycles) Self Refresh	tREF		64		64		64	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	tRPC	5		5		5		ns	
$\overline{\text{CAS}}$ Setup Time(CBR REFRESH)	tCSR	5		5		5		ns	1,18
$\overline{\text{CAS}}$ Hold Time(CBR REFRESH)	tCHR	10		10		10		ns	1,19
$\overline{\text{OE}}$ Hold Time From $\overline{\text{WE}}$ During Read-Mode-Write Cycle	tOEH	6		7		10		ns	16
$\overline{\text{OE}}$ Low to $\overline{\text{CAS}}$ High Setup Time	tOES	5		5		5		ns	
$\overline{\text{OE}}$ High Hold Time From $\overline{\text{CAS}}$ High	tOEHC	2		2		2		ns	
$\overline{\text{OE}}$ Precharge Time	tOEP	2		2		2		ns	
$\overline{\text{OE}}$ Setup Prior to $\overline{\text{RAS}}$ During Hidden Refresh Cycle	tORD	0		0		0		ns	
Last $\overline{\text{CAS}}$ Going Low to First $\overline{\text{CAS}}$ Returning High	tCLCH	6		7		10		ns	21
Data Output Hold After $\overline{\text{CAS}}$ Returning Low	tCOH	3		3		3		ns	
Output Disable Delay From $\overline{\text{WE}}$	tWHZ	0	11	0	13	0	15	ns	
Self Refresh $\overline{\text{RAS}}$ Low Pulse width	tRASS	100		100		100		us	27,28
Self Refresh $\overline{\text{RAS}}$ High Precharge Time	tRPS	77		84		104		ns	27,28
Self Refresh $\overline{\text{CAS}}$ Hold Time	tCHS	-50		-50		-50		ns	27,28
Read Setup Time Reference to $\overline{\text{RAS}}$ in CBR/SR	tRSR	0		0		0		ns	27,28
Read Hold Time Reference to $\overline{\text{RAS}}$ in CBR/SR	tRHR	6		7		10		ns	27,28

**Notes :**

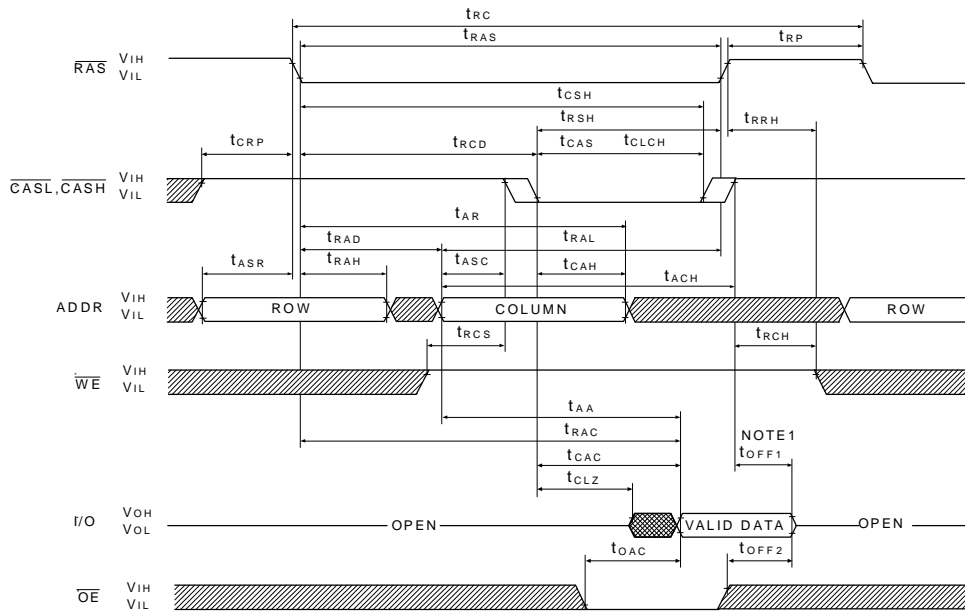
1. Enables on-chip refresh and address counters.
2.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
3. In addition to meet the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  in a monotonic manner.
4. Assume that  $t_{RCD} < t_{RCD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
5. Assume that  $t_{RCD} \geq t_{RCD}(\max)$
6. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{CAS}$  and  $\overline{RAS}$  must be pulsed high.
7. Operation within the  $t_{RCD}$  limit ensures that  $t_{RCD}(\max)$  can be met,  $t_{RCD}(\max)$  is specified as a reference point only ; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled by  $t_{CAC}$ .
8. Operation within the  $t_{RAD}$  limit ensures that  $t_{RAD}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only ; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled by  $t_{AA}$ .
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
10.  $t_{OFF1}(\max)$  defines the time at which the output achieves the open circuit condition ; it is not a reference to  $V_{OH}$  or  $V_{OL}$ .
11.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CWD} \geq t_{CWD}(\min)$ , the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{CAS}$  and  $\overline{RAS}$  or  $\overline{OE}$  go back to  $V_{IH}$ ) is indeterminate.  $\overline{OE}$  held high and  $\overline{WE}$  taken low after  $\overline{CAS}$  goes low result in a LATE WRITE ( $\overline{OE}$ -controlled) cycle.
12. Those parameters are referenced to  $\overline{CAS}$  leading edge in EARLY WRITE cycles and  $\overline{WE}$  leading edge in LATE WRITE or READ-MODIFY- WRITE cycles.
13. During a READ cycle, if  $\overline{OE}$  is low then taken HIGH before  $\overline{CAS}$  goes high, I/O goes open, if  $\overline{OE}$  is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of  $200\mu s$  is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$  only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycle wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
15. WRITE command is defined as  $\overline{WE}$  going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OFF2}$  and  $t_{OEH}$  met ( $\overline{OE}$  high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once  $t_{OFF1}$  or  $t_{OFF2}$  occur.
18. Referenced to the earlier  $\overline{CAS}$  falling edge.
19. Referenced to the latter  $\overline{CAS}$  rising edge.
20. Output parameter (I/O) is referenced to corresponding  $\overline{CAS}$  input, IO0~7 by  $\overline{CASL}$  and IO8~15 by  $\overline{CASH}$ .
21. Last falling  $\overline{CAS}$  edge to first rising  $\overline{CAS}$  edge.
22. Last rising  $\overline{CAS}$  edge to next cycle's last rising  $\overline{CAS}$  edge.
23. Last rising  $\overline{CAS}$  edge to first falling  $\overline{CAS}$  edge.
24. Each  $\overline{CAS}$  must meet minimum pulse width.
25. Referenced to the latter  $\overline{CAS}$  falling edge.
26. All IOs controlled by  $\overline{OE}$ , regardless  $\overline{CASL}$  and  $\overline{CASH}$ .
27. Self refresh mode is initiated by performing a CBR refresh cycle and holding  $\overline{RAS}$  low for the specified  $t_{RASS}$ . Self refresh mode is terminated by rising  $\overline{RAS}$  high for a minimum time of  $t_{RPS}$ .
28. For all of the refresh mode except the distributed CBR refresh mode, all rows must be refreshed within the refresh rate before and after self refresh.

## TRUTH TABLE

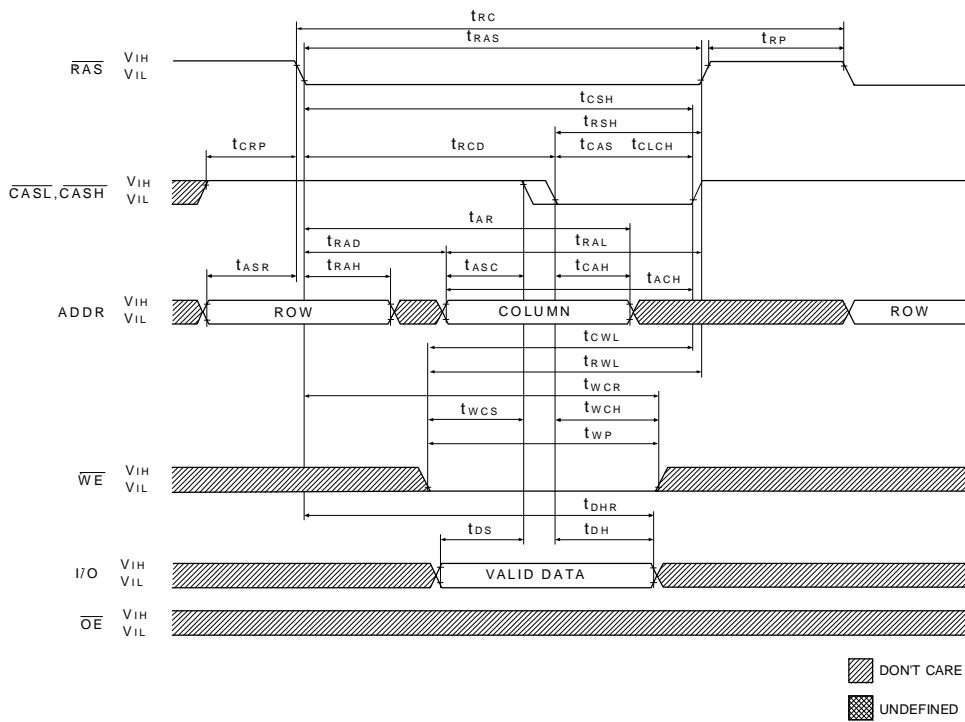
FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES		DQs	NOTES
							ROW	COL		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
Read : Word		L	L	L	H	L	ROW	COL	Data-Out	
Read : Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out	
Read : Upper Byte		L	H	L	H	L	ROW	COL	Upper Byte, Data-Out	
Write : Word (Early Write)		L	L	L	L	X	ROW	COL	Data-In	
Write : Lower Byte (Early)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In , Upper Byte, High-Z	
Write : Upper Byte (Early)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z , Upper Byte, Data-In	
Read-Write		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L		COL	Data-Out	2
	Any Cycle	L	L→H	L→H	H	L			Data-Out	2
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X		COL	Data-In	1
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H		COL	Data-Out, Data-In	1, 2
Hidden Refresh		L→H→L	L	L	H	L	ROW	COL	Data-Out	2
RAS -Only Refresh		L	H	H	X	X	ROW		High-Z	
CBR Refresh		H→L	L	L	H	X	X	X	High-Z	3

- \*Note : 1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).  
 2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).  
 3. Only one  $\overline{\text{CAS}}$  must be active ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ).

**READ CYCLE**



**EARLY WRITE CYCLE**

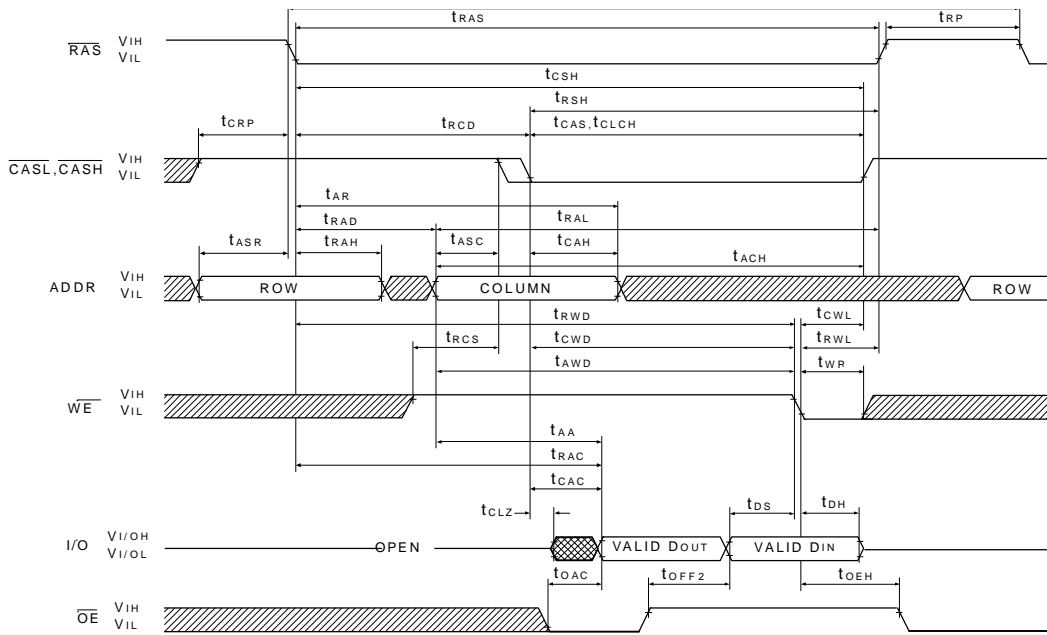


 DONT CARE  
 UNDEFINED

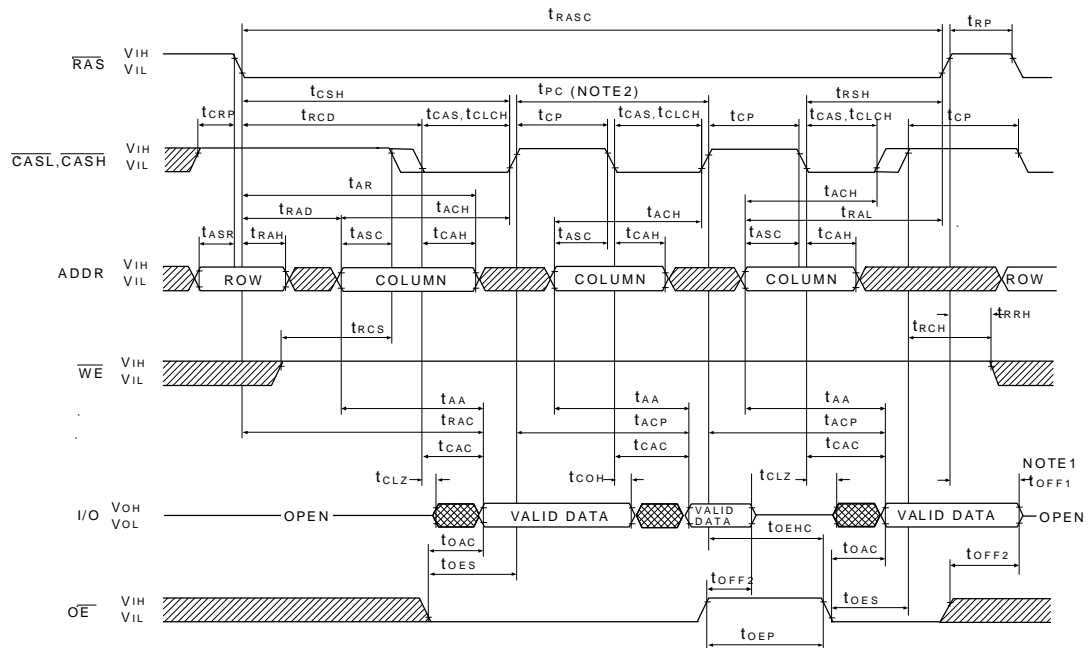
Note: 1.  $t_{OFF1}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.



**READ WRITE CYCLE  
(LATE WRITE and READ-MODIFY-WRITE CYCLES)**



**EDO-PAGE-MODE READ CYCLE**

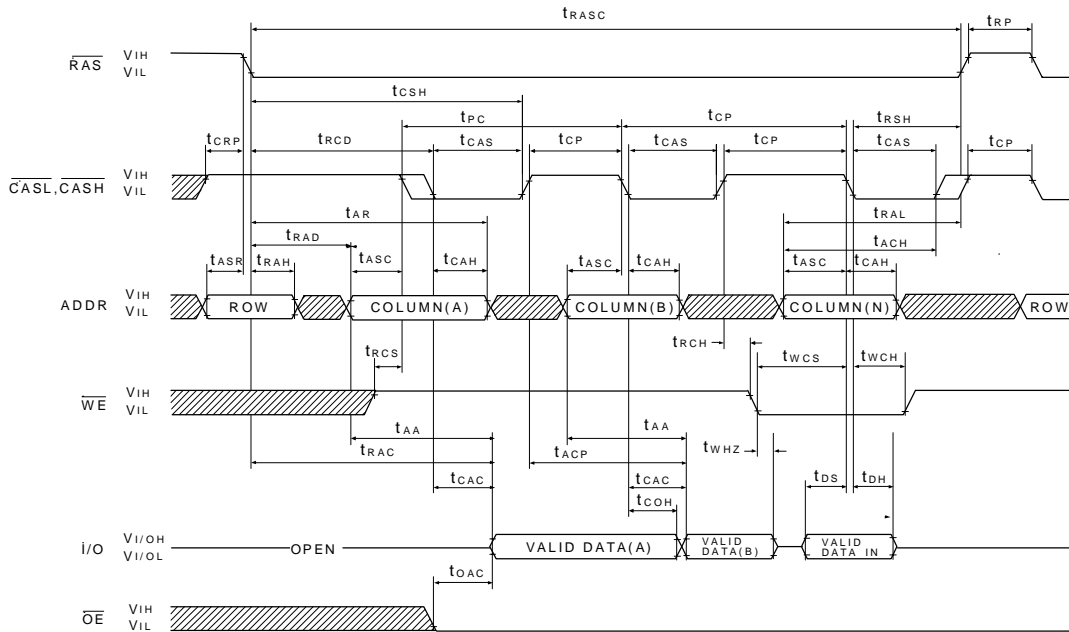


▨ DONT CARE  
▣ UNDEFINED

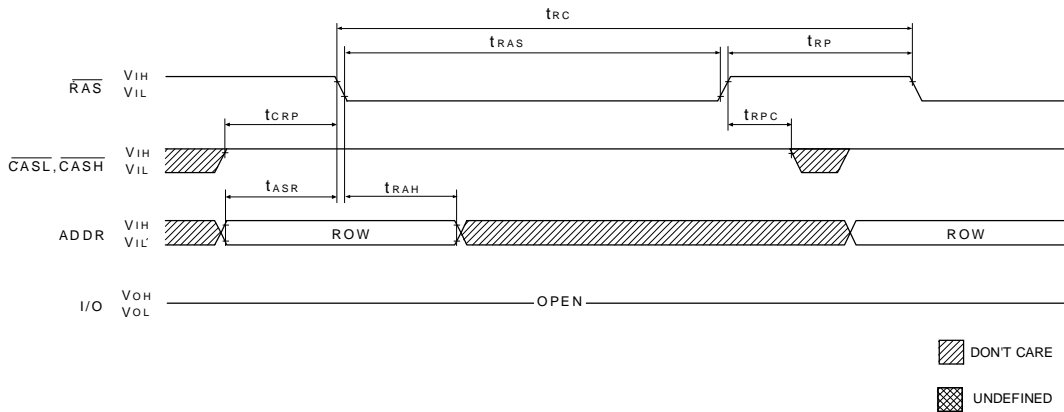
- \*NOTE : 1. t<sub>OFF1</sub> is referenced from the rising edge of  $\overline{\text{RAS}}$  or  $\overline{\text{CAS}}$ , whichever occurs last.  
2. t<sub>PC</sub> can be measured from falling edge of  $\overline{\text{CAS}}$  to falling edge of  $\overline{\text{CAS}}$ , or from rising edge of  $\overline{\text{CAS}}$  to rising edge of  $\overline{\text{CAS}}$ . Both measurements must meet the t<sub>PC</sub> specification.



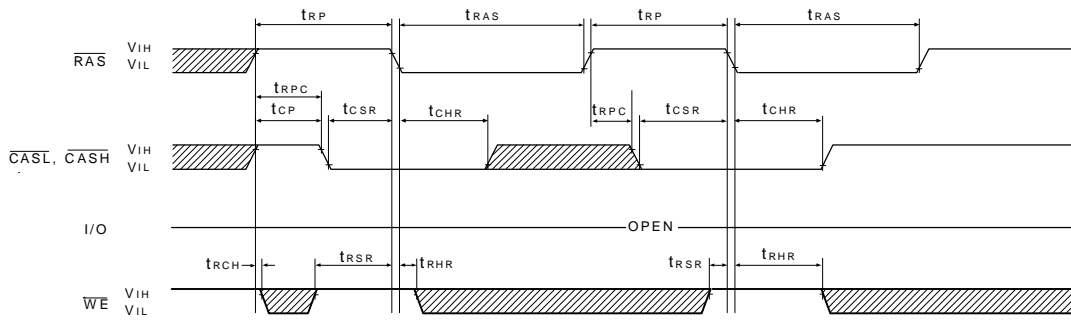
**EDO-PAGE-MODE READ-EARLY-WRITE CYCLE  
(Pseudo READ-MODIFY-WRITE)**



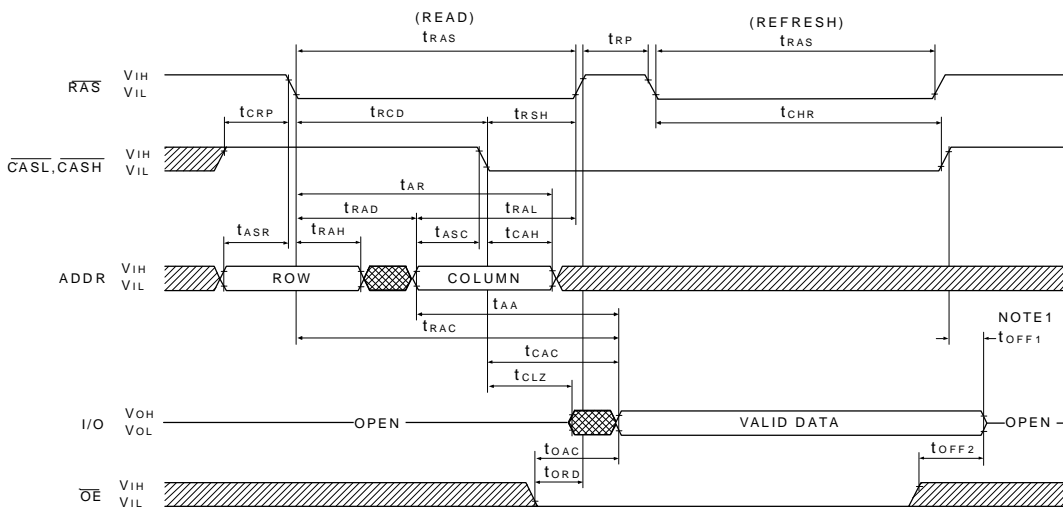
**$\overline{\text{RAS}}$  ONLY REFRESH CYCLE  
(ADDR = A0~A9 ;  $\overline{\text{OE}}$  ,  $\overline{\text{WE}}$  = DON'T CARE)**



**CBR REFRESH CYCLE  
(A0~A9 ;  $\overline{OE}$  = DON'T CARE)**



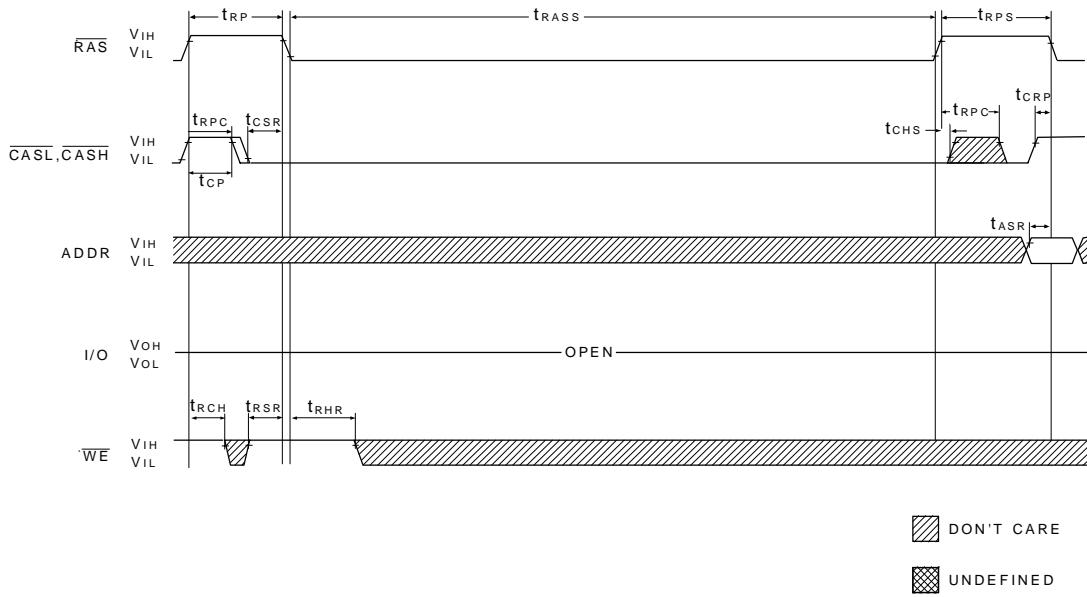
**HIDDEN REFRESH CYCLE  
( $\overline{WE}$  = HIGH ;  $\overline{OE}$  = LOW)**



▨ DON'T CARE  
▩ UNDEFINED

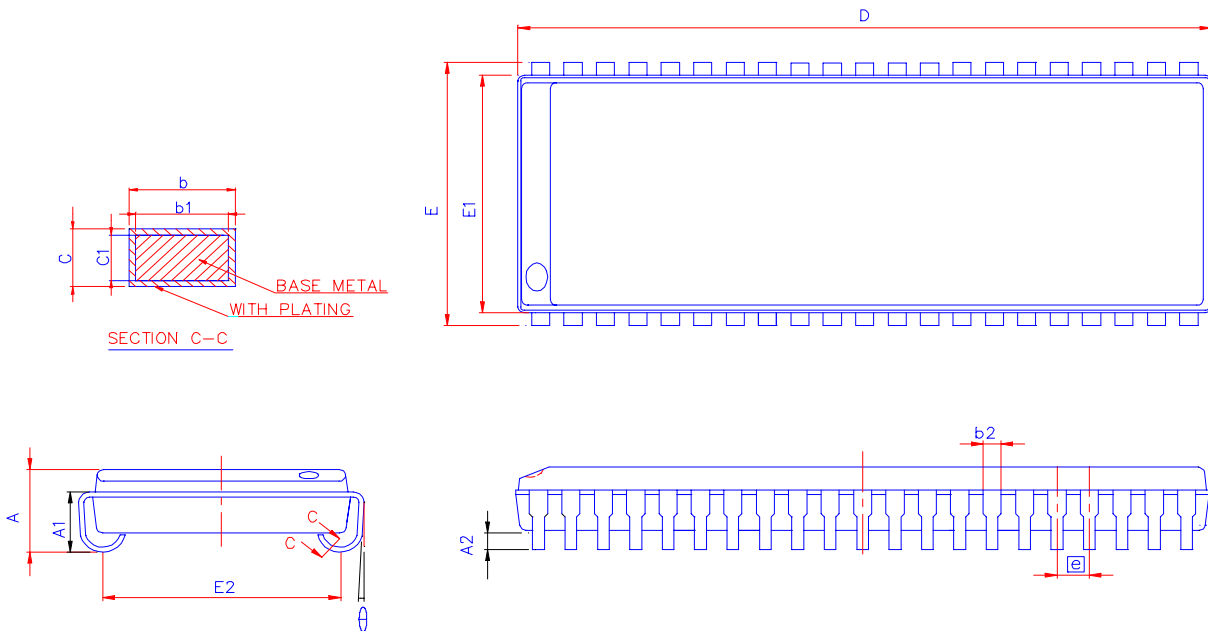
Note : 1.  $t_{OFF1}$  is reference from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$  , whichever occurs last.

**SELF REFRESH CYCLE  
( $\overline{OE}$  = DON'T CARE)**



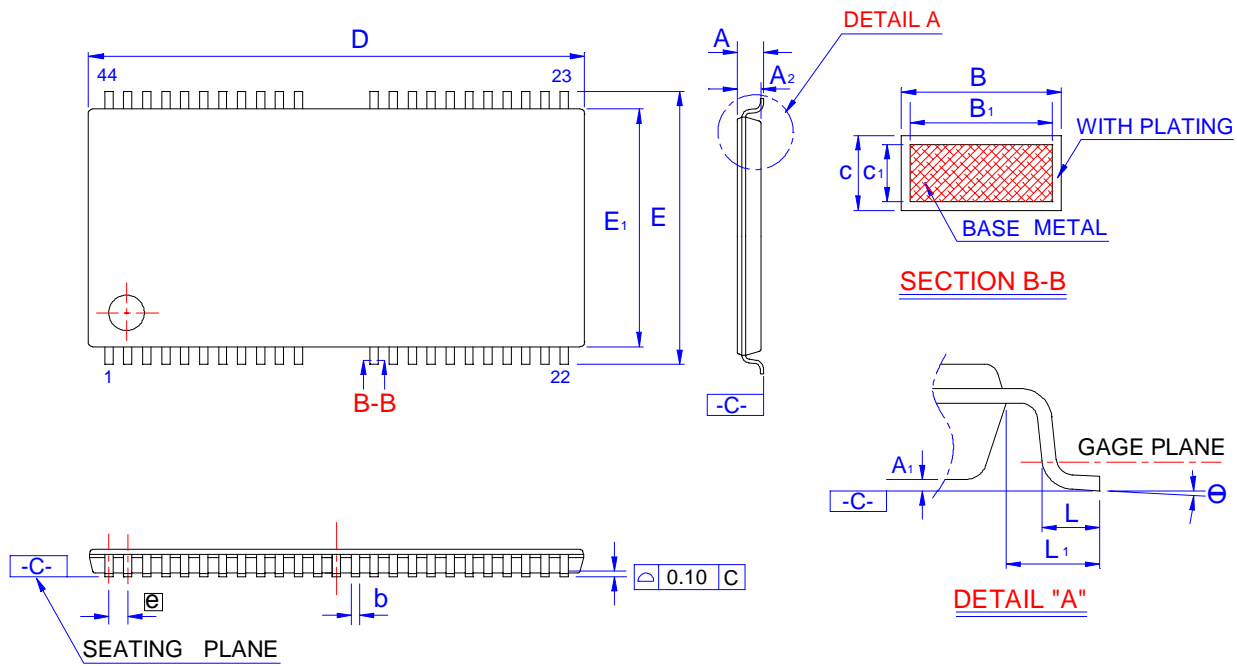
PACKING DIMENSIONS

42-LEAD SOJ(400mil)



Symbol	Dimension mm			Dimension inch		
	Min	Nom	Max	Min	Nom	Max
A	3.35	3.51	3.68	0.132	0.138	0.145
A1	2.24	-	-	0.088	-	-
A2	0.635	-	-	0.025	-	-
B	0.41	0.46	0.51	0.016	0.018	0.020
B1	0.46	0.41	0.38	0.018	0.016	0.015
B2	0.66	0.71	0.81	0.026	0.028	0.032
C	0.18	0.20	0.28	0.007	0.008	0.011
C1	0.28	0.20	0.17	0.011	0.008	0.007
D	27.18	27.31	27.43	1.070	1.075	1.080
ZD	1.09 REF			0.043 REF		
E	11.05	11.18	11.30	0.435	0.440	0.445
E1	10.03	10.06	10.29	0.395	0.400	0.405
E2	9.40 BASIC			0.370 BASIC		
$\theta$	0°		10°	0°		10°
e	1.27 BASIC			0.050 BASIC		

PACKING                      DIMENSIONS  
44 / 50-LEAD              TSOP(II)                      DRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.041
B	0.30	-	0.45	0.012	-	0.018
B1	0.30	0.35	0.40	0.012	0.014	0.016
C	0.12	-	0.21	0.005	-	0.008
C1	0.10	0.127	0.16	0.004	0.005	0.006
D	20.82	20.95	21.08	0.820	0.825	0.830
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.394	0.400	0.405
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.031 BSC		
θ	0	-	8	0	-	8

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