

## DRAM

## 256 K x 16 DRAM

## EDO PAGE MODE

### FEATURES

- X16 organization
- EDO (Extended Data-Output) access mode
- 2  $\overline{\text{CAS}}$  Byte/Word Read/Write operation
- Single 5V ( $\pm 10\%$ ) power supply
- TTL-compatible inputs and outputs
- 512-cycle refresh in 8ms
- Refresh modes :  $\overline{\text{RAS}}$  only,  $\overline{\text{CAS}}$  BEFORE  $\overline{\text{RAS}}$  (CBR) and HIDDEN
- JEDEC standard pinout
- Key AC Parameter

	t <sub>RAC</sub>	t <sub>CAC</sub>	t <sub>RC</sub>	t <sub>PC</sub>
-25	25	8	43	10
-28	28	9	48	11
-30	30	9	55	12
-35	35	10	65	14
-40	40	11	75	16

### ORDERING INFORMATION - PACKAGE

40-pin 400mil SOJ  
44 / 40-pin 400mil TSOP (Typell)

PRODUCT NO.	PACKING TYPE
M11B416256A-25J	SOJ
M11B416256A-28J	
M11B416256A-30J	
M11B416256A-35J	
M11B416256A-40J	
M11B416256A-25T	TSOPII
M11B416256A-28T	
M11B416256A-30T	
M11B416256A-35T	
M11B416256A-40T	

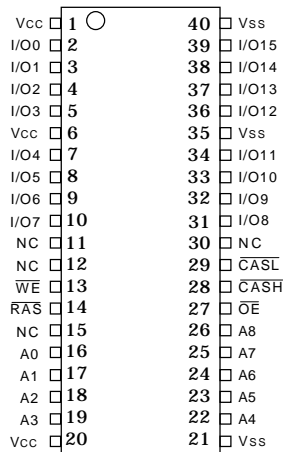
### GENERAL DESCRIPTION

The M11B416256A is a randomly accessed solid state memory, organized as 262,144 x 16 bits device. It offers Extended Data-Output , 5V ( $\pm 10\%$ ) single power supply. Access time (-25,-28,-30,-35,-40) and package type (SOJ, TSOP II) are optional features of this family. All these family have  $\overline{\text{CAS}}$  - before - $\overline{\text{RAS}}$  ,  $\overline{\text{RAS}}$  -only refresh and Hidden refresh capabilities.

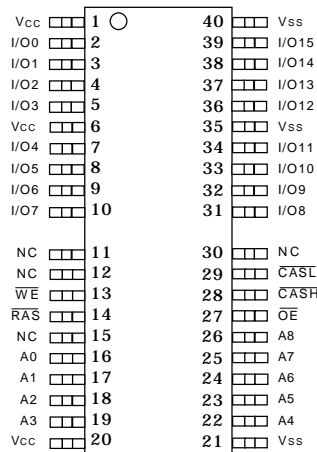
Two access modes are supported by this device : Byte access and Word access. Use only one of the two  $\overline{\text{CAS}}$  and leave the other staying high will result in a BYTE access. WORD access happens when two  $\overline{\text{CAS}}$  ( $\overline{\text{CASL}}$  ,  $\overline{\text{CASH}}$ ) are used.  $\overline{\text{CASL}}$  transiting low during READ or WRITE cycle will output or input data into the lower byte (IO0~IO7), and  $\overline{\text{CASH}}$  transiting low will output or input data into the upper byte (IO8~15).

### PIN ASSIGNMENT

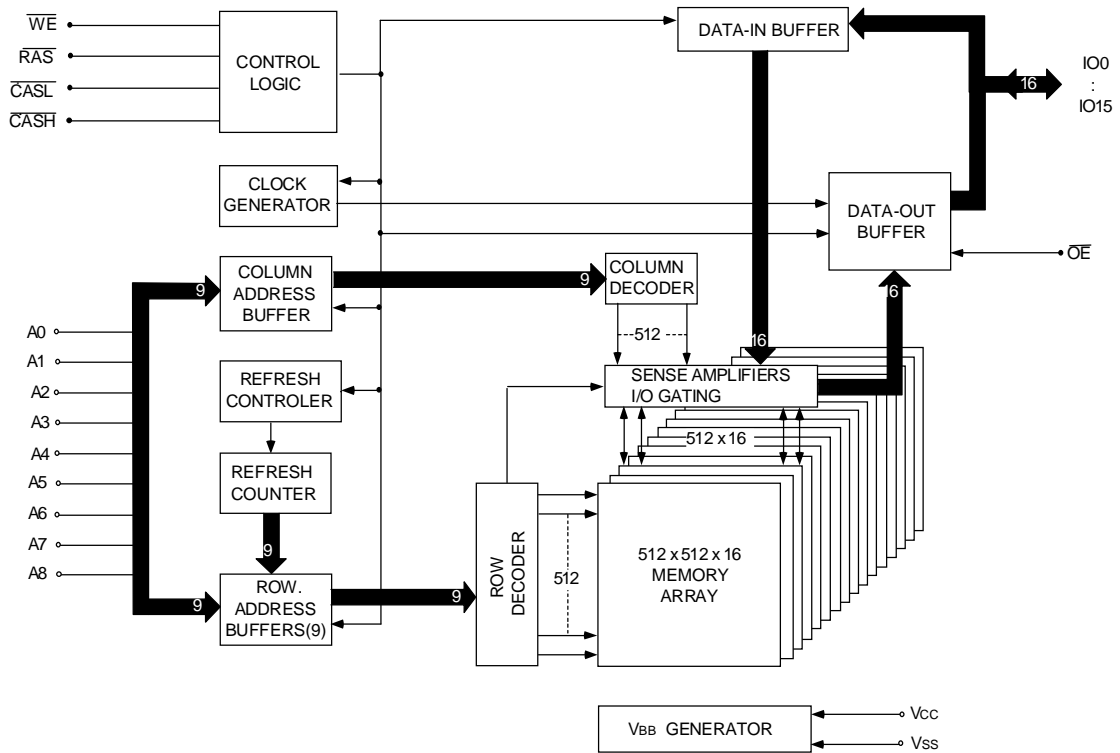
SOJ Top View



TSOP (Typell) Top View



## FUNCTIONAL BLOCK DIAGRAM



## PIN DESCRIPTIONS

PIN NO.	PIN NAME	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input Row Address : A0~A8 Column Address : A0~A8
14	RAS	Input	Row Address Strobe
28	CASH	Input	Column Address Strobe / Upper Byte Control
29	CASL	Input	Column Address Strobe / Lower Byte Control
13	WE	Input	Write Enable
27	OE	Input	Output Enable
2~5,7~10,31~34,36~39	I/O0 ~ I/O15	Input / Output	Data Input / Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

## ABSOLUTE MAXIMUM RATINGS

Voltage on Any pin Relative to Vss ... .....-1V to +7V  
 Operating Temperature, T<sub>A</sub> (ambient) ....0 °C to +70 °C  
 Storage Temperature (plastic) .....-55 °C to +150 °C  
 Power Dissipation .....1.43W  
 Short Circuit Output Current .....50mA

Permanent device damage may occur if “Absolute Maximum Ratings” are exceeded. This is a stress rating only, and functional operation of the device above those conditions indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC ELECTRICAL CHARACTERISTICS AND RECOMMENDED

### OPERATING CONDITIONS (0 °C ≤ T<sub>A</sub> ≤ 70 °C ; V<sub>CC</sub> = 5V ± 10% unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage		V <sub>CC</sub>	4.5	5.5	V	1
Supply Voltage		V <sub>SS</sub>	0	0	V	
Input High Voltage		V <sub>IH</sub>	2.4	V <sub>CC</sub> +0.3	V	1
Input Low Voltage		V <sub>IL</sub>	-0.3	0.8	V	1
Input Leakage Current	0V ≤ V <sub>IN</sub> ≤ V <sub>IH</sub> (max)	I <sub>LI</sub>	-10	10	μA	
Output Leakage Current	0V ≤ V <sub>OUT</sub> ≤ V <sub>CC</sub> Output(s) disable	I <sub>LO</sub>	-10	10	μA	
Output High Voltage	I <sub>OH</sub> = -5 mA	V <sub>OH</sub>	2.4	-	V	
Output Low Voltage	I <sub>OL</sub> = 4.2 mA	V <sub>OL</sub>	-	0.4	V	

Note : 1.All Voltages referenced to V<sub>SS</sub>

PARAMETER	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-25	-28	-30	-35	-40		
Operating Current	RAS̄, CAS̄ cycling, t <sub>RC</sub> = min	I <sub>CC1</sub>	210	190	170	150	135	mA	1,2
Standby Current	TTL interface, RAS̄, CAS̄ = V <sub>IH</sub> , D <sub>OUT</sub> = High-Z	I <sub>CC2</sub>	4	4	4	4	4	mA	
	CMOS interface, RAS̄, CAS̄ ≥ V <sub>CC</sub> - 0.2V		2	2	2	2	2	mA	
RAS̄ only refresh Current	t <sub>RC</sub> = min	I <sub>CC3</sub>	210	190	170	150	135	mA	2
EDO Page Mode Current	t <sub>PC</sub> = min	I <sub>CC4</sub>	210	190	170	150	135	mA	1,3
Standby Current	RAS̄ = V <sub>IH</sub> , CAS̄ = V <sub>IL</sub>	I <sub>CC5</sub>	5	5	5	5	5	mA	1
CAS̄ Before RAS̄ Refresh Current	t <sub>RC</sub> = min	I <sub>CC6</sub>	210	190	170	150	135	mA	

Note : 1. ICC max is specified at the output open condition.

2. Address can be changed twice or less while RAS̄ = V<sub>IL</sub>.

3. Address can be changed once or less while CAS̄ = V<sub>IH</sub>.

**CAPACITANCE** ( $T_a = 25^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	TYP	MAX	UNIT
Input Capacitance (address)	$C_{i1}$	-	5	pF
Input Capacitance ( $\overline{\text{RAS}}$ , $\overline{\text{CASH}}$ , $\overline{\text{CASL}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ )	$C_{i2}$	-	7	pF
Output capacitance (I/O0~I/O15)	$C_{i/o}$	-	10	pF

**AC ELECTRICAL CHARACTERISTICS** ( $T_a = 0$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 10\%$ ,  $V_{SS} = 0V$ ) (note 14)

## Test Conditions

Input timing reference levels : 0V, 3V

Output reference level :  $V_{OL} = 0.8V$ ,  $V_{OH} = 2.0V$ 

Output Load : 2TTL gate + CL (50pF)

Assumed  $t_r = 2\text{ns}$ 

PARAMETER	SYMBOL	-25		-28		-30		-35		-40		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read or Write Cycle Time	$t_{RC}$	43		48		55		65		75		ns	
Read Write Cycle Time	$t_{RWC}$	65		70		85		95		105		ns	
EDO-Page-Mode Read or Write Cycle Time	$t_{PC}$	10		11		12		14		16		ns	22
EDO-Page-Mode Read-Write Cycle Time	$t_{PCM}$	32		35		37		42		47		ns	22
Access Time From $\overline{\text{RAS}}$	$t_{RAC}$		25		28		30		35		40	ns	4
Access Time From $\overline{\text{CAS}}$	$t_{CAC}$		8		9		9		10		11	ns	5,20
Access Time From $\overline{\text{OE}}$	$t_{OAC}$		8		9		9		10		11	ns	13,20
Access Time From Column Address	$t_{AA}$		12		15		15		18		20	ns	
Access Time From $\overline{\text{CAS}}$ Precharge	$t_{ACP}$		14		17		17		20		22	ns	20
$\overline{\text{RAS}}$ Pulse Width	$t_{RAS}$	25	10K	28	10K	30	10K	35	10K	40	10K	ns	
$\overline{\text{RAS}}$ Pulse Width (EDO Page Mode)	$t_{RASC}$	25	100K	28	100K	30	100K	35	100K	40	100K	ns	
$\overline{\text{RAS}}$ Hold Time	$t_{RSH}$	8		9		9		10		11		ns	25
$\overline{\text{RAS}}$ Precharge Time	$t_{RP}$	15		17		20		25		30		ns	
$\overline{\text{CAS}}$ Pulse Width	$t_{CAS}$	4	10K	5	10K	5	10K	5	10K	6	10K	ns	24
$\overline{\text{CAS}}$ Hold Time	$t_{CSH}$	21		24		26		30		35		ns	19
$\overline{\text{CAS}}$ Precharge Time	$t_{CP}$	4		4		4		5		5		ns	6,23
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	$t_{RCD}$	10	17	10	19	10	21	10	25	10	29	ns	7,18
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	$t_{CRP}$	5		5		5		5		5		ns	19
Row Address Setup Time	$t_{ASR}$	0		0		0		0		0		ns	
Row Address Hold Time	$t_{RAH}$	5		5		5		5		5		ns	
$\overline{\text{RAS}}$ to Column Address Delay Time	$t_{RAD}$	8	13	8	13	8	15	8	17	8	20	ns	8
Column Address Setup Time	$t_{ASC}$	0		0		0		0		0		ns	18
Column Address Hold Time	$t_{CAH}$	5		5		5		5		5		ns	18
Column Address Hold Time (Reference to $\overline{\text{RAS}}$ )	$t_{AR}$	22		24		26		30		34		ns	
Column Address to $\overline{\text{RAS}}$ Lead Time	$t_{RAL}$	12		15		15		18		20		ns	

(Continued)

PARAMETER	SYMBOL	-25		-28		-30		-35		-40		UNIT	Notes
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Read Command Setup Time	tRCS	0		0		0		0		0		ns	15,18
Read Command Hold Time Reference to $\overline{\text{CAS}}$	tRCH	0		0		0		0		0		ns	9,15,19
Read Command Hold Time Reference to $\overline{\text{RAS}}$	tRRH	0		0		0		0		0		ns	9
$\overline{\text{CAS}}$ to Output in Low-Z	tCLZ	3		3		3		3		3		ns	20
Output Buffer Turn-off Delay From $\overline{\text{CAS}}$ or $\overline{\text{RAS}}$	tOFF1	3	15	3	15	3	15	3	15	3	15	ns	10,17,20
Output Buffer Turn-off to $\overline{\text{OE}}$	tOFF2		6		7		8		8		8	ns	17,26
Write Command Setup Time	tWCS	0		0		0		0		0		ns	11,15,18
Write Command Hold Time	tWCH	5		5		5		5		5		ns	15,25
Write Command Hold Time (Reference to $\overline{\text{RAS}}$ )	tWCR	22		24		26		30		34		ns	15
Write Command Pulse Width	tWP	5		5		5		5		5		ns	15
Write Command to $\overline{\text{RAS}}$ Lead Time	tRWL	7		7		8		9		10		ns	15
Write Command to $\overline{\text{CAS}}$ Lead Time	tCWL	5		5		6		7		8		ns	15,19
Data-in Setup Time	tDS	0		0		0		0		0		ns	12,20
Data-in Hold Time	tDH	5		5		5		5		5		ns	12,20
Data-in Hold Time (Reference to $\overline{\text{RAS}}$ )	tDHR	22		24		26		30		34		ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	tRWD	34		38		46		51		56		ns	11
Column Address to $\overline{\text{WE}}$ Delay Time	tAWD	21		25		31		34		36		ns	11
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time	tCWD	17		19		25		26		27		ns	11,18
Transition Time (rise or fall)	tT	1.5	50	1.5	50	1.5	50	2.5	50	2.5	50	ns	2,3
Refresh Period (512 cycles)	tREF		8		8		8		8		8	ms	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	tRPC	10		10		10		10		10		ns	
$\overline{\text{CAS}}$ Setup Time(CBR REFRESH)	tCSR	5		5		10		10		10		ns	1,18
$\overline{\text{CAS}}$ Hold Time(CBR REFRESH)	tCHR	7		7		10		10		10		ns	1,19
$\overline{\text{OE}}$ Hold Time From $\overline{\text{WE}}$ During Read-Mode-Write Cycle	tOEH	4		4		4		4		5		ns	16
$\overline{\text{OE}}$ Low to $\overline{\text{CAS}}$ High Setup Time	tOES	4		4		4		4		5		ns	
$\overline{\text{OE}}$ High Hold Time From $\overline{\text{CAS}}$ High	tOEHC	2		2		2		2		2		ns	
$\overline{\text{OE}}$ Precharge Time	tOEP	2		2		2		2		2		ns	
$\overline{\text{OE}}$ Setup Prior to $\overline{\text{RAS}}$ During Hidden Refresh Cycle	tORD	0		0		0		0		0		ns	
Last $\overline{\text{CAS}}$ Going Low to First $\overline{\text{CAS}}$ Returning High	tCLCH	4		5		5		5		6		ns	21
Data Output Hold After $\overline{\text{CAS}}$ Returning Low	tCOH	3		3		3		3		3		ns	
Output Disable Delay From $\overline{\text{WE}}$	tWHZ	3	7	3	7	3	7	3	7	3	7	ns	

## Notes :

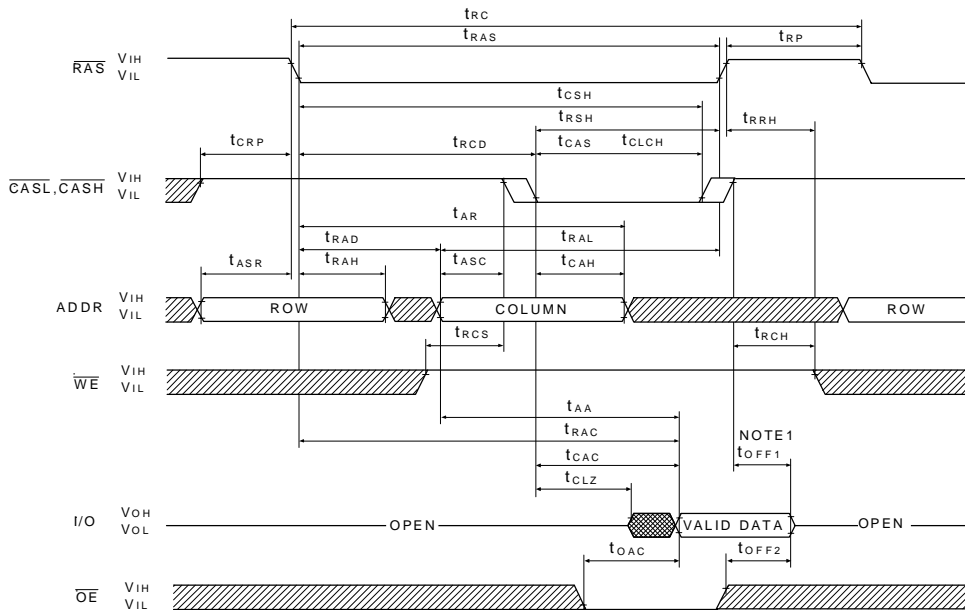
1. Enables on-chip refresh and address counters.
2.  $V_{IH}(\min)$  and  $V_{IL}(\max)$  are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
3. In addition to meet the transition rate specification, all input signals must transit between  $V_{IH}$  and  $V_{IL}$  in a monotonic manner.
4. Assume that  $t_{RCD} < t_{RCD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds the value shown.
5. Assume that  $t_{RCD} \geq t_{RCD}(\max)$
6. If  $\overline{CAS}$  is low at the falling edge of  $\overline{RAS}$ , data-out will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer,  $\overline{CAS}$  and  $\overline{RAS}$  must be pulsed high.
7. Operation within the  $t_{RCD}$  limit ensures that  $t_{RCD}(\max)$  can be met,  $t_{RCD}(\max)$  is specified as a reference point only ; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled by  $t_{CAC}$ .
8. Operation within the  $t_{RAD}$  limit ensures that  $t_{RAD}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only ; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled by  $t_{AA}$ .
9. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied for a READ cycle.
10.  $t_{OFF1}(\max)$  defines the time at which the output achieves the open circuit condition ; it is not a reference to  $V_{OH}$  or  $V_{OL}$ .
11.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are restrictive operating parameters in LATE WRITE and READ-MODIFY-WRITE cycle only. If  $t_{WCS} \geq t_{WCS}(\min)$ , the cycle is an EARLY WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If  $t_{RWD} \geq t_{RWD}(\min)$ ,  $t_{AWD} \geq t_{AWD}(\min)$  and  $t_{CWD} \geq t_{CWD}(\min)$ , the cycle is READ-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of I/O (at access time and until  $\overline{CAS}$  and  $\overline{RAS}$  or  $\overline{OE}$  go back to  $V_{IH}$ ) is indeterminate.  $\overline{OE}$  held high and  $\overline{WE}$  taken low after  $\overline{CAS}$  goes low result in a LATE WRITE ( $\overline{OE}$ -controlled) cycle.
12. Those parameters are referenced to  $\overline{CAS}$  leading edge in EARLY WRITE cycles and  $\overline{WE}$  leading edge in LATE WRITE or READ-MODIFY-WRITE cycles.
13. During a READ cycle, if  $\overline{OE}$  is low then taken HIGH before  $\overline{CAS}$  goes high, I/O goes open, if  $\overline{OE}$  is tied permanently low, a LATE WRITE or READ-MODIFY-WRITE operation is not possible.
14. An initial pause of 100ms is required after power-up followed by eight  $\overline{RAS}$  refresh cycles ( $\overline{RAS}$  only or CBR) before proper device operation is assured. The eight  $\overline{RAS}$  cycle wake-ups should be repeated any time the  $t_{REF}$  refresh requirement is exceeded.
15. WRITE command is defined as  $\overline{WE}$  going low.
16. LATE WRITE and READ-MODIFY-WRITE cycles must have both  $t_{OFF2}$  and  $t_{OEH}$  met ( $\overline{OE}$  high during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycles.
17. The I/Os open during READ cycles once  $t_{OFF1}$  or  $t_{OFF2}$  occur.
18. Referenced to the earlier  $\overline{CAS}$  falling edge.
19. Referenced to the latter  $\overline{CAS}$  rising edge.
20. Output parameter (I/O) is referenced to corresponding  $\overline{CAS}$  input, IO0~7 by  $\overline{CASL}$  and IO8~15 by  $\overline{CASH}$ .
21. Last falling  $\overline{CAS}$  edge to first rising  $\overline{CAS}$  edge.
22. Last rising  $\overline{CAS}$  edge to next cycle's last rising  $\overline{CAS}$  edge.
23. Last rising  $\overline{CAS}$  edge to first falling  $\overline{CAS}$  edge.
24. Each  $\overline{CAS}$  must meet minimum pulse width.
25. Referenced to the latter  $\overline{CAS}$  falling edge.
26. All IOs controlled by  $\overline{OE}$ , regardless  $\overline{CASL}$  and  $\overline{CASH}$ .

## TRUTH TABLE

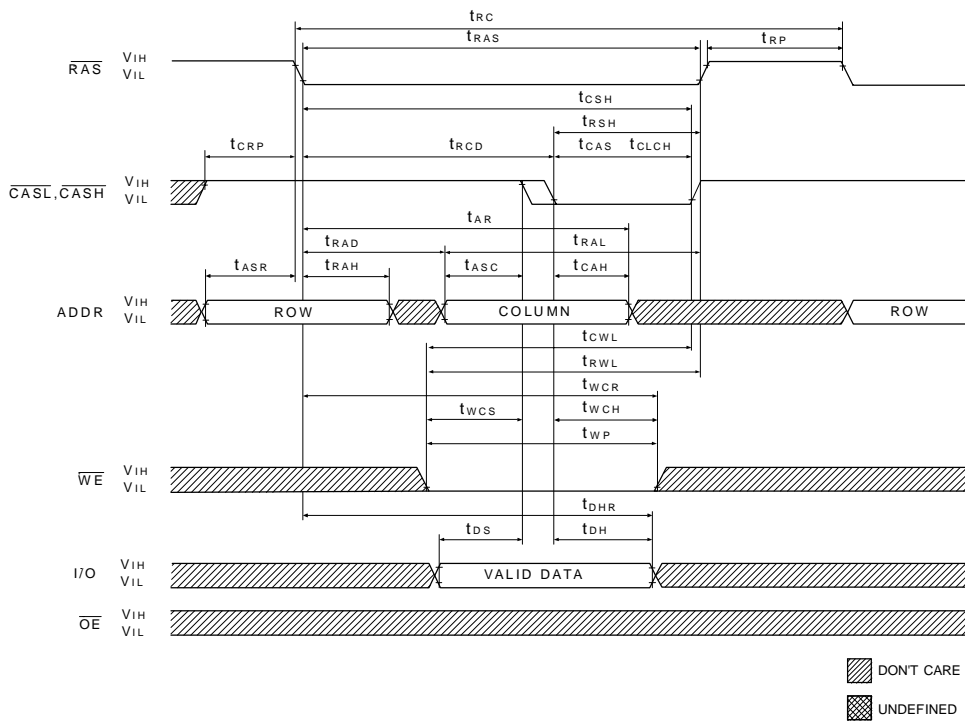
FUNCTION		RAS	CASL	CASH	WE	OE	ADDRESSES		DQs	NOTES
							ROW	COL		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
Read : Word		L	L	L	H	L	ROW	COL	Data-Out	
Read : Lower Byte		L	L	H	H	L	ROW	COL	Lower Byte, Data-Out	
Read : Upper Byte		L	H	L	H	L	ROW	COL	Upper Byte, Data-Out	
Write : Word (Early Write)		L	L	L	L	X	ROW	COL	Data-In	
Write : Lower Byte (Early)		L	L	H	L	X	ROW	COL	Lower Byte, Data-In , Upper Byte, High-Z	
Write : Upper Byte (Early)		L	H	L	L	X	ROW	COL	Lower Byte, High-Z , Upper Byte, Data-In	
Read-Write		L	L	L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-Out	2
	2nd Cycle	L	H→L	H→L	H	L		COL	Data-Out	2
	Any Cycle	L	L→H	L→H	H	L			Data-Out	2
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-In	1
	2nd Cycle	L	H→L	H→L	L	X		COL	Data-In	1
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H		COL	Data-Out, Data-In	1, 2
Hidden Refresh		L→H→L	L	L	H	L	ROW	COL	Data-Out	2
RAS -Only Refresh		L	H	H	X	X	ROW		High-Z	
CBR Refresh		H→L	L	L	H	X	X	X	High-Z	3

- \*Note : 1. These WRITE cycles may also be BYTE WRITE cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).  
 2. These READ cycles may also be BYTE READ cycles (either  $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$  active).  
 3. Only one  $\overline{\text{CAS}}$  must be active ( $\overline{\text{CASL}}$  or  $\overline{\text{CASH}}$ ).

**READ CYCLE**



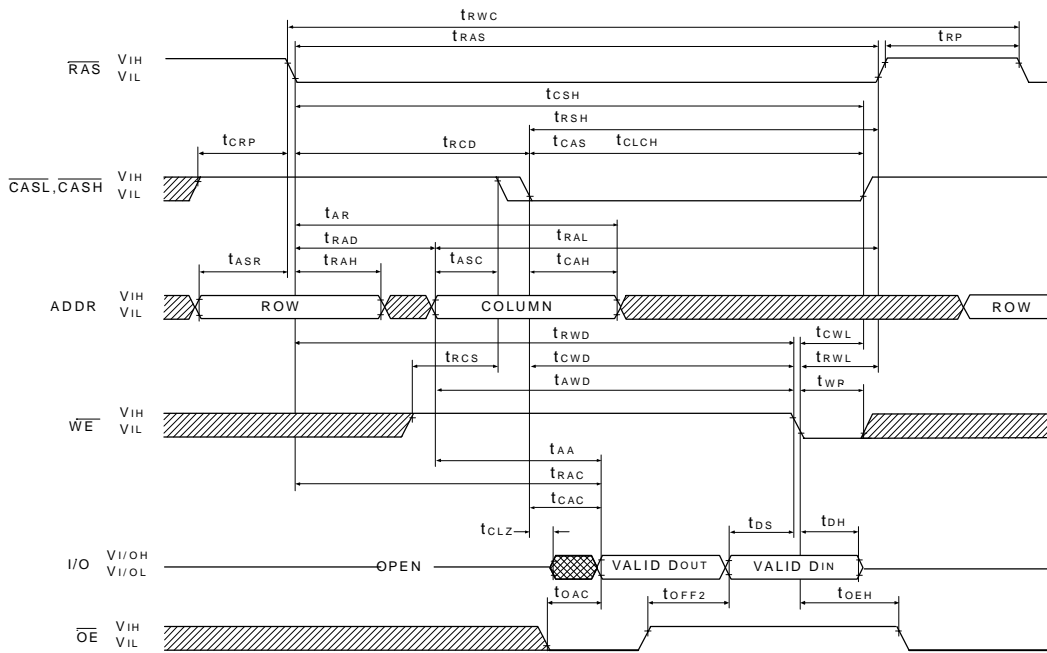
**EARLY WRITE CYCLE**



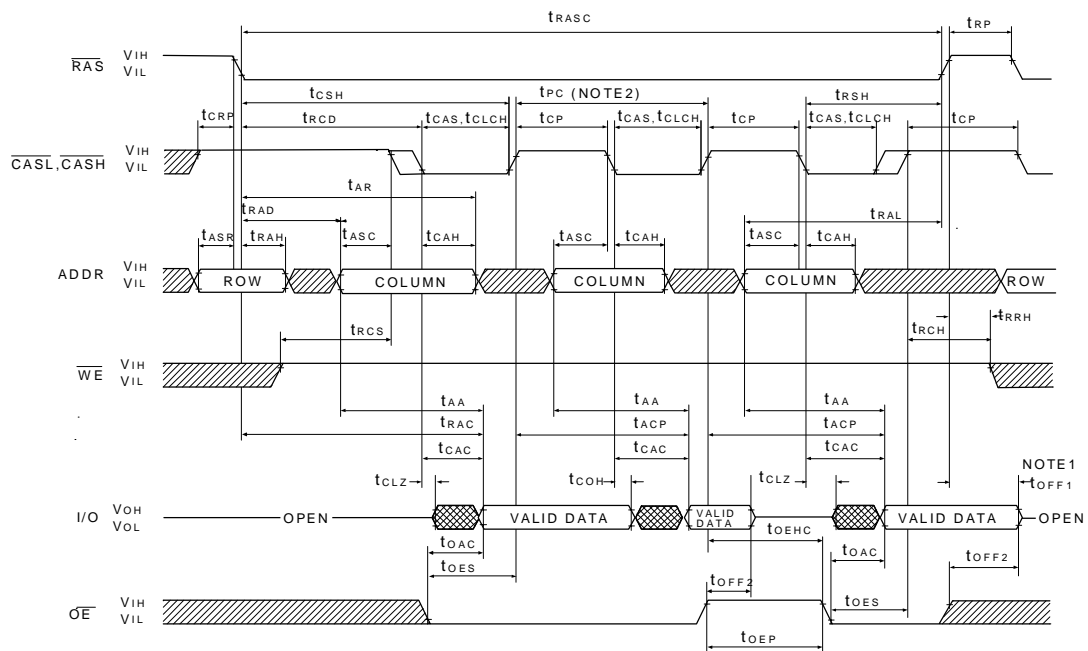
Note: 1.  $t_{OFF1}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.



**READ WRITE CYCLE  
(LATE WRITE and READ-MODIFY-WRITE CYCLES)**



**EDO-PAGE-MODE READ CYCLE**

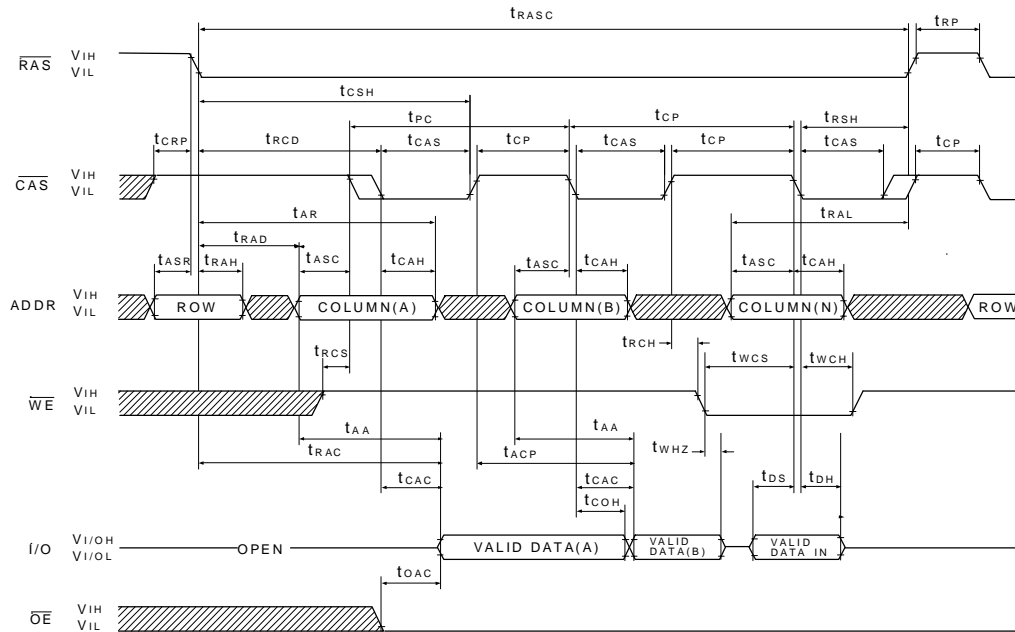


▨ DONT CARE  
▩ UNDEFINED

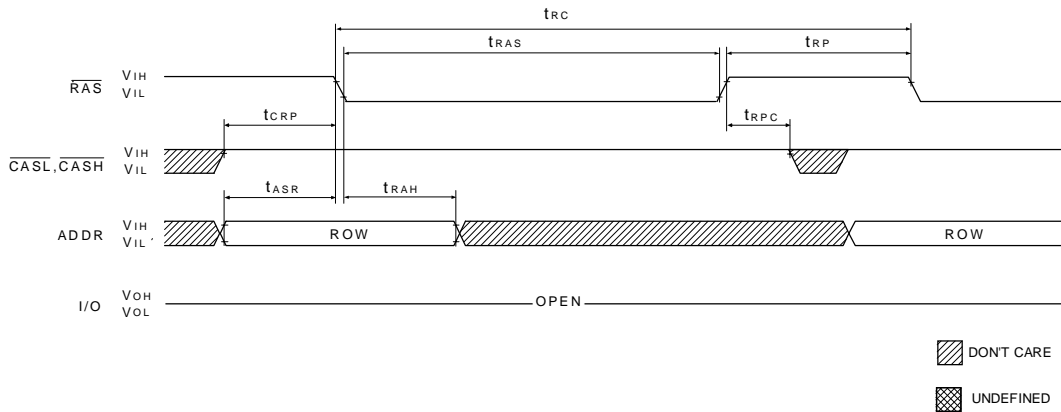
- \*NOTE : 1.  $t_{OFF1}$  is referenced from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$ , whichever occurs last.  
 2.  $t_{PC}$  can be measured from falling edge of  $\overline{CAS}$  to falling edge of  $\overline{CAS}$ , or from rising edge of  $\overline{CAS}$  to rising edge of  $\overline{CAS}$ . Both measurements must meet the  $t_{PC}$  specification.



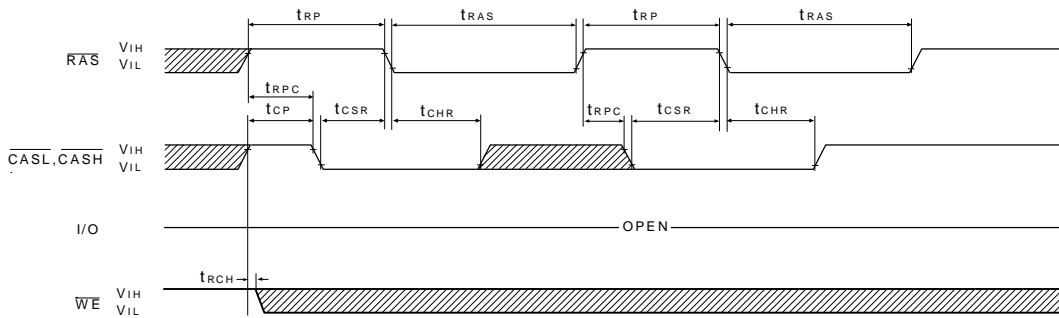
**EDO-PAGE-MODE READ-EARLY-WRITE CYCLE  
(Pseudo READ-MODIFY-WRITE)**



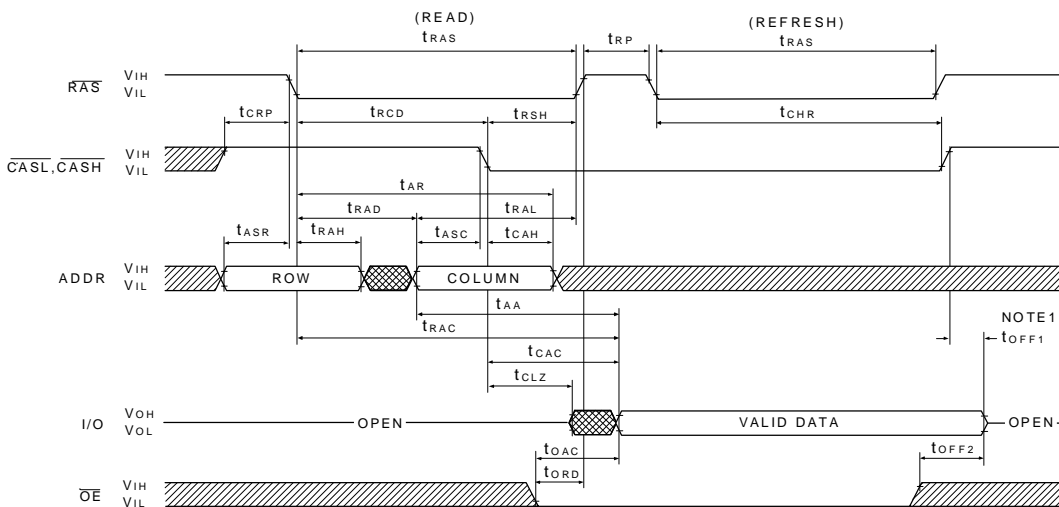
**RAS ONLY REFRESH CYCLE  
(ADDR = A0~A8 ; OE , WE = DON'T CARE)**



**CBR REFRESH CYCLE  
(A0~A8 ;  $\overline{OE}$  = DON'T CARE)**



**HIDDEN REFRESH CYCLE  
( $\overline{WE}$  = HIGH ;  $\overline{OE}$  = LOW)**



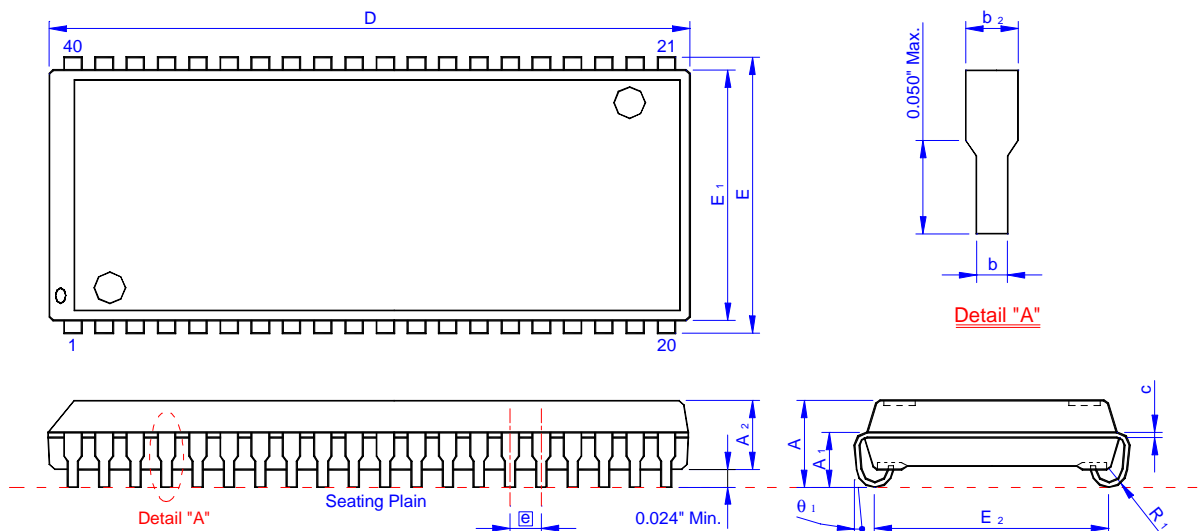
 DON'T CARE  
 UNDEFINED

Note : 1.  $t_{OFF1}$  is reference from the rising edge of  $\overline{RAS}$  or  $\overline{CAS}$  , whichever occurs last.

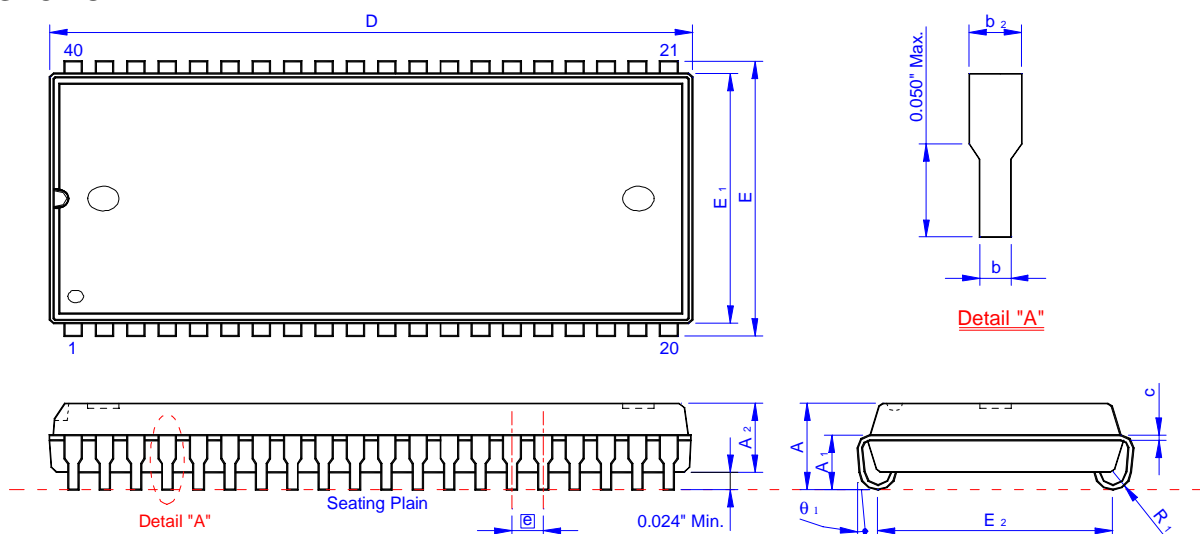
## PACKING DIMENSIONS

40-LEAD SOJ(400mil)

### SECTION I



### SECTION II



Symbol	Dimension in mm			Dimension in inch			Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max		Min	Norm	Max	Min	Norm	Max
A	3.250	3.510	3.760	0.128	0.138	0.148	E	10.920	11.176	11.430	0.430	0.440	0.450
A 1	2.080	___	___	0.082	___	___	E 1	10.030	10.160	10.290	0.395	0.400	0.405
A 2	2.790 REF			0.110 REF			E 2	9.40 BSC			0.370 BSC		
b	0.380	0.460	0.560	0.015	0.018	0.022	R 1	0.760	0.890	1.020	0.030	0.035	0.040
b2	0.635 REF			0.025 REF			theta 1	0°	___	10°	0°	___	10°
c	0.180	0.250	0.360	0.007	0.010	0.014	D	25.91	26.040	26.290	1.02	1.025	1.035
e	1.270 BSC			0.050 BSC									

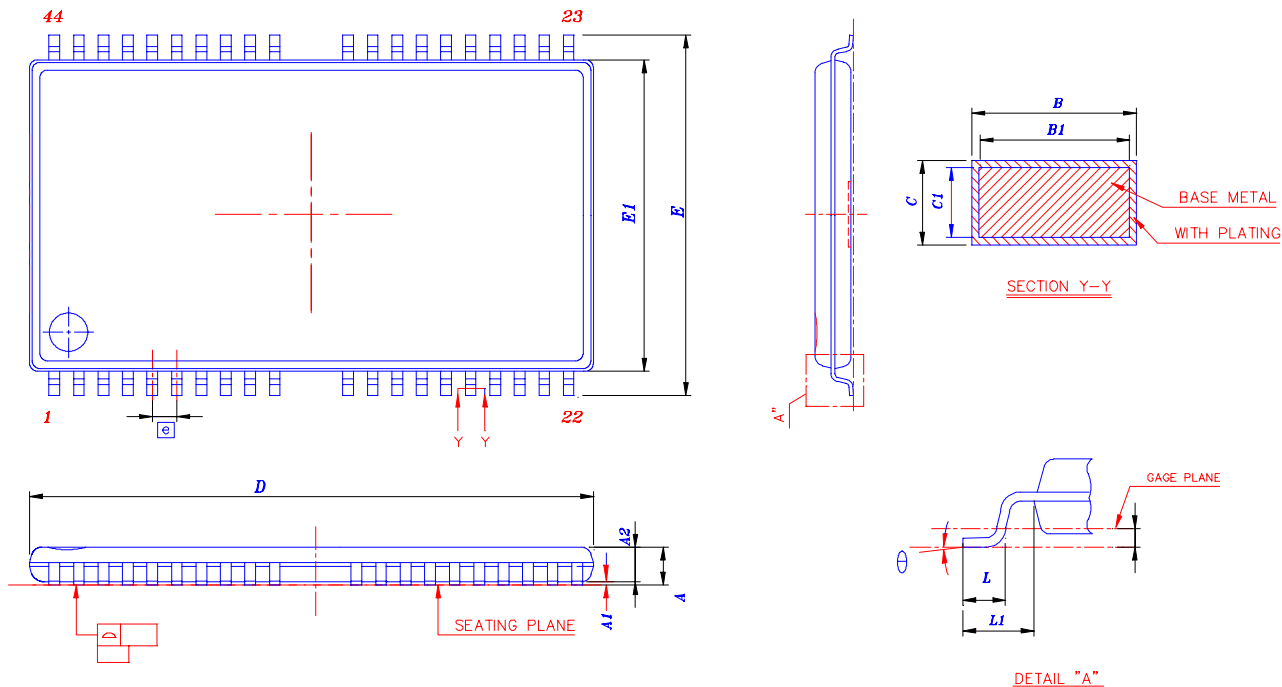
PACKING

DIMENSIONS

40 / 44-LEAD

TSOP(II)

DRAM(400mil)



Symbol	Dimension in mm			Dimension in inch		
	Min	Norm	Max	Min	Norm	Max
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	0.95	1.00	1.05	0.037	0.039	0.042
b	0.30	—	0.45	0.012	—	0.018
b1	0.30	0.35	0.40	0.012	0.014	0.016
c	0.12	—	0.21	0.005	—	0.008
c1	0.10	—	0.16	0.004	—	0.006
D	18.28	18.41	18.54	0.720	0.725	0.730
ZD	0.805 REF			0.0317 REF		
E	11.56	11.76	11.96	0.455	0.463	0.471
E1	10.03	10.16	10.29	0.395	0.400	0.4
L	0.40	0.59	0.69	0.016	0.023	0.027
L1	0.80 REF			0.031 REF		
e	0.80 BSC			0.0315 BSC		
θ	0° ~ 7° REF			0° ~ 7° REF		

### **Important Notice**

All rights reserved.

No part of this document may be reproduced or duplicated in any form or by any means without the prior permission of EliteMT.

The contents contained in this document are believed to be accurate at the time of publication. EliteMT assumes no responsibility for any error in this document, and reserves the right to change the products or specification in this document without notice.

The information contained herein is presented only as a guide or examples for the application of our products. No responsibility is assumed by EliteMT for any infringement of patents, copyrights, or other intellectual property rights of third parties which may result from its use. No license, either express, implied or otherwise, is granted under any patents, copyrights or other intellectual property rights of EliteMT or others.

Any semiconductor devices may have inherently a certain rate of failure. To minimize risks associated with customer's application, adequate design and operating safeguards against injury, damage, or loss from such failure, should be provided by the customer when making application designs.

EliteMT's products are not authorized for use in critical applications such as, but not limited to, life support devices or system, where failure or abnormal operation may directly affect human lives or cause physical injury or property damage. If products described here are to be used for such kinds of application, purchaser must do its own quality assurance testing appropriate to such applications.